SCTD001

Telecommunications Circuits Data Book

1986

Data Transmission, Switching, and Subscriber Set Products

TEXAS INSTRUMENTS

Telecommunications Circuits Data Book 1986

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TELECOM SELECTION GUIDE

SWITCHING AND TRANSMISSION PRODUCTS

DESCRIPTION	DEVICE NUMBER	PROCESS PACKAGE	SUPPLY VOLTAGE	PAGE
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HDB3/AMI — Encoder/Decoder	TCM2222	NMOS 16-Pin J	5 V	2-29
Line Interface	TCM2203	Bipolar 28-Pin J	5 V	2-45

CODECS, FILTERS, COMBOS

DESCRIPTION	DEVICE NUMBER	PROCESS PACKAGE	SUPPLY VOLTAGE	PAGE
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PCM Codec — μ-Law	TCM2910A	NMOS 24-Pin J	12 V, ±5 V	2-55
PCM Line Filter	TCM2912B	NMOS 16-Pin J	±5 V	2-75
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Synchronous/Asynchronous	TCM2914	NMOS 24-Pin J 28-Pin FN	±5 V	2-89
μ-Law	TCM2916	NMOS 16-Pin J	±5 V	2-89
A-Law	TCM2917	NMOS 16-Pin J	±5 V	2-89
Synchronous	TCM29C13	CMOS 20-Pin J	±5 V	2-111
Synchronous/Asynchronous	TCM29C14	CMOS 24-Pin J 28-Pin FN	±5 V	2-111
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A-Law	TCM29C17	CMOS 16-Pin J	±5 V	2-111

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DESCRIPTION	DEVICE NUMBER	PROCESS PACKAGE	SUPPLY VOLTAGE	PAGE
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DESCRIPTION	DEVICE NUMBER	PROCESS PACKAGE	SUPPLY VOLTAGE	PAGE
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Flux Canceling	TCM4207A	CMOS 24-Pin J	±5 V	2-155
Quad DC-DC Converter	TCM4208	CMOS 20-Pin J	±5 V	2-175
Quad Telephone Relay Driver	DS3680	Bipolar 14-Pin D 14-Pin N 14-Pin J	5 V, −60 V 5 V, −60 V 5 V, −60 V	2-3
Octal Asynchronous Receiver/ Transmitter	TCM78808	NMOS 68-Pin FN, HA, HB	5 V	2-193

SUBSCRIBER PRODUCTS

DESCRIPTION	DEVICE NUMBER	PROCESS PACKAGE	SUPPLY VOLTAGE	PAGE
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Ringer – 0.5 kHz Output	TCM1506A	BIDFET 8-Pin P	40-150 Vac	2-7
Ringer – 1.250 kHz Output	TCM1512A	BIDFET 8-Pin P	40-150 Vac	2-7
Ringer – 2 kHz Output	TCM1531	BIDFET 8-Pin P	40-150 Vac	2-21
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Ringer – 1.250 kHz Output	TCM1532	BIDFET 8-Pin P	40-150 Vac	2-21
Ringer – 1.250 kHz Output	TCM1532A	BIDFET 8-Pin P	40-150 Vac	2-21
Ringer – 0.5 kHz Output	TCM1536	BIDFET 8-Pin P	40-150 Vac	2-21
Ringer – 0.5 kHz Output	TCM1536A	BIDFET 8-Pin P	40-150 Vac	2-21
Ringer – 1.8 kHz Output	TCM1539	BIDFET 8-Pin P	40-150 Vac	2-21
Ringer – 1.8 kHz Output	TCM1539A	BIDFET 8-Pin P	40-150 Vac	2-?
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DTMF Encoder—Standard	TCM5087	CMOS 16-[illegible] N	3.5 [illegible] V	2-181
DTMF Encoder—Electronic Input	TCM5089	CMOS 16 Pin N	3.0 – [illegible] V	2-187
Tone/Pulse Dialer	TMS99531	NMOS 14-Pin N	5 V. – 2 V	2-219
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Transient Voltage Suppressor	TISP229A	Bipolar TO-220	200 V	2-211
Transient Voltage Suppressor	TISP318A	Bipolar TO-220	120 V	2-215
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ADC

Analog-to-digital converter. A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range.

Note: This quantization procedure introduces inherent errors of one-half LSB (least significant bit) in the representation since, within this fractional range, only one analog value can be represented free of error by a single digital output code.

AMI

Alternate Mark Inversion. A pseudoternary signal converting binary digits, in which successive "marks" are normally of alternate positive and negative polarity but equal in amplitude and in which "space" is of zero amplitude.

Address

The number dialed by a calling party that identifies the party called. Also a location or destination in a computer program.

ALBO

Automatic Line Build Out. In digital transmission systems, a circuit that monitors the amplitude of the received digital signal and, based on this information, automatically adjusts its gain and frequency response to correct for the effects of the transmission line.

Aliasing

The occurrence of spurious frequencies in the output of a pulse-coded modulation (PCM) system or ADC that were not present in the input due to foldover of higher frequencies.

Bell Tapping

The undesired activation of the ringer circuit of a telephone caused by dial pulses from a parallel telephone. Also known as tinkling.

Bias (Asymmetrical) Distortion

Distortion affecting a binary modulation scheme whereby the actual mark or space has a longer or shorter duration than the corresponding theoretical duration.

Bit Rate (BPS) Versus Baud Rate

For modems using voice grade telephone lines, the bit rate equals the data rate. The baud rate is the actual number of times per second that the transmitted carrier is modulated or changes state.

BORSCHT

An acronym for the function that must be performed in the central office when digital voice transmission occurs; **B**attery, **O**vervoltage, **R**inging, **S**upervision, **C**oding, **H**ybrid, and **T**est.

Byte

A group of bits treated as a unit. Often equivalent to one alphabetic or numeric character.

CCITT

International Telegraph and Telephone Consultative Committee. An international forum for establishing communication system standards.

Central Office (CO)

The switching equipment that provides local-exchange telephone service for a given geographical area and is designated by the first three digits of the telephone number.

Channel

An electronic communication path. In telecommunications, it is usually a voice bandwidth of 4,000 Hz.

Circuit

An interconnected group of electronic devices or, in telecommunications, the path connecting two or more communications terminals.

C-Message Weighting

A noise weighting used to measure noise on a line that would be terminated by a 500-type telephone set or similar instrument. The resulting noise reading is in dBrnC.

Codec

An assembly comprising an encoder and a decoder in the same unit. A device that produces a coded output from an analog input, and vice versa.

Combo

A single-chip pulse-code-modulated encoder, decoder (PCM codec) and PCM line filter.

Common Battery

A system supplying direct current for the telephone set from the central office.

Compander

A contraction for a compressor-expander; a circuit that compresses the dynamic range of an input signal and expands it back to almost the original form at the output.

Crossbar Switch

An electromechanical switching machine using a relay mechanism with horizontal and vertical input lines (usually 10 to 20). Uses a contact matrix to connect any vertical to any horizontal.

Crosspoint

The element that actually performs the switching function in a telephone system. It may be mechanical using metal contacts or solid state using integrated circuits.

Crosstalk

Undesired voice-band energy transfer from one circuit to another (usually adjacent).

Cutoff Frequency

The frequency above or below which signals are attenuated below a specified value by a circuit or network.

DAC

Digital-to-analog converter. A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.
Note: Examples of input code formats are straight binary, two's complement, and binary-coded decimal.

Data

In telephone systems, any information other than human speech.

Data Set

Telecommunications term for a modem.

Decibel (dB)

A unit of measure of relative power, 10 log (P1/P2), or voltage, 20 log (V1/V2), in terms of the ratio of two values.

dBm

Decibels referenced to one milliwatt; used in communication work as a measure of absolute power values. Zero dBm equals one milliwatt.

dBm0

Noise power referenced to or measured at a zero transmission level point (0TLP).

dBm0p

Noise power in dBm0, measured by a psophometer or noise measuring set having psophometric weighting.

dBrn

Decibels above reference noise. Rated noise power in dB referenced to one picowatt. Zero dBrn equals −90 dBm.

dBrnC

Weighted noise power in dBrn, measured by a noise measuring set with C-message weighting.

dBrnC0

Noise power in dBrnC referenced to or measured at a zero transmission level point (0TLP).

dBW

Decibels referenced to one watt.

Decoder

Any device that modifies transmitted information to a form that can be understood by the receiver.

Demultiplexer

A circuit that distributes an input signal to a selected output line (with more than one output line available).

Dial Pulsing

Transmission of address information by breaking a dc path; the number of breaks corresponds to the decimal digit dialed.

DTMF

Dual-Tone-Multi-Frequency. Use of two simultaneous voice-band tones for dialing.

EIA

Electronic Industries Association. (2001 Eye Street, N.W., Washington, D.C. 20006)

Electromagnetic Spectrum

The total range of wavelengths or frequencies of electromagnetic radiation, extending from the longest radio waves to the shortest known cosmic rays.

Encoder

Any device that modifies information into the desired pattern or form for a specific method of transmission.

ESS

Electronic Switching System. A telephone switching machine using electronics, often combined with electromechanical crosspoints, and usually with a stored-program computer as the control element.

Exchange Area

The territory within which telephone service is provided for a basic charge. Also called the local calling area.

Equalization

The reduction of frequency distortion and/or phase distortion of a circuit by the introduction of networks to compensate for the difference in attenuation, time delay, or both, at the various frequencies in the transmission band.

FCC

Federal Communications Commission. A government agency that regulates and monitors the domestic use of the electromagnetic spectrum for communications.

FCC Part 68

A government document describing the types of equipment that must be registered and the electrical and mechanical standards to be met when connecting equipment to the public telephone network.

Fiber Optics

The process of transmitting infrared and visible light frequencies through a low-loss glass fiber with a transmitting laser or LED.

FSK

Frequency-Shift Keying. A method of transmitting digital information that utilizes two tones; one representing a high level, the other a low level.

Full Duplex

Simultaneous communication in both directions between two points.

Ground Start

A method of signaling between two machines in which one machine grounds one side of the line and the other machine detects the presence of the ground.

HDB3

High-Density Bipolar Three-line code. See AMI.

Half-Duplex

A circuit that can carry information in both directions but not simultaneously.

Hybrid

In telecommunications, a circuit that divides a signal transmission channel into two channels (i.e., one for each direction) or, conversely, combines two channels into one.

Instruction Code

Digital information that represents an instruction to be performed by a computer.

ISDN

Integrated Services Digital Network. A communication network capable of carrying digitized voice and data multiplexed onto the public network.

Lineside

Refers to the portion of the central office that connects to the local loop.

Local Loop

The voice-band channel connecting the subscriber to the central office.

Longitudinal Balance

A measure of symmetry impedance of a balanced network. Improper longitudinal balance results in poor common-mode rejection.

Loop Current

Flow of dc in the local loop. Indicates that a telephone is in use.

Loss

Attenuation of a signal due to any cause.

Mark

One of the two possible states of a binary information element. The closed circuit and idle state in a teleprinter circuit. See Space.

MTS

Message Telephone Service. The official name for long distance or toll service.

Modem

A device to convert digital data into an analog signal and vice versa so that two electronic devices (e.g., a computer and a data terminal) may communicate over the telephone system. The word modem is a contraction of modulator/demodulator.

Multiplexer

A device for accomplishing simultaneous transmission of two or more signals over a common transmission medium.

Off-Hook

The condition that indicates the active state of a telephone circuit. The opposite condition is On-Hook.

PABX

Private Automated Branch Exchange. Small local automatic telephone office serving extensions in a business complex providing access to the public network.

Parallel Data

The transfer of data simultaneously over two or more wires or transmission links.

Parity

A bit that indicates whether the number of "ones" in a bit string is odd or even.

PBX

Private Branch Exchange. A telephone exchange serving an individual organization and having connection to a public telephone exchange.

Period

The time between successive similar points of a repetitive signal.

Phase

The time or angle that a signal is delayed with respect to some reference position.

POTS

Plain Old Telephone Service. An acronym used by the telephone industry for conventional telephone service.

PSK

Phase Shift-Keyed modulation. A method of placing data of a carrier signal by modifying the phase of the carrier wave.

Psophometric Weighting

A noise weighting recommended by the CCITT for use in a noise measuring set or psophometer.

PCM

Pulse-Coded Modulation. That form of modulation in which the modulating signal is sampled and then quantized and coded, so that each element of information is represented in digital form by a serial bit stream.

Quantizing Noise

An undesirable random signal caused by the error of approximation in a quantizing process. It may be regarded as noise arising in the pulse-code modulation process due to the code-derived facsimile not exactly matching the waveform of the original message.

Register

A storage element for one or more bits of digital information.

Ring

The alerting signal to the subscriber or terminal equipment. Also, the name for one conductor of the wire pair comprising the local loop, designated by R.

Ring Trip

During ring signaling, the detection of the off-hook condition and removal of the ring signal from the line by the switch.

Serial Data

The transfer of data over a single wire in a sequential pattern.

Sidetone

That portion of the speaker's voice that is fed back to his receiver.

Simplex

A circuit that can carry information in only one direction (e.g., broadcasting.)

SLCC

Subscriber Line Control Circuits. A family of CMOS LSI circuits which provide the hybrid, supervisor and controlling functions in a single package.

SLIC

Subscriber Line Interface Circuit. In digital transmission of voice, the circuit that performs some or all of the interface functions at the central office. See BORSCHT.

Space

One of the two possible states of a binary information element. The open-circuit or no-current state of a teleprinter.

State

A condition of an electronic device, especially a computer, that is maintained until an internal or external occurrence causes change.

S by S

Step-by-Step system. An electromechanical telephone switching system in which the switches are controlled directly by digits dialed by the calling party.

Subscriber Loop

See Local Loop.

Supervision

The function of monitoring and controlling the status of a call.

TDM

Time Division Multiplexing. A communication system technique that separates information from channel inputs and places them on a carrier in specific positions of time.

Tip

One conductor of the wire pair composing the local loop and designated by T. Usually the more positive of the two conductors.

Toll Center

A major telephone distribution center that distributes calls from one major metropolitan area to another.

Transhybrid Loss

In a telphone hybrid, the measure of the isolation between the receive and transmit ports. It is also a measure of the balance between the two matched windings of a hybrid transformer.

Transmission Link

The path over which information flows from sender to receiver.

Trunk

A transmission channel connecting two switching machines.

Trunkside

That portion of the central office that connects to trunks going to other switching offices.

Voice-Grade Line

A local loop, or trunk, having a bandpass of approximately 300 to 3,000 Hz.

Wideband Circuit

A transmission facility having a bandwidth greater than that of a voice-grade line.

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ATTENTION

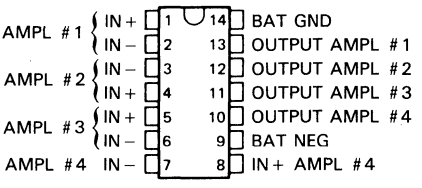
These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields, however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

D2758, MARCH 1986

- Designed for −52-V Battery Operation
- 50-mA Output Current Capability
- Input Compatible with TTL and CMOS
- High Common-Mode Input Voltage Range
- Very Low Input Current
- Fail-Safe Disconnect Feature
- Built-In Output Clamp Diode
- Direct Replacement for National DS3680 and Fairchild μA3680

D, J OR N PACKAGE
(TOP VIEW)

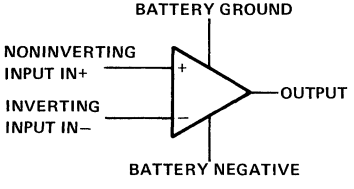


description

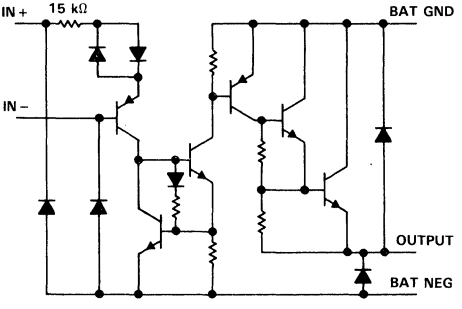
The DS3680 telephone relay driver is a monolithic integrated circuit designed to interface −48-volt relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 milliamperes from standard −52-volt battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ±20 volts referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output will be "off" as a fail-safe condition when either output is open.

The DS3680 is characterized for operation from −25°C to 85°C.

symbol (each driver)



schematic diagram (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range at BAT NEG, V_{B-} . . . . . −70 V to 0.5 V
Input voltage with respect to BAT GND . . . . . −70 V to 20 V
Input voltage with respect to BAT NEG . . . . . −0.5 V to 70 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±20 V
Output current: resistive load . . . . . −100 mA
inductive load . . . . . −50 mA
Inductive output load . . . . . 5 H
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
D package . . . . . 900 mW
J package . . . . . 1025 mW
N package . . . . . 1650 mW
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
N package . . . . . 260°C

NOTES: 1. All voltages are with respect to the BAT GND terminal, unless otherwise specified.
2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN−.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 7.2 mW/°C for the D package, 8.2 mW/°C for the J package, and 13.2 mW/°C for the N package.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{B-}	−10	−60	V
Input voltage, either input	−20†	20	V
High-level differential input voltage, V_{IDH}	2	20	V
Low-level differential input voltage, V_{IDL}	−20†	0.8	V
Operating free-air temperature, T_A	−25	85	°C

†The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{B-} = −52 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current (into IN+)	V_{ID} = 2 V			40	100	μA
		V_{ID} = 7 V			375	1000	
I_{IL}	Low-level input current (into IN+)	V_{ID} = 0.4 V			0.01	5	μA
		V_{ID} = −7 V			−1	−100	
$V_{O(on)}$	On-state output voltage	I_O = 50 mA,	V_{ID} = 2 V		−1.6	−2.1	V
$I_{O(off)}$	Off-state output current	V_O = V_{B-}	V_{ID} = 0.8 V		−2	−100	μA
			Inputs open		−2	−100	
I_R	Clamp diode reverse current	V_O = 0			2	100	μA
V_{OK}	Output clamp voltage	I_O = 50 mA			0.9	1.2	V
		I_O = −50 mA,	V_{B-} = 0		−0.9	−1.2	
$I_{B(on)}$	On-state battery current	All drivers on			−2	−4.4	mA
$I_{B(off)}$	Off-state battery current	All drivers off			−1	−100	μA

‡All typical values are at T_A = 25°C.

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switching characteristics V_{B-} = −52 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_{ID} = 3-V pulse, R_L = 1 kΩ,		1	10	μs
t_{off}	Turn-off time	L = 1 H, See Figure 1		1	10	μs

PARAMETER MEASUREMENT INFORMATION

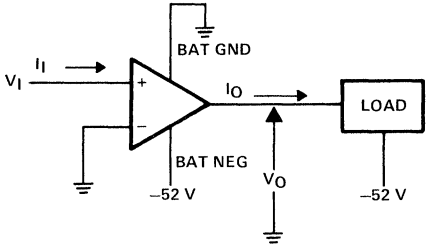
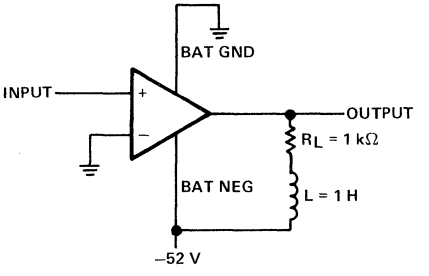
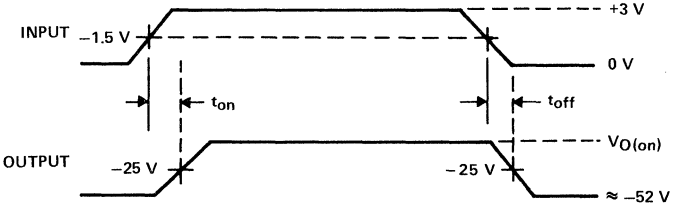


FIGURE 1. GENERALIZED TEST CIRCUIT, EACH DRIVER



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2. SWITCHING CHARACTERISTICS, EACH DRIVER

TYPICAL APPLICATION DATA

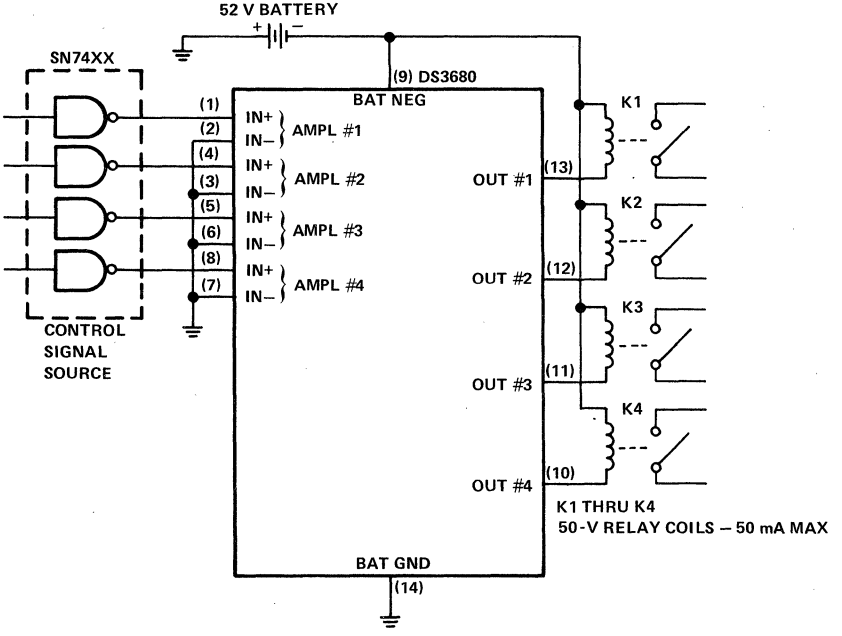


FIGURE 3. RELAY DRIVER

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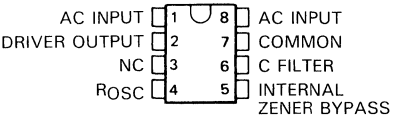
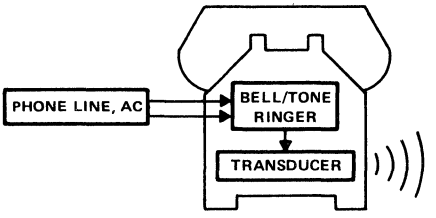
D2763, SEPTEMBER 1983—REVISED MARCH 1986

- **Electronic Replacement for Electromechanical Telephone Bell When Used with Transducer**
- **Designed to Meet or Exceed FCC Part 68 Class B Ringer Requirements**
- **Low-Cost External Component Requirements**
- **Low External Component Count**
- **High Standby Input Impedance . . . 1 MΩ Typ**
- **Low Ringer Equivalency Number . . . < 1 Typ**
- **Single-Ended High-Voltage Output Compatible with Piezo Transducer or Transformer-Coupled Speaker**
- **Reliable BIDFET† Process Technology Provides Efficient High-Voltage Operation**
- **On-Chip High-Voltage Full-Wave Diode Bridge Rectifier and Output Voltage Regulator**
- **On-Chip Circuitry Provides Ring Rejection of Rotary Dial Transients, Lightning, and Induced High-Voltage Transients**
- **Improved Direct Replacements for TCM1501, TCM1506, and TCM1512**

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection



TYPICAL CHARACTERISTICS
TELEPHONE TONE RINGER DRIVER FAMILY

PART NO.	NOMINAL OUTPUT CENTER FREQUENCY (Hz)	WARBLE RATIO (f_H:f_L)	NOMINAL WARBLE FREQ. (Hz)
TCM1501A	2000	8:7	7.8
TCM1506A	500	5:4	7.8
TCM1512A	1250	8:7	9.8

description

The TCM1501A, TCM1506A, and TCM1512A are monolithic integrated circuit telephone tone ringer drivers that, when coupled with an appropriate transducer, replace the electromechanical bell. These devices are designed, using BIDFET† technology, for use with either a Piezo transducer or an inexpensive transformer-coupled speaker to produce a pleasing tone composed of a high frequency (f_H) alternating with a low frequency (f_L) resulting in a warble frequency. Each device is powered and activated by the telephone line ring voltage, which may vary from 40 volts to 150 volts rms at frequencies from 15.3 hertz to 68 hertz.

During low voltage (off-hook) standby, typical input impedance is greater than 1 megohm; this prevents interference with telephone DTMF or voice signals without the use of expensive mechanical switches. This high standby impedance is achieved with an on-chip series zener diode that is activated by a differential input voltage of typically 8.9 volts at pins 1 and 8. A voltage level of typically 17 volts differential at pins 1 and 8 deactivates the internal zener diode, allowing for more efficient power transfer to the load when the device is in the operating mode. During ringing, the impedance of the applied circuit (see Figures 4 and 5) varies from 30 kilohms to 8 kilohms over the Class B ring signal, and is reasonably independent of the output load.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

†BIDFET — Bipolar, double-diffused, N-channel and P-channel, MOS transistors on the same chip—patented process.

TEXAS INSTRUMENTS
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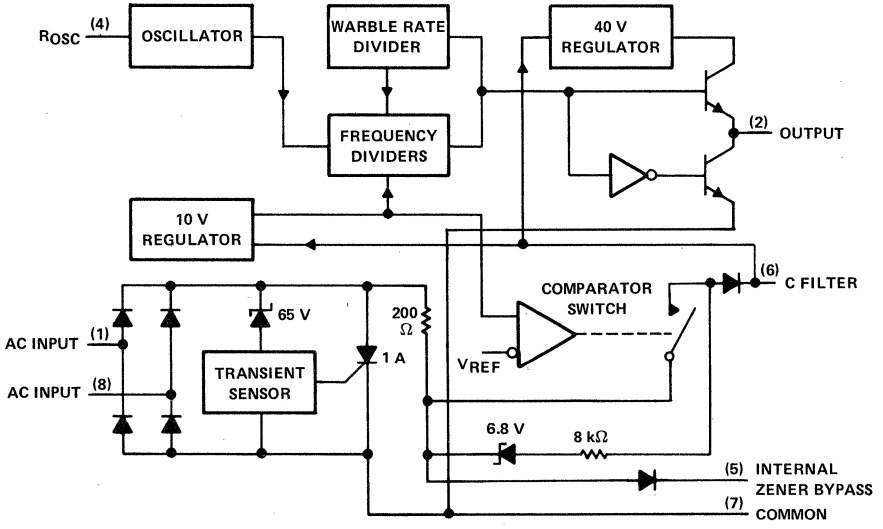
description (continued)

When used with the proper external circuitry (see Figures 4 and 5), these devices feature lightning and transient protection circuitry designed to withstand lightning strikes of 1.5 kilovolts for up to 200 microseconds duration. In addition, internal circuitry will reject dial pulses from parallel telephones so that false ringing (tapping) will not occur.

These telephone tone ringer drivers may be used in nontelephone communications applications. For example, the devices can be used, with few external components, to produce an inexpensive and highly efficient alarm (see Figure 6).

functional block diagram



absolute maximum ratings

Continuous peak-to-peak input voltage, pin 1 to pin 8 (see Note 1)	65 V
Continuous dc input voltage at pin 6	65 V
Continuous output current, I_O, at pin 2	12 mA
Continuous output current, pin 5 and pin 6	30 mA
Continuous SCR on-state input current, pin 1 to pin 8	200 mA
SCR on-state input current, pin 1 to pin 8 (duration ≤200 μs)	900 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000 mW
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−40°C to 125°C

NOTES: 1. For applications requiring ≥ 45 Vrms, an external resistor and capacitor are required to prevent damage to the device (see Note 3). Tip and ring may be connected interchangeably to either pin 1 or pin 8.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 8 mW/°C.

recommended operating conditions

		MIN	MAX	UNIT
RMS input voltage, V_I (f = 15.3 Hz to 68 Hz) (see Note 3)		40	150	V
Output frequency (MIN applies to f_L, MAX applies to f_H)	TCM1501A	1700	2500	Hz
	TCM1506A	425	575	
	TCM1512A	1062	1438	
Operating free-air temperature, T_A		−20	70	°C

NOTE 3: Input voltage is applied to pins 1 and 8 through a series 2.2 kΩ ±10% resistor and a 0.47 μF ±10% capacitor (see Figures 4 and 5).

electrical characteristics at 25°C free-air temperature, R_L = open, $C_{(fltr)}$ = 10 μF, f = 20 Hz (unless otherwise noted), see Figure 2

detector section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ringing start threshold voltage	Pin 5 open, R_L = 4 kΩ		19	28	V
Ringing start threshold rms voltage	Pin 5 open, R_L = 4 kΩ, f = 15.3 Hz			40	V
Ringing stop threshold voltage	Pin 5 open, R_L = 4 kΩ	7	11		V
Standby input impedance	V_i = 3 V, f ≤ 20 kHz	0.1	1		MΩ
	V_i = 3 V, f ≤ 20 kHz (see Note 5)		10		kΩ
Impedance when ringing	V_i = 40 V, R_L = 4 kΩ, f = 15.3 Hz		25		kΩ
	V_i = 130 V, R_L = 4 kΩ		22		
Operating current	Pin 2 open, V_I = 40 V			1.1	mA
	Pin 2 open, V_I = 55 V			4	
Low level input current	V_I = 5 V			20	μA
SCR trigger voltage (pin 1 to pin 8)	All pins open, I_I ≤ 125 mA (see Note 4)	65	75	100	V
SCR trigger current (pin 1 to pin 8)	All pins open, V_I ≤ 100 V (see Note 4)	55	90	110	mA
SCR input hold current	(see Note 4)			100	μA

NOTES: 4. These parameters are measured using pulse techniques (t_W ≤ 200 μs, duty cycle ≤ 5%).
5. Pin 5 connected to pin 6, and pin 6 connected to pin 7 through a 100 Ω resistor.

electrical characteristics at 25°C free-air temperature, $C_{(fltr)}$ = 10 μF, f = 20 Hz (unless otherwise noted), see Figure 2

output section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage, pin 2	V_I = 17 V, I_O = 2 mA, See Note 6	6			V
	V_I = 65 V, I_O = 5 mA, See Note 6	36	40		
	V_i = 40 V, f = 16 Hz, I_O = 2 mA	8			
	V_i = 150 V, f = 15.3 Hz, I_O = 2 mA,	22	30		
Output voltage, pin 6 (see Note 7)	V_i = 150 V, f = 15.3 to 68 Hz			100	V
High-level output current	V_I = 65 V, V_O = 36 V, See Note 6	−5	−10		mA
Low-level output current	V_I = 65 V, V_O = 5 V, See Note 6	5	6		mA

NOTES: 6. Devices must be forced to the required output state by taking pin 4 to 10 V and toggling to 0 V as required. This stops the on-chip oscillator.

7. Normal device operation requires that a capacitor be connected from pin 6 to common (pin 7). A 10 μF capacitor is recommended for optimum antitapping vs turn-off-time performance of the circuit. Increasing or decreasing the value of this capacitor will respectively increase or decrease the antitapping capabilities of the circuit.

oscillator section

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output tone frequency High tone frequency/Low tone frequency	See Note 8	TCM1501A		2142/1874		Hz
		TCM1506A		562/450		
		TCM1512A		1339/1172		
Warble frequency	See Note 8	TCM1501A	7.41	7.8	8.3	Hz
		TCM1506A	7.41	7.8	8.3	
		TCM1512A	9.3	9.8	10.4	
Temperature coefficient of frequency	T_A = −20°C to 70°C			±0.05		%/°C

NOTE 8: Normal device operation requires that a resistor (± 1%) be connected from pin 4 to common (pin 7). Texas Instruments separates the devices during final test to match one of the resistor values listed in Table 1 below. Each device is then symbolized, as shown in Figure 1, with the appropriate recommended resistor value of R_{OSC} required to guarantee specified output frequencies. For oscillator stability, it is recommended that R_{OSC} be located on the printed-circuit board as close as possible to pin 4 of the integrated circuit and be surrounded by the ground plane.

TABLE I. STANDARD RESISTOR VALUES
(See Note 8)

DEVICE NO.	RESISTOR VALUES (kΩ)				
TCM1501A	130	140	150	158	165
TCM1506A	130	140	150	158	165
TCM1512A	130	140	150	158	165

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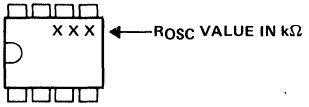

FIGURE 1. TELEPHONE TONE RINGER DRIVER SYMBOLIZATION

PARAMETER MEASUREMENT INFORMATION

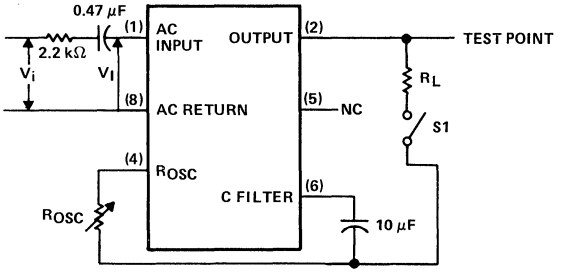

FIGURE 2. TEST CIRCUIT

TYPICAL CHARACTERISTICS

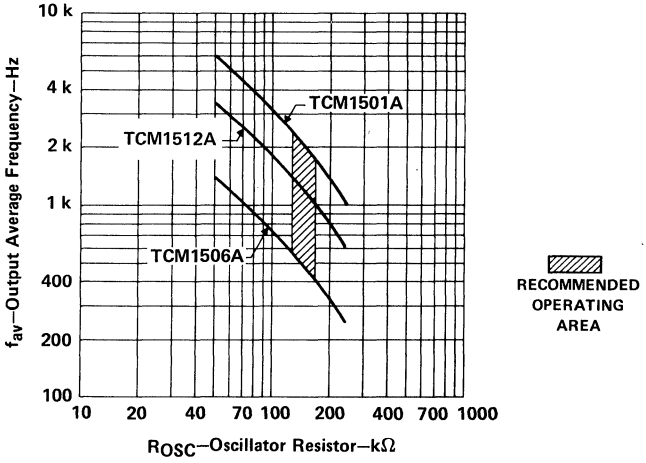

FIGURE 3. OSCILLATOR RESISTOR vs OUTPUT AVERAGE FREQUENCY

TYPICAL APPLICATIONS

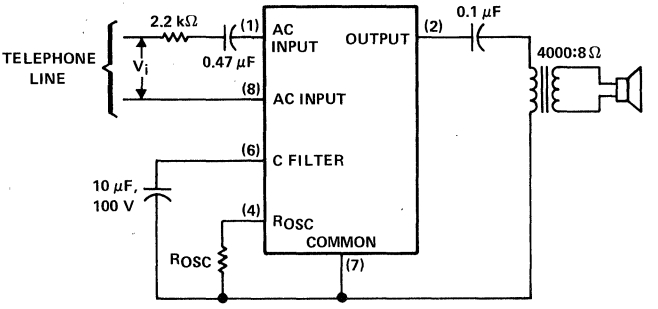

FIGURE 4. TELEPHONE APPLICATION—SPEAKER DRIVE

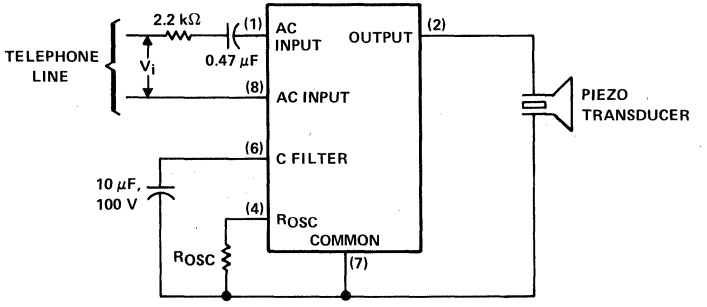

FIGURE 5. TELEPHONE APPLICATION—PIEZO DRIVE

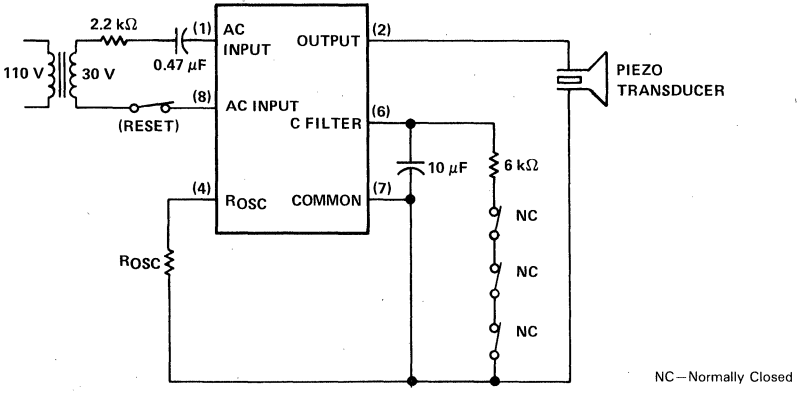

FIGURE 6. ALARM SYSTEM CONFIGURATION

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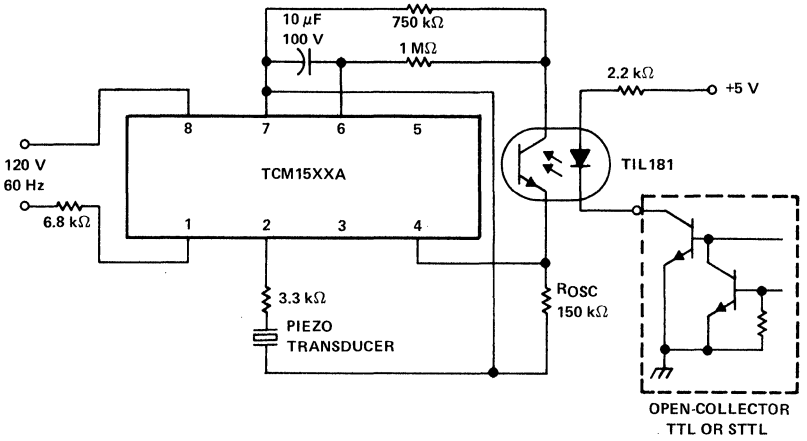


FIGURE 7. NONTELEPHONE APPLICATION

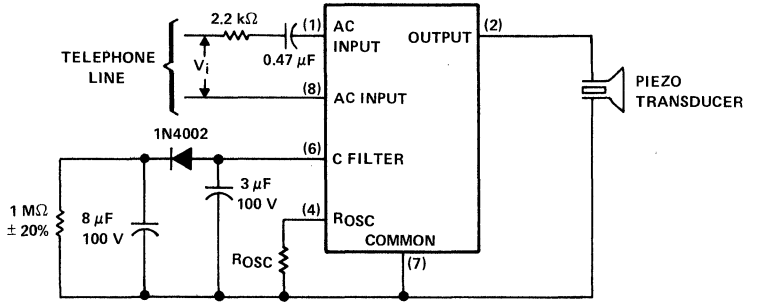
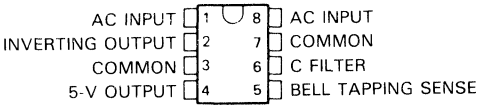


FIGURE 8. TELEPHONE APPLICATION—PIEZO DRIVE FAST RING SIGNAL CUTOFF

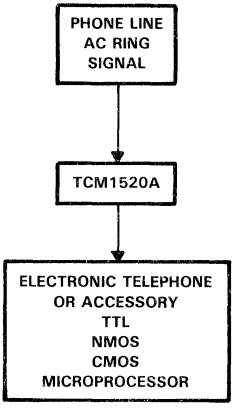
D2860, OCTOBER 1984

- **On-Chip 150-V Bridge Diode Configuration**
- **Reliable BIDFET† Technology**
- **High Standby Impedance . . . 1 MΩ Typ**
- **Efficient High-Voltage Operation**
- **Output Compatible with TTL, NMOS, and CMOS**
- **Built-In 5-V Series Regulator**
- **Built-In Lightning and Transient Protection**

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM1520A APPLICATION



description

The TCM1520A is a monolithic ring detection integrated circuit designed for use in isolated or nonisolated telephone applications. The device uses a modified form of the Texas Instruments BIDFET† technology to combine low-voltage CMOS and high-voltage bipolar input/output circuitry. It features efficient high-voltage (40 volts to 150 volts) operation with a maximum of 1 milliampere of current drain.

During standby, the input impedance is approximately 1 megohm or greater, which will prevent any interference with parallel "off-hook" telephones transmitting DTMF or voice frequencies. The device achieves such a high input impedance with an on-chip series zener diode that does not conduct until the voltage across Pins 1 and 8 exceeds 8 volts. When the voltage across Pins 1 and 8 exceeds 17 volts the internal switch is closed, which bypasses the 6.8-volt zener diode and series resistor. This allows more efficient power transfer to the load when the device is in the operating mode. In the operating mode, the impedance of the device varies from 30 kilohms to 7 kilohms over the ring signal of 40 volts at 16 hertz to 150 volts at 68 hertz and is reasonably independent of the output load.

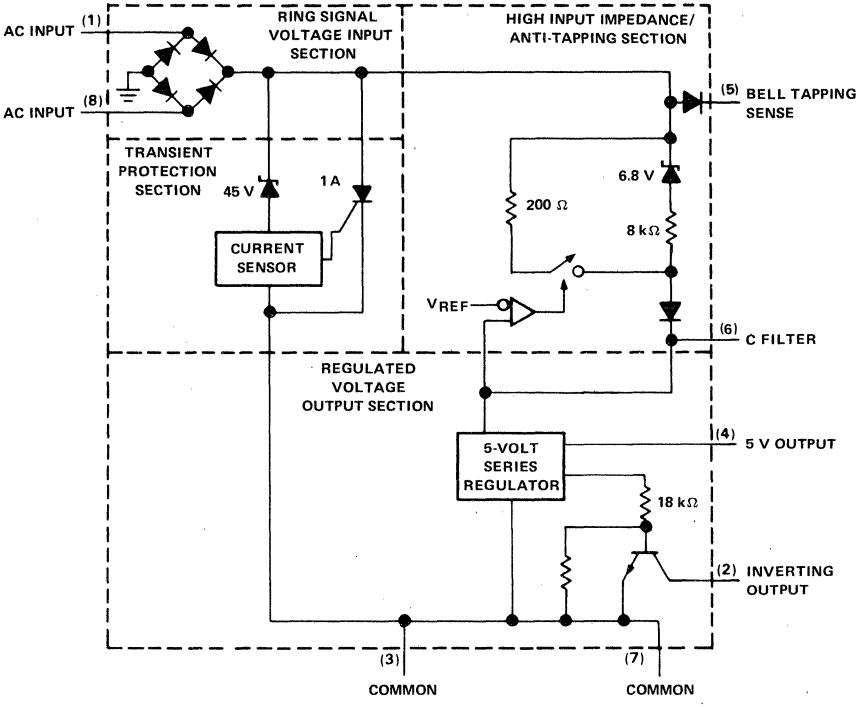
In typical telephone applications, the TCM1520A is activated through the telephone line by a ring voltage of 40 volts at 16 hertz to 150 volts at 68 hertz. The TCM1520A generates a signal suitable to drive an optocoupler or TTL, NMOS, or CMOS logic. The +5 V Output (pin 4) may be used as a supply source for optocouplers or low-power logic. This output is noninverting and will be at a high-level during ringing.

The TCM1520A incorporates lightning and transient protection that is designed to suppress lightning strikes of 1.5-kilovolt amplitude and 200-microsecond duration. The TCM1520A also features built-in circuitry to avoid tapping or false triggering due to transients.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

‡BIDFET — Bipolar, Double-Diffused, N-channel and P-channel MOS transistors on the same chip — patented process.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Continuous supply voltage at pin 6 (see Note 1)	40 V
Continuous differential input voltage, V_{ID} (Pins 1 and 8)	40 V
Continuous output current, I_O	12 mA
Continuous SCR on-state input current (see Note 2)	200 mA
SCR on-state input current, $I_{I(on)}$ (duration $\leq 200\ \mu s$) (see Note 2)	900 mA
Continuous total dissipation at (or below) 25°C free-air temperature: (see Note 3)	
P Package	1000 mW
Operating free-air temperature range	−20°C to 70°C
Storage temperature range	−40°C to 125°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to pin 7.
2. SCR on-state input current is the current at the input when the SCR turns on.
3. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
P	1 W	8 mW/°C	25°C

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recommended operating conditions

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	40			V
Low-level input voltage, V_{IL}			5	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at 25 °C operating free-air temperature, R_L = open, $C_{(fltr)}$ = 10 μF (unless otherwise noted)

detector section

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{(BR)CEX}$	Collector-emitter output breakdown voltage, Pin 2	$V_i \leq 5$ V (rms),	I_O = 5 μA	45			V
V_{OL}	Low-level output voltage, Pin 2	V_i = 25 V (rms),	I_O = 1.6 mA			1	V
V_{T+}	Positive-going threshold voltage				17	25	V
V_{T-}	Negative-going threshold voltage				11		V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)				6		V
$Z_{I(off)}$	Standby input impedance	V_i = 3 V,	f ≤ 20 kHz	0.1	5		MΩ
Z_{ring}	Impedance when ringing	V_{id} = 40 V,	f = 16 Hz		30		kΩ
		V_{id} = 130 V,	f = 20 Hz		20		kΩ
$I_{I(on)}$	On-state input current, SCR‡	See Note 4		55		110	mA
$I_{I(hold)}$	Input holding current, SCR	See Note 4		100			μA
V_O	Output voltage, Pin 4	V_i = 40 V to 150 V,	R_L = 10 kΩ	4.5	5	5.5	V
	Shunt voltage	I_I = 10 mA		40		50	V

switching characteristics at 25 °C operating free-air temperature, f = 20 Hz (unless othewise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_I = 40 V			100	ms
$t_{(off)}$	Turn-off time	V_I = 40 V		175		ms
		V_I = 60 V to 150 V		300		

† All characteristics are measured with a 2.2 kΩ resistor connected to pin 1 and a 0.47 μF capacitor connected at pin 1 in series with the input signal, unless otherwise noted.
‡This is the input current required to turn on the SCR.
NOTE 4: These parameters are measured using pulse techniques ($t_w \leq 200$ μs, duty cycle ≤ 5%) with terminal pin 6 grounded.

PARAMETER MEASUREMENT INFORMATION

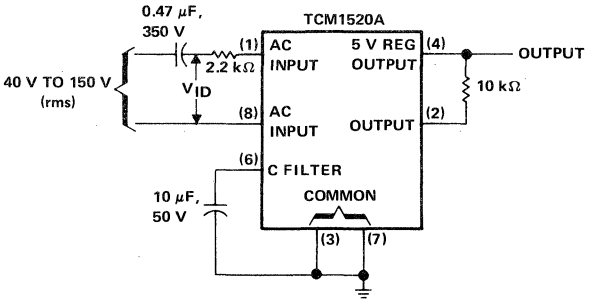

FIGURE 1. SWITCHING TEST CIRCUIT

2 Telecommunications Circuits

TYPICAL CHARACTERISTICS

CAPACITOR VOLTAGE (PIN 6)
vs
DC INPUT VOLTAGE (PINS 1 AND 8)

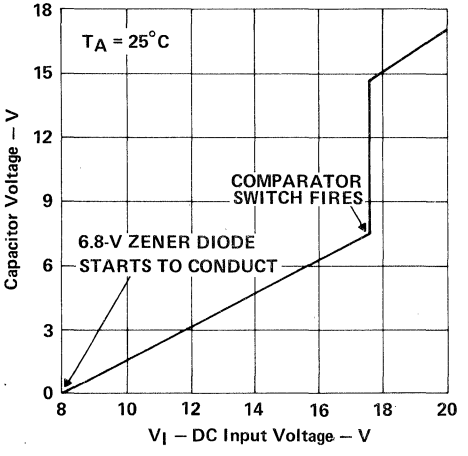

FIGURE 2

OUTPUT VOLTAGE (PIN 4)
vs
CAPACITOR VOLTAGE (PIN 6)

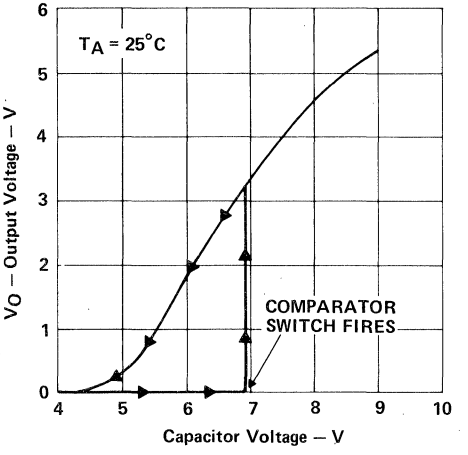

FIGURE 3

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

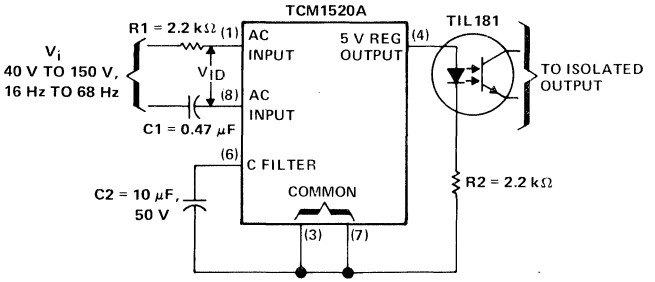


FIGURE 4. ISOLATED CONFIGURATION

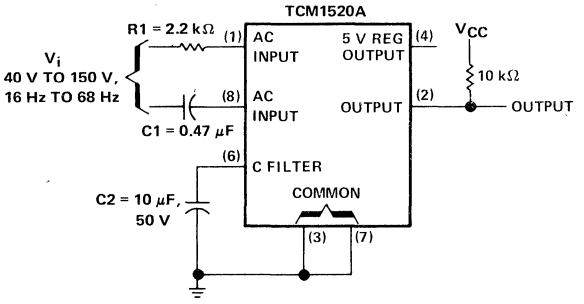


FIGURE 5. NONISOLATED CONFIGURATION

NOTE: See Table 1 for component functions.

TABLE 1. COMPONENT FUNCTIONS

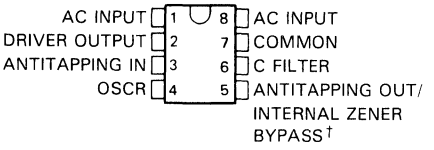
COMPONENT	FUNCTION
R1	Limits current into SCR during high voltage transients and aids in dial pulse rejection.
R2	Limits current into light-emitting diode.
C1	Blocks dc battery voltage in standby and aids in filtering dial pulses. Smaller values of C1 improve tapping immunity.
C2	Stores energy from the ring signal to power the 5-V regulator.
OPTOCOUPLER	Provides ground and transient isolation between the host system and the telephone line.

TCM1531, TCM1532, TCM1536, TCM1539
TCM1531A, TCM1532A, TCM1536A, TCM1539A
TELEPHONE TONE RINGER DRIVERS

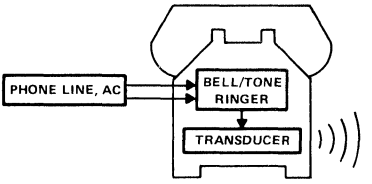
D2940, MARCH 1986

- Electronic Replacement for Electromechanical Telephone Bell When Used with Transducer
- Designed to Meet or Exceed FCC Part 68 Class B Ringer Requirements
- Low-Cost External Component Requirements
- Low External Component Count
- High Standby Input Impedance . . . 1 MΩ Typ
- Low Ringer Equivalency Number . . . < 1 Typ
- Single-Ended High-Voltage Output Compatible with Piezo Transducer or Transformer-Coupled Speaker
- Reliable BIDFET† Process Technology Provides Efficient High-Voltage Operation
- On-Chip High-Voltage Full-Wave Diode Bridge Rectifier and Output Voltage Regulator
- On-Chip Circuitry Provides Ring Rejection of Rotary Dial Transients, Lightning, and Induced High-Voltage Transients
- On-Chip Thyristor Coupled with Additional External Components Provides Enhanced Rejection of Dial Pulses
- TCM1531A, TCM1532A, and TCM1536A are Improved Direct Replacements for TCM1501A, TCM1512A, and TCM1506A, Respectively

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



† Antitapping Output for TCM1531, TCM1532, TCM1536, and TCM1539. Internal Zener Bypass for A-suffix versions.



TYPICAL CHARACTERISTICS
TELEPHONE TONE RINGER DRIVER FAMILY

PART NO.	NOMINAL OUTPUT CENTER FREQUENCY (Hz)	WARBLE RATIO (f_H:f_L)	NOMINAL WARBLE FREQ. (Hz)
TCM1531, TCM1531A	2000	8:7	7.8
TCM1532, TCM1532A	1250	8:7	9.8
TCM1536, TCM1536A	500	5:4	7.8
TCM1539, TCM1539A	2000	5:4	31.2

description

The TCM1531, TCM1532, TCM1536, TCM1539, TCM1531A, TCM1532A, TCM1536A, and TCM1539A are monolithic integrated circuit telephone tone ringer drivers that, when coupled with an appropriate transducer, replace the electromechanical bell. These devices are designed, using BIDFET† technology, for use with either a Piezo transducer or an inexpensive transformer-coupled speaker to produce a pleasing tone composed of a high frequency (f_H) alternating with a low frequency (f_L) resulting in a warble frequency. Each device is powered and activated by the telephone line ring voltage, which may vary from 40 volts to 150 volts rms at frequencies from 15.3 hertz to 68 hertz.

During low voltage (off-hook) standby, typical input impedance is greater than 1 megohm; this prevents interference with telephone DTMF or voice signals without the use of expensive mechanical switches. This high standby impedance is achieved with an on-chip series zener diode that is activated by a differential input voltage of typically 8.9 volts at pins 1 and 8. A voltage level of typically 17 volts differential at pins

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

†BIDFET — Bipolar, double-diffused, N-channel and P-channel, MOS transistors on the same chip—patented process.

description (continued)

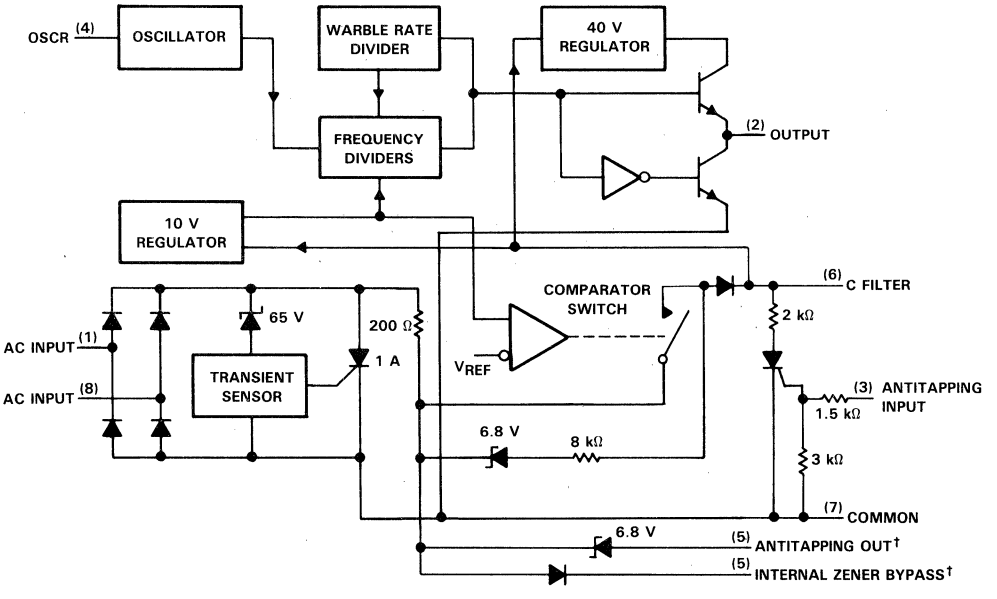
1 and 8 deactivates the internal zener diode, allowing for more efficient power transfer to the load when the device is in the operating mode. During ringing, the impedance of the applied circuit (see Figures 4, 5 and 6) varies from 30 kilohms to 8 kilohms over the Class B ring signal, and is reasonably independent of the output load.

These devices feature lightning and transient protection circuitry designed to withstand transients of 1.5 kilovolt for up to 200 microseconds duration when used with the proper external circuitry (see Figures 4 and 5). In addition, an on-chip thyristor coupled with an external resistor and capacitor circuit will reject dial pulses from parallel telephones so that false ringing (tapping) will not occur (see Typical Application Data).

The TCM1531A, TCM1532A, TCM1536A and TCM1539A have a provision for bypassing the internal series diode with one of lower voltage, thereby lowering the turn-on threshold of the device. If the antitapping thyristor is used with these devices, an external zener diode must be added in series with pin 5.

These telephone tone ringer drivers may be used in nontelephone communications applications. For example, the devices can be used with a few external components to produce an inexpensive and highly efficient alarm (see Figure 6).

functional block diagram



† Antitapping output for TCM1531, TCM1532, TCM1536, and TCM1539. Internal Zener Bypass for A-suffix versions.

TEXAS INSTRUMENTS
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absolute maximum ratings

Continuous peak-to-peak input voltage, pin 1 to pin 8 (see Note 1) . . . . . 110 V
Continuous dc input voltage at pin 6 . . . . . 55 V
Negative dc voltage, any pin . . . . . −1.2 V
Continuous output current, I_O, at pin 2 . . . . . 12 mA
Continuous output current, pin 5 and pin 6 . . . . . 30 mA
Continuous SCR on-state input current, pin 1 to pin 8 . . . . . 200 mA
SCR on-state input current, pin 1 to pin 8 (duration ≤200 μs) . . . . . 900 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1000 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −40°C to 125°C

NOTES: 1. For applications requiring ≥ 38 Vrms, an external resistor and capacitor are required to prevent damage to the device (see Note 3). Tip and ring may be connected interchangeably to either pin 1 or pin 8.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 8 mW/°C.

recommended operating conditions

	MIN	MAX	UNIT
RMS input voltage, V_I (f = 15.3 Hz to 68 Hz) (see Note 3)	40	150	V
Resistor between OSCR and COMMON, R_{OSC}	120	180	kΩ
Operating free-air temperature, T_A	−20	70	°C

NOTE 3: Input voltage is applied to pins 1 and 8 through a series 2.2 kΩ ± 10% resistor and a 0.47 μF ± 10% capacitor (see Figures 4, 5, and 6).

electrical characteristics at 25°C free-air temperature, R_L = open, $C_{(fltr)}$ = 10 μF, f = 20 Hz (unless otherwise noted), see Figure 2

detector section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ringing start threshold voltage	Pin 5 open, R_L = 4 kΩ		19	28	V
Ringing start threshold rms voltage	Pin 5 open, R_L = 4 kΩ, f = 15.3 Hz			40	V
Ringing stop threshold voltage	Pin 5 open, R_L = 4 kΩ	7	11		V
Ringing start threshold voltage	Antitapping thyristor activated		40		V
Pin 3 voltage required to activate antitapping thyristor			1		V
Pin 3 input current required to activate antitapping thyristor			0.2		mA
Standby input impedance	V_i = 3 V, f ≤ 20 kHz	0.1	1		MΩ
	V_i = 3 V, f ≤ 20 kHz (see Note 5)		10		kΩ
Impedance when ringing	V_i = 40 V, R_L = 4 kΩ, f = 15.3 Hz		25		kΩ
	V_i = 130 V, R_L = 4 kΩ		22		
Operating current	Pin 2 open, V_I = 40 V			1.3	mA
Low-level input current	V_I = 5 V			20	μA
SCR trigger voltage (pin 1 to pin 8)	All pins open, I_I ≤ 125 mA (see Note 4)	50	60	100	V
SCR trigger current (pin 1 to pin 8)	All pins open, V_I ≤ 100 V (see Note 4)	55	80	110	mA
SCR input hold current	(see Note 4)		10		mA

NOTES: 4. These parameters are measured using pulse techniques (t_W ≤ 200 μs, duty cycle ≤ 5%).
5. Pin 5 connected to pin 6, and pin 6 connected to pin 7 through a 100 Ω resistor.

electrical characteristics at 25 °C free-air temperature, $C_{(fltr)}$ = 10 μF, f = 20 Hz (unless otherwise noted), see Figure 2

output section

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Output voltage, pin 2	V_I = 17 V,	I_O = 2 mA,	See Note 6		10		V
	V_I = 50 V,	I_O = 5 mA,	See Note 6		44		
	V_i = 40 V,	I_O = 2 mA,	f = 16 Hz		8		
	V_i = 150 V,	I_O = 2 mA,	f = 15.3 Hz		40		
Output voltage, pin 6 (See Note 7)	V_i = 150 V,	f = 15.3 to 68 Hz				55	V
High-level output current	V_I = 50 V,	V_{OH} = 43 V			−15		mA
Low-level output current	V_I = 50 V,	V_{OL} = 1.5 V,	See Note 6		11		mA

NOTES: 6. Devices must be forced to the required output state by taking pin 4 to 8 V and toggling to 0 V as required. This stops the on-chip oscillator.

7. Normal device operation requires that a capacitor be connected from pin 6 to common (pin 7). A 10 μF capacitor is recommended for optimum antitapping vs turn-off-time performance of the circuit. Increasing or decreasing the value of this capacitor will respectively increase or decrease the antitapping capabilities of the circuit.

oscillator section

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output tone frequency High tone frequency/ Low tone frequency	R_{osc} = 150 kΩ ± 1%	TCM1531, TCM1531A	1983/1736	2133/1867	2283/1998	Hz
		TCM1532, TCM1532A	1239/1085	1333/1167	1427/1249	
		TCM1536, TCM1536A	516/414	555.5/445.5	595/477	
		TCM1539, TCM1539A	2066/1653	2222/1778	2378/1903	
Warble frequency	R_{osc} = 150 kΩ ± 1%	TCM1531, TCM1531A		7.8		Hz
		TCM1532, TCM1532A		9.8		
		TCM1536, TCM1536A		7.8		
		TCM1539, TCM1539A		31.2		
Temperature coefficient of frequency	T_A = −20 °C to 70 °C			±0.05		%/°C

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PARAMETER MEASUREMENT INFORMATION

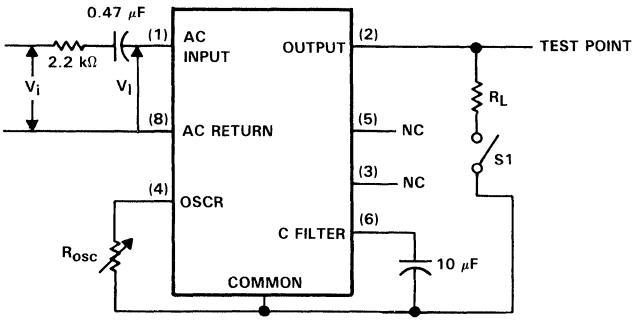


FIGURE 1. TEST CIRCUIT

TYPICAL CHARACTERISTICS

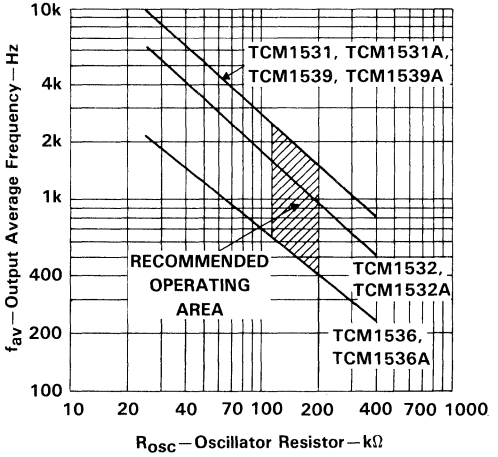


FIGURE 2. OSCILLATOR RESISTOR vs OUTPUT AVERAGE FREQUENCY

TYPICAL APPLICATIONS

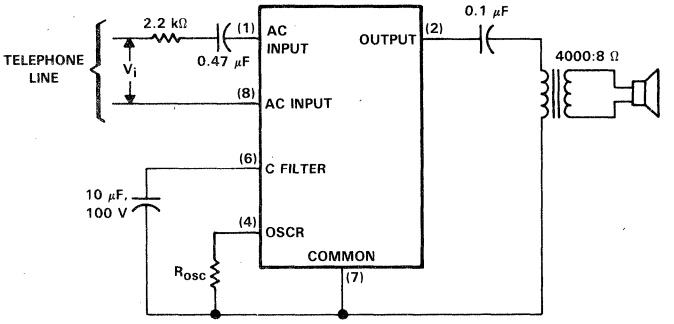


FIGURE 3. TELEPHONE APPLICATION—SPEAKER DRIVE

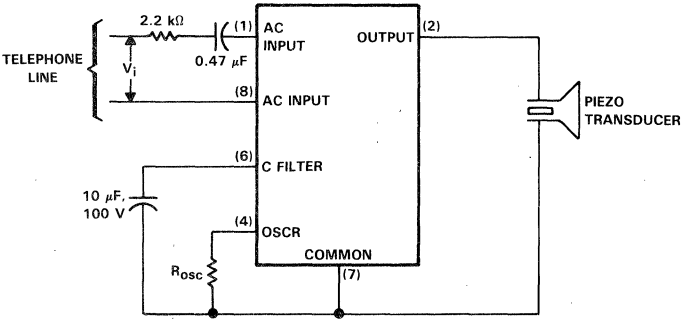
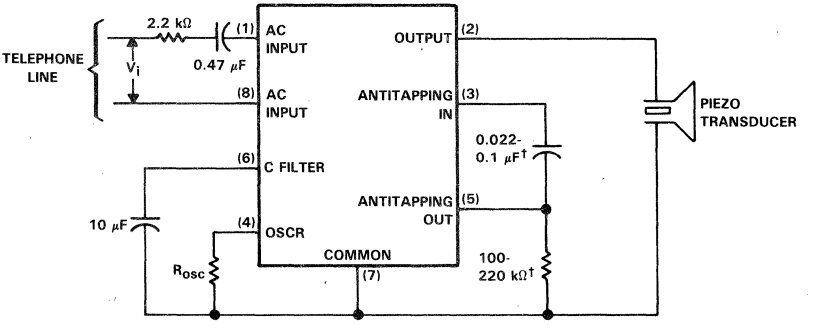


FIGURE 4. TELEPHONE APPLICATION—PIEZO DRIVE



† Optimum values to be determined by specific antitapping requirements.

FIGURE 5. TELEPHONE APPLICATION, IMPROVED ANTITAPPING CIRCUIT

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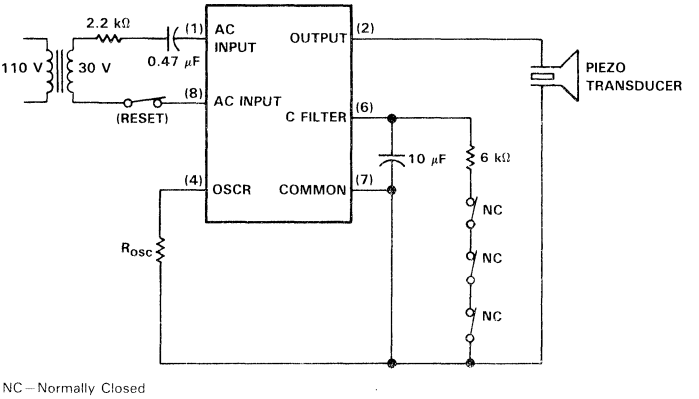
TYPICAL APPLICATIONS



NC—Normally Closed

FIGURE 6. ALARM SYSTEM CONFIGURATION

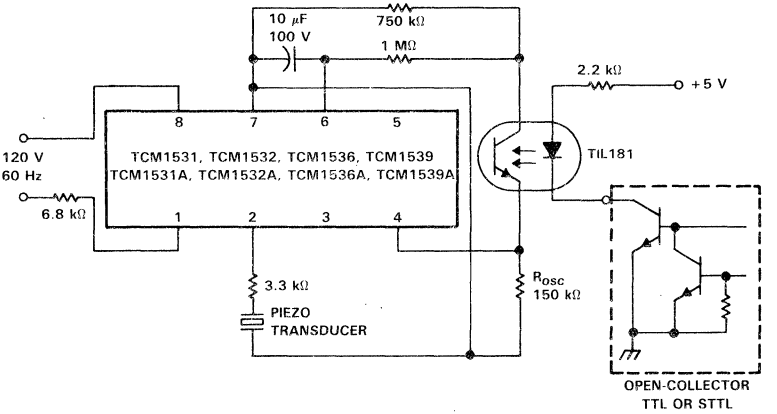


FIGURE 7. NONTELEPHONE APPLICATION

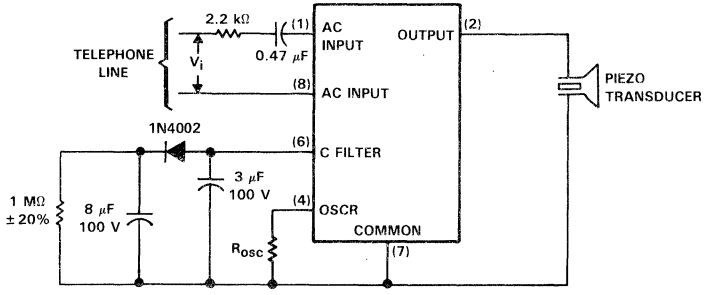


FIGURE 8. TELEPHONE APPLICATION—PIEZO DRIVE FAST RING SIGNAL CUTOFF

TCM2202, TCM2222
AMI/HDB3 ENCODERS/DECODERS

D2894, OCTOBER 1985—REVISED APRIL 1986

- **AMI or HBD3 Encoding of Binary Data**
- **Simultaneous Decoding of Received AMI or HDB3 Signal**
- **Static Logic Allows Zero to 3-MHz Bit Rate**
- **Seven Outputs for Received-Signal Diagnostics**
- **Optional CPU Interface (TCM2202 only)**
- **Reliable NMOS Technology**
- **Single 5-V Supply**

description

The TCM2202 and TCM2222 perform three functions: encoding, decoding, and signal monitoring.

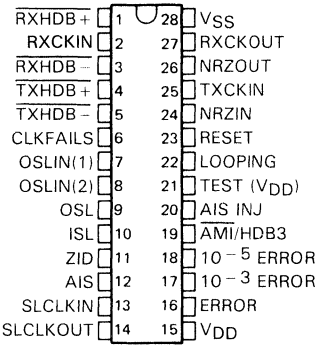
In the encoding section, a binary non-return-to-zero (NRZ) signal is converted to a ternary signal to improve its transmission characteristics. In the decoding section, a received ternary signal is independently converted into a binary form. In the signal-monitoring section, the received ternary signal in the decoder is checked for various diagnostics, and errors that are found are flagged.

The TCM2202 or TCM2222 can be directly connected to the TCM2203 line interface device to form a complete equipment transmission interface.

The TCM2202 and TCM2222 are characterized for operation from 0°C to 70°C.

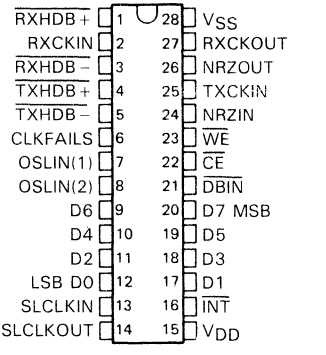
TCM2202 . . . J PACKAGE
(TOP VIEW)

TCM2202 PIN NAMES WITHOUT CPU INTERFACE

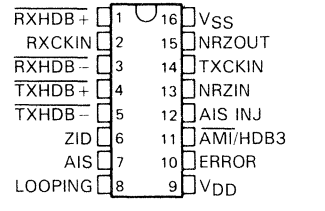


TCM2202 . . . J PACKAGE
(TOP VIEW)

TCM2202 PIN NAMES WITH CPU INTERFACE



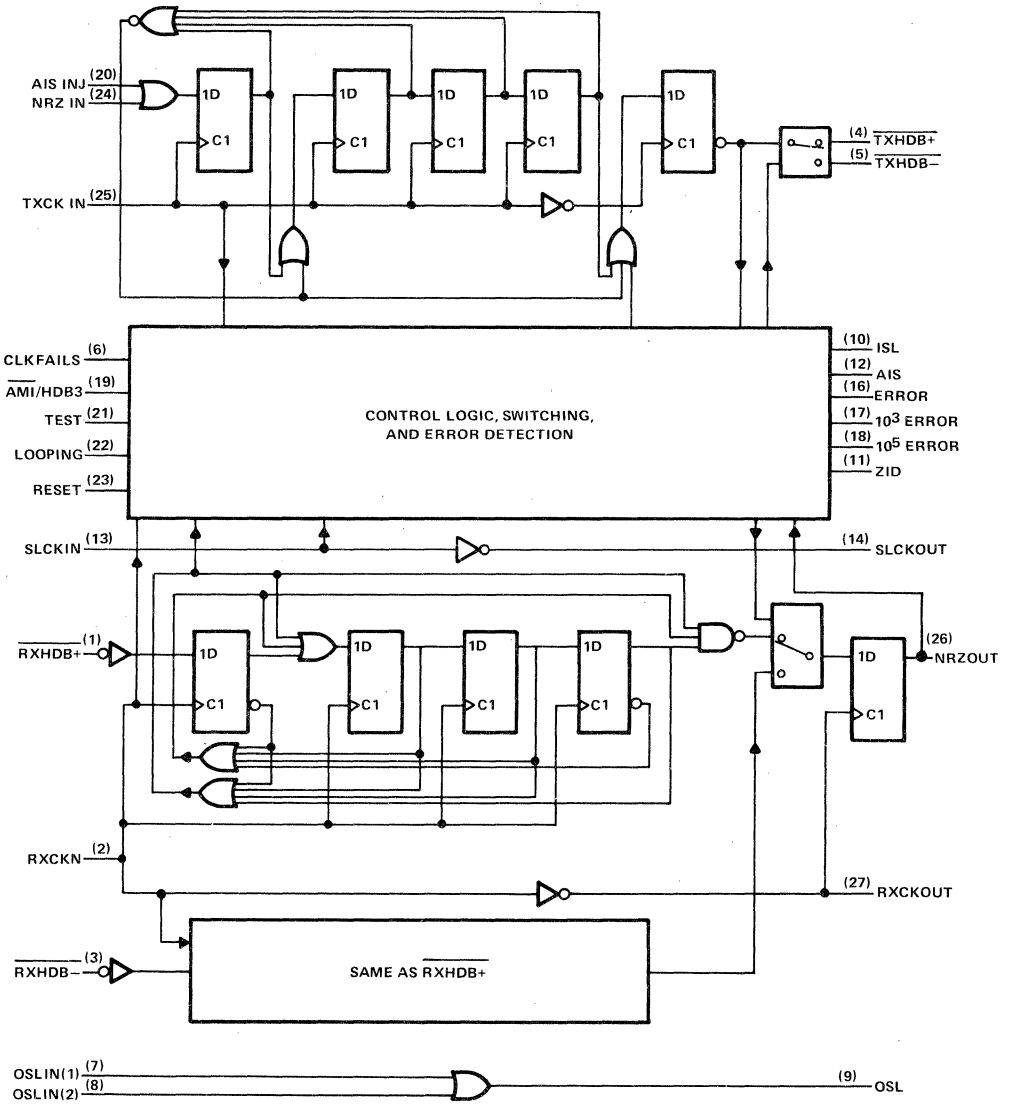
TCM2222 . . . J PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

functional block diagram

TCM2202



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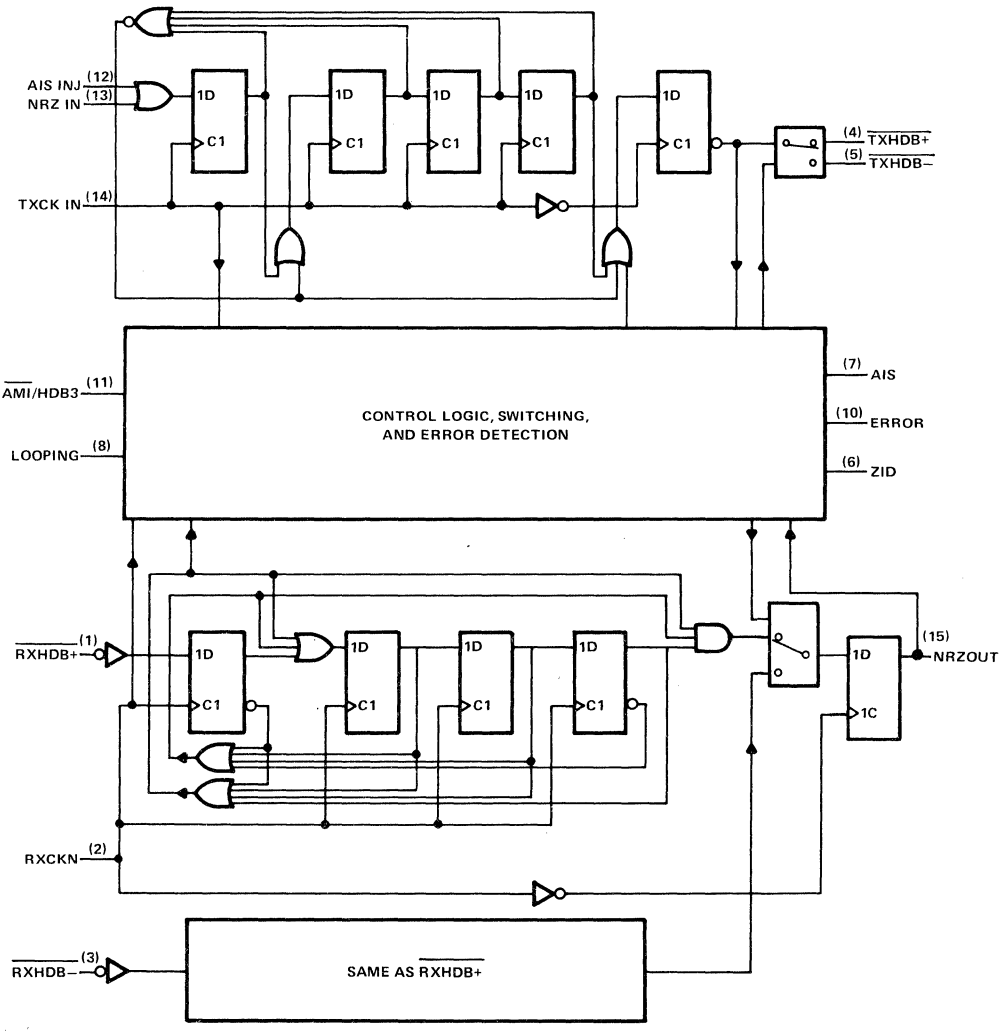
functional block diagram

TCM2222



PIN FUNCTIONAL DESCRIPTION WITHOUT CPU INTERFACE

PIN			DESCRIPTION
TCM2202	TCM2222	NAME	
1	1	$\overline{\text{RXHDB}+}$	Receive High-Density Bipolar Positive input. One of two data inputs to the decoder section. A low level indicates a positive pulse from the line.
2	2	RXCKIN	Clock from PCM transceiver. $\overline{\text{RXHDB}+}$ and $\overline{\text{RXHDB}-}$ data are clocked in on the rising edge of RXCKIN.
3	3	$\overline{\text{RXHDB}-}$	Receive High-Density Bipolar Negative input. One of two data inputs to the decoder section. A low level indicates a negative pulse from the line.
4	4	$\overline{\text{TXHDB}+}$	Transmit High-Density Bipolar Positive output. Low when a positive pulse is sent to the line.
5	5	$\overline{\text{TXHDB}-}$	Transmit High-Density Bipolar Negative output. Low when a negative pulse is sent to the line.
6		CLKFAILS	Clock Fails input. Normally connected to the mute output of the line interface. When high, indicates the absence of any clock from the PCM transceiver (RXCKIN) and causes the TCM2202 to go into the loop mode.
7		OSLIN(1)	Output Signal Loss input. When high, activates the Output Signal Loss (OSL) output.
8		OSLIN(2)	Output Signal Loss input. When high, activates the Output Signal Loss (OSL) output.
9		OSL	Output Signal Loss output. High when the OSLIN(1) or OSLIN(2) input is high.
10		ISL	Incoming Signal Loss output. Buffered version of CLKFAILS input synchronized to TXCKIN.
11	6	ZID	Incoming Zero Detection output. High when a sequence of 128 consecutive lows is received from the line. Disabled in the AMI mode.
12	7	AIS	Alarm Inhibit Signal output. High when an alarm-inhibit signal consisting of essentially all highs is received from the line.
13		SLCKIN	Slow Clock input for error detection. Can be an input for an external clock. Normally, a capacitor is connected between this pin and ground.
14		SLCKOUT	Slow Clock output for error integration. Normally, a resistor is connected between this pin and the SLCKIN pin.
15	9	V_{DD}	Positive supply voltage. 5 V ±10%.
16	10	ERROR	Error output. Goes high for one-half cycle at every error found in the incoming line signal.
17		10^{-3} ERROR	Error output goes high if the input error rate is greater than 1 in 10^3 receive clock cycles over a period of time defined by 1000 slow clock pulses.
18		10^{-5} ERROR	Error output goes high if the input error rate is greater than 1 in 10^5 receive clock cycles over a period of time defined by 1000 slow clock pulses.
19	11	$\overline{\text{AMI}}$/HDB3	Alternate Mark Inversion ($\overline{\text{AMI}}$) or High-Density Bipolar Three (HDB3) control input. When high, HDB3 is selected. When low, $\overline{\text{AMI}}$ is selected.
20	12	AIS INJ	Alarm Inhibit Signal Injection input. Forces the alarm inhibit signal (all pulses) onto outputs $\overline{\text{TXHDB}+}$ and $\overline{\text{TXHDB}-}$.
21		TEST	5 V ±10% (tied to V_{DD})
22	8	LOOPING	When high, the coder outputs are internally looped to the decoder inputs.
23		RESET	Control input to clear the AIS, ZID, and OSL outputs. When low, the error outputs are latched. AIS, ZID, and OSL are cleared when RESET goes high. When RESET is high, the error outputs reflect the current presence or absence of these errors.
24	13	NRZIN	Serial binary Non-Return-to-Zero (NRZ) data input.
25	14	TXCKIN	Transmit Clock input. The NRZIN input data is clocked in on the rising edge of TXCKIN.
26	15	NRZOUT	Non-Return-to-Zero output. Binary NRZ data recovered from the $\overline{\text{RXHDB}+}$ and $\overline{\text{RXHDB}-}$ inputs. "Stuffing" sequence pulses are removed when the $\overline{\text{AMI}}$/HDB3 control input is high.
27		RXCKOUT	Receive Clock output. Buffered TTL-compatible output that is derived from the RXCKIN input, but of opposite phase.
28	16	V_{SS}	Supply ground (0 V).

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TCM2202 PIN FUNCTIONAL DESCRIPTION WITH CPU INTERFACE

PIN		DESCRIPTION
TCM2202	NAME	
1	$\overline{\text{RXHDB}}+$	Receive High-Density Bipolar Positive input. One of two data inputs to decoder section. A low level indicates a positive pulse from the line.
2	RXCKIN	Clock from PCM transceiver. $\overline{\text{RXHDB}}+$ and $\overline{\text{RXHDB}}-$ data are clocked in on the rising edge of RSCKIN.
3	$\overline{\text{RXHDB}}-$	Receive High-Density Bipolar Negative input. One of two data inputs to decoder section. A low level indicates a negative pulse from the line.
4	$\overline{\text{TXHDB}}+$	Transmit High-Density Bipolar Positive output. Low when a positive pulse is sent to the line.
5	$\overline{\text{TXHDB}}-$	Transmit High-Density Bipolar Negative output. Low when a negative pulse is sent to the line.
6	CLKFAILS	Clock Fails input. Normally connected to the mute output of the line interface. When high, indicates the absence of any clock from the PCM transceiver (RXCKIN) and causes the TCM2202 to go into the loop mode.
7	OSLIN(1)	Output Signal Loss input. When high, activates the output signal loss (OSL) output.
8	OSLIN(2)	Output Signal Loss input. When high, activates the output signal loss (OSL) output.
9 10 11 12	D6 D4 D2 D0 (LSB)	Four bits of the 8-bit bidirectional data bus. Outputs are at high impedance when $\overline{\text{CE}}$ is high or $\overline{\text{DBIN}}$ is low. When $\overline{\text{CE}}$ is low and $\overline{\text{DBIN}}$ is high, the TCM2202 places the contents of the status register onto the data bus.
13	SLCKIN	Slow Clock input for error detection. Can be an input for an external clock. Normally, a capacitor is connected between this pin and ground.
14	SCLKOUT	Slow Clock output for error integration. Normally, a resistor is connected from this pin to SLCKIN.
15	V_{DD}	Positive supply voltage. 5 V $\pm$10%.
16	$\overline{\text{INT}}$	Interrupt output. When low, a diagnostic has occurred. The exact diagnostic can be found by reading the status register.
17 18 19 20	D1 D3 D5 D7 (MSB)	Four bits of the 8-bit bidirectional data bus. Outputs are at high impedance when $\overline{\text{CE}}$ is high or $\overline{\text{DBIN}}$ is low. When $\overline{\text{CE}}$ is low and $\overline{\text{DBIN}}$ is high, the TCM2202 places the contents of the status register onto the data bus.
21	$\overline{\text{DBIN}}$	Databus input. When high (if $\overline{\text{CE}}$ is low), the TCM2202 data bus ports D0 through D7 are outputs. When low, D0 through D7 are inputs.
22	$\overline{\text{CE}}$	Chip Enable input. When high, outputs D0 through D7 are in high-impedance state.
23	$\overline{\text{WE}}$	Write Enable input. The rising edge latches data from the data bus during a write to the TCM2202.
24	NRZIN	Serial binary Non-Return-to-Zero (NRZ) data input.
25	TXCKIN	Transmit clock input. The NRZIN input data is clocked in on the rising edge of TXCKIN.
26	NRZOUT	Binary NRZ data recovered from the $\overline{\text{RXHDB}}+$ and $\overline{\text{RXHDB}}-$ inputs. Stuffing sequence pulses are removed when the $\overline{\text{AMI}}$/HDB3 control input is high.
27	RXCKOUT	Buffered TTL-comptible clock that is derived from the RXCKIN input, but of opposite phase.
28	V_{SS}	Supply ground (0 V).

absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 0.3 V to 7 V
Input voltage, V_I . . . . . −0.3 V to 20 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: All voltages are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply ground		0		V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs except $\overline{\text{TXHDB}\pm}$, SLCLKOUT	V_{DD} = 5 V, I_{OH} = −120 μA	2.4			V
		$\overline{\text{TXHDB}+}$, $\overline{\text{TXHDB}-}$	V_{DD} = 5 V, I_{OH} = − 40 μA	4.2			
V_{OL}	Low-level output voltage	All outputs except $\overline{\text{TXHDB}\pm}$, SLCLKOUT	V_{DD} = 5 V, I_{OL} = 2.4 mA			0.4	V
		$\overline{\text{TXHDB}+}$, $\overline{\text{TXHDB}-}$	V_{DD} = 5 V, I_{OL} = 2 mA			0.4	
I_{IH}	High-level input current	All inputs except OSLIN(1), OSLIN(2) RESET, and TEST	V_{DD} = 5.5 V, V_{IH} = 2.4 V			10	μA
I_{IL}	Low-level input current		V_{DD} = 5.5 V, V_{IL} = 0.4 V			−10	μA
I_{DD}	Supply current		V_{DD} = 5 V		45	60	mA
C_i	Input capacitance					20	pF
	Threshold voltage at OSLIN(1) or OSLIN(2) required to switch OSL				$V_{DD}/2$		V

timing requirements, transmit and receive sections

PARAMETER		MIN	MAX	UNIT
t_{su1}	Setup time, NRZIN before TXCKIN↑	40		ns
t_{h1}	Hold time NRZIN after TXCKIN↑	40		ns
t_{su2}	Setup time, $\overline{\text{RXHDB}\pm}$ before RXCKIN↑	40		ns
t_{h2}	Hold time, $\overline{\text{RXHDB}\pm}$ after RXCKIN↑	40		ns
t_{r1}	Rise time, RXCKIN		25	ns
t_{f1}	Fall time, RXCKIN		15	ns

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switching characteristics, transmit and receive sections

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{r2}	Rise time, $\overline{TXHDB\pm}$	C_L = 25 pF,	I_{OH} = −40 μA		40	ns
t_{f2}	Fall time, $\overline{TXHDB\pm}$	C_L = 25 pF,	I_{OL} = 2 mA		40	ns
t_{r3}	Rise time, RXCKOUT, NRZOUT	C_L = 50 pF,	I_{OH} = −120 μA		100	ns
t_{f3}	Fall time, RXCKOUT, NRZOUT	C_L = 50 pF,	I_{OL} = 2.4 mA		100	ns
t_{w1}	Pulse duration, ERROR output	I_{OH} = −120 μA, C_L = 25 pF,	I_{OL} = 2.4 mA, t_{cC} = 488 ns	200		ns
t_{pd1}	Propagation delay, TXCKIN to $\overline{TXHDB\pm}$	I_{OH} = −40 μA, C_L = 25 pF	I_{OL} = 2 mA,	50	200	ns
t_{pd2}	Propagation delay, RXCKIN to RXCKOUT	I_{OH} = −120 μA, C_L = 25 pF	I_{OL} = 2.4 mA,		125	ns
t_{d1}	Delay time, NRZOUT after RXCKOUT↑	I_{OH} = −120 μA, C_L = 50 pF	I_{OL} = 2.4 mA,	0	150	ns

timing requirements, TCM2202 microprocessor interface

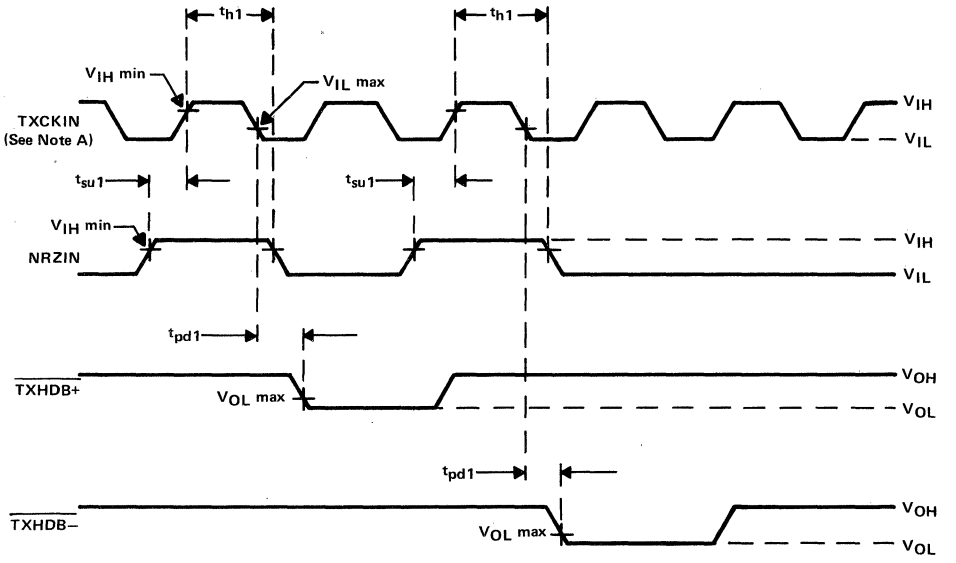
PARAMETER		MIN	MAX	UNIT
t_{su3}	Setup time, $\overline{CE}$ low before $\overline{DBIN}$↑	0		ns
t_{su4}	Setup time, $\overline{CE}$ high before $\overline{DBIN}$↓	0		ns
t_{su5}	Setup time, $\overline{CE}$ low before $\overline{WE}$↑	200		ns
t_{su6}	Setup time, $\overline{DBIN}$ low before $\overline{WE}$↑	200		ns
t_{su7}	Setup time, valid data before $\overline{WE}$↑	50		ns
t_{h3}	Hold time, $\overline{CE}$ low after $\overline{WE}$↑	0		ns
t_{h4}	Hold time, $\overline{DBIN}$ low after $\overline{WE}$↑	0		ns
t_{h5}	Hold time, valid data after $\overline{WE}$↑	20		ns
t_{w2}	Pulse duration, $\overline{CE}$ low	200		ns
t_{w3}	Pulse duration, $\overline{DBIN}$ high or low	200		ns
t_{w4}	Pulse duration, $\overline{WE}$ high or low	100		ns

switching characteristics, TCM2202 microprocessor interface

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{en}	Enable time, $\overline{DBIN}$↑ to valid data out	C_L = 100 pF, $\overline{CE}$ low		150		ns
t_{dis}	Disable time, $\overline{CE}$↑ to high impedance on D0 through D7	C_L = 100 pF			100	ns

†All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTE A: The CLKSENSE is low and the rising edge of the TXCKIN is used to strobe NRZIN.
† In the HDB3 mode, the pulses on $\overline{\text{TXHDB}}\pm$ are delayed three additional clock periods.

FIGURE 1. TRANSMIT CHANNEL TIMING INFORMATION (AMI MODE†)

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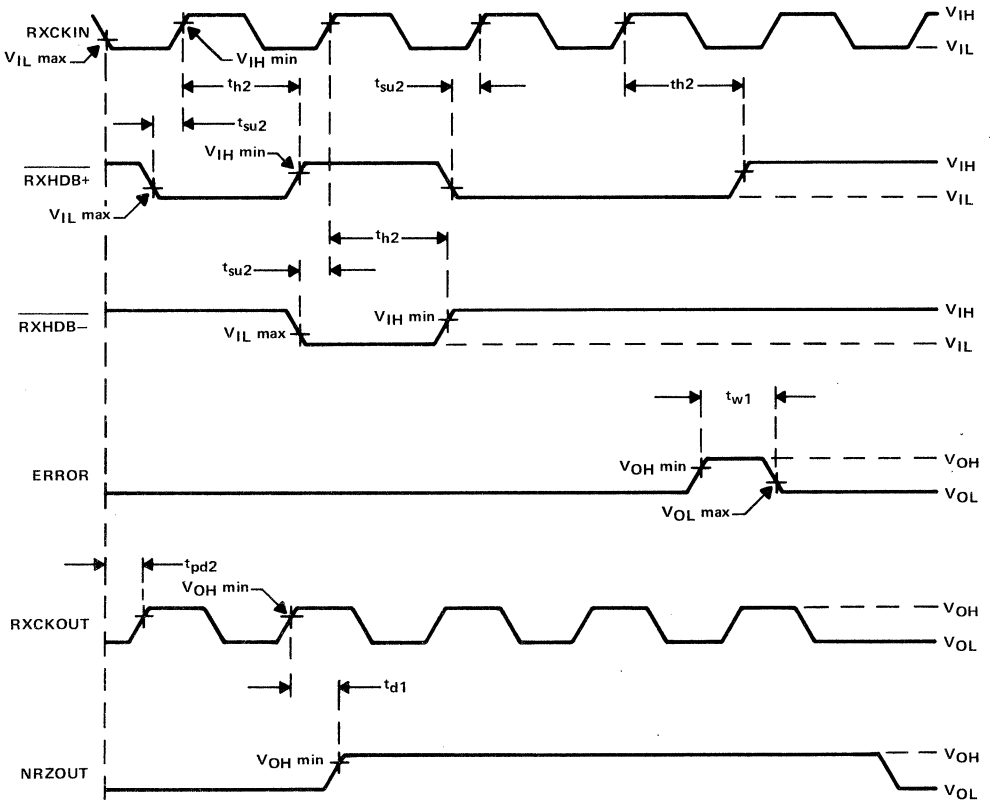
PARAMETER MEASUREMENT INFORMATION



† In the HDB3 mode NRZOUT is delayed three additional clock periods.

FIGURE 2. RECEIVE CHANNEL TIMING INFORMATION (AMI MODE†)

PARAMETER MEASUREMENT INFORMATION

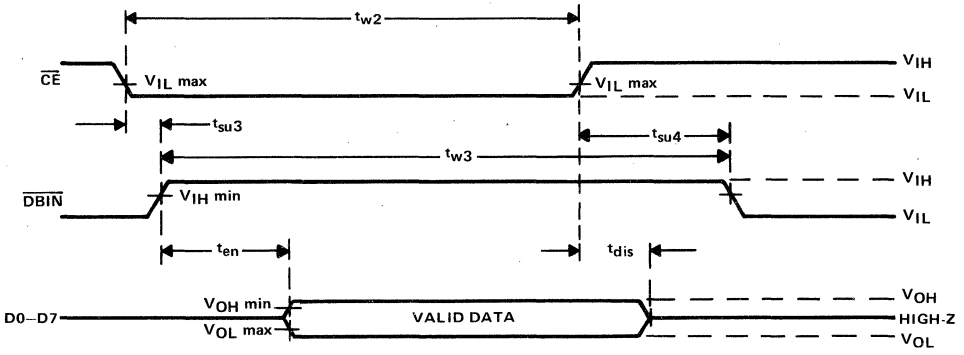


FIGURE 3. MICROPROCESSOR INTERFACE WRITE TO CPU (TCM2202 ONLY)

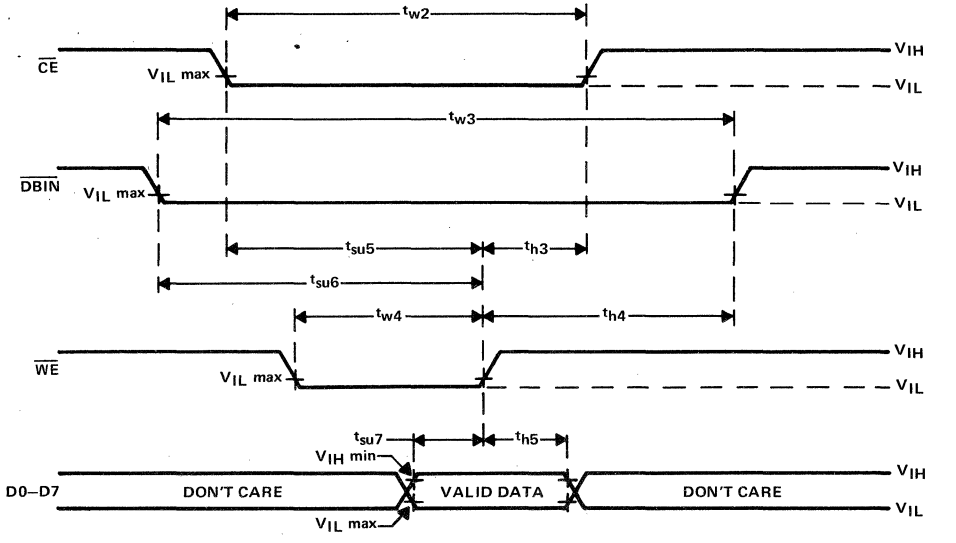


FIGURE 4. MICROPROCESSOR INTERFACE READ FROM CPU (TCM2202 ONLY)

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PRINCIPLES OF OPERATION

The TCM2202 and TCM2222 combine a coder section and a decoder section to which a signal monitor function is attached. They can operate at clock frequencies from zero to 3 MHz in either the AMI or HDB3 modes. The AMI or HDB3 mode is selected by the $\overline{\text{AMI}}$/HDB3 input. The TCM2202 can operate with or without a microprocessor interface. The selection of operation with or without the microprocessor interface is controlled by the TEST input. When the TEST input is connected to V_{DD}, operation without the interface is selected. When the microprocessor interface is selected, the TEST input acts as $\overline{\text{DBIN}}$. In the following description, operation without the interface is described first, with the differences for operation with the interface described afterward.

operation without microprocessor interface

Binary data at the NRZIN input is clocked into the coder on the rising edge of TXCKIN. In the AMI mode a logic high at NRZIN causes an output at either $\overline{\text{TXHDB}+}$ or $\overline{\text{TXHDB}-}$ on the falling edge of TXCKIN. In the HDB3 mode, the output appears on the falling edge of TXCKIN 3.5 clock cycles later. This delay allows the insertion of extra pulses due to sequences of four consecutive lows. When the AIS INJ input is high, data at NRZIN is ignored and an "all highs" signal is transmitted with alternate outputs on $\overline{\text{TXHDB}+}$ and $\overline{\text{TXHDB}-}$ every clock cycle.

Ternary data received at $\overline{\text{RXHDB}-}$ or $\overline{\text{RXHDB}+}$ is clocked into a decoder on the rising edge of RXCKIN. In the AMI mode, the decoded data is output on NRZOUT on the falling edge of RXCKIN 0.5 clock cycles later. In the HDB3 mode, the receiver recognizes violation pulses and removes any pulse sequences added by the originating equipment, and outputs the decoded data 3.5 clock cycles later.

If the LOOPING input is high, the decoder ignores data received on $\overline{\text{RXHDB}+}$ or $\overline{\text{RXHDB}-}$ and uses data at the $\overline{\text{TXHDB}+}$ and $\overline{\text{TXHDB}-}$ outputs. In addition, RXCKIN is ignored and TXCKIN is used to control the decoder timing. In the AMI mode there is a 1.5-clock-cycle delay from NRZIN to NRZOUT. In the HDB3 mode the delay is 7.5 clock cycles.

A signal monitor circuit associated with the decoder monitors the received ternary signal and diagnoses the presence of particular conditions. There are seven outputs: six received signal diagnostic outputs and one output that monitors the transmitted ternary signal. The seven outputs are as follows:

ERROR — This output flags an error in the received signal by pulsing high for 0.5 clock cycles. In the AMI mode an error is two consecutive pulses of the same polarity. In the HDB3 mode an error can be either the same as the AMI error (provided it is not part of a violation stuffing sequence) or an incorrect stuffing sequence. On power up, the ERROR output remains high until the RXCKIN input is functioning.

10^{-5} ERROR — This is an error rate flag that is set high if an error rate of 1 error for 10^5 clock cycles is detected over a period defined by the slow clock. The slow clock frequency is determined by the time constant of an RC network connected to SLCKIN and SLCKOUT and is typically 100 Hz. The integration period for error rate detection is 1000 slow clock cycles. Each received error increments a counter, which is decremented every 10^5 clock cycles. If there are no errors, the counter will remain at zero. The counter must remain at a non-zero value for the entire integration period (typically 10 seconds) in order to set the 10^5 ERROR output. A hysteresis factor of 1:4 is built into this flag. When the flag is set, it cannot be reset until the error rate has fallen to less than 1 in 400,000.

PRINCIPLES OF OPERATION

10^{-3} ERROR This is a gross-error-rate flag. Flag operation is identical to the 10^{-5} ERROR except that the counter is decremented every 1024 clock cycles giving an error rate indicator of approximately 1 in 1000. The hysteresis is increased to 1:8.

ZID This flag is set high if a sequence of 128 incoming lows is detected. It is inhibited when the device is in AMI mode. The output is latched if the RESET input is low.

AIS The AIS output goes high when two frames of 512 bits each, each containing no more than two lows, is received. If the reset input is low, the output is latched. This flag is set if a sequence of continuous highs is detected.

ISL This flag is set to indicate failure of the received clock. The CLKFAILS input has to be driven high to indicate loss of signal. This is typically driven by the mute output from TCM2203, a retriggerable monostable controlled by RXCKIN, or the ZID output. The CLKFAILS input is buffered onto the ISL output and synchronized to the transmit clock. If CLKFAILS goes high, the TCM2202 switches into a loop back mode, which is analogous to taking the LOOPING pin high.

OSL This output reflects the condition of the two inputs, OSLIN(1) and OSLIN(2). Each one of the inputs monitors one of the line driver transistors on the TCM2203 line interface (or equivalent line drive device). The drive transistor outputs are connected by RC networks to OSLIN(0) and OSLIN(1) inputs so that one capacitor is discharged by each output pulse. If the output signal fails, a capacitor will charge to the OSLIN threshold level and OSL will be set high. It is latched if the RESET input is low.

Other pin functions are as follows:

RESET A positive transition on this input resets the ZID, AIS, and OSL outputs for one cycle of RXCKIN. They are then free to be set again when their diagnostic condition occurs. RESET can be used in the normally high mode, in which the three outputs are not latched but continuously reflect the current diagnostic status.

operation with the microprocessor interface (TCM2202 only)

The TCM2202 can be operated with a microprocessor interface by controlling the TEST/$\overline{\text{DBIN}}$ input. When power is initially applied to the device, operation without the interface is selected and remains selected until a logic low at the TEST/$\overline{\text{DBIN}}$ input puts it into the software mode. The device will then operate with the microprocessor interface until power is removed.

When operating with the microprocessor interface, the functions of several pins are altered. The functions of the coder and decoder inputs and outputs remain the same, but the diagnostic outputs and control inputs are replaced by an 8-bit bidirectional data bus, three control inputs, and an interrupt output. The 8-bit bidirectional data bus is used for writing to and reading from the device internal registers.

The three control inputs are $\overline{\text{DBIN}}$, $\overline{\text{WE}}$ and $\overline{\text{CE}}$. The device is configured into the test mode by a high-to-low transition of the TEST/$\overline{\text{DBIN}}$ input. When $\overline{\text{DBIN}}$ goes low, the device latches into the software mode and remains in this mode until power is removed.

structure

The device contains an 8-bit status register that holds the seven diagnostic outputs from the signal monitor section, an 8-bit interrupt register and 3 8-bit control registers, each of which holds 5 of the 15 control inputs. There is an additional control register that is used for test purposes (see Table 1).

PRINCIPLES OF OPERATION

The three control inputs are:

$\overline{DBIN}$ When $\overline{DBIN}$ has gone low to set the device into the software mode, it controls the direction of data flow on the data bus. It is high to read data from the TCM2202 (status register) and low to write data to the TCM2202 (control or interrupt registers).

$\overline{CE}$ Chip enable. When high, D0 through D7 are in a high-impedance state. It is typically an address decode of the controller.

$\overline{WE}$ Write enable. The rising edge of $\overline{WE}$ strobes in data from the bus to the TCM2202 when $\overline{CE}$ and $\overline{DBIN}$ are low. It can be tied to $\overline{DBIN}$ in certain CPU systems.

Table 1. Software Mode Register Map

REGISTER	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Status	ERROR	L	OSL	ISL	10^{-5}	ZID	10^{-3}	AIS
Interrupt	L	Enable	OSL	ISL	10^{-5}	ZID	10^{-3}	AIS
Control 0	H	L	L	CLKSENSE	RESET	LOOPING	AIS INJ	$\overline{AMI}$/HDB3
Control 1	H	L	H	FRAMESIZE	Z(3)	Z(2)	Z(1)	Z(0)
Control 2	H	H	L	AISZ(1)	AISZ(0)	FSEO(2)	FSEO(1)	FSEO(0)
Control 3	H	H	H		Used for test purposes only			

H = high level, L = low level

internal registers

There are three types of internal registers: interrupt, control, and status.

interrupt register

Six diagnostics can each be set to cause an interrupt output if required. They are individually enabled or disabled by writing to the interrupt register. A low in bit D7 addresses the interrupt register.

A particular diagnostic condition is enabled to cause an interrupt when the relevant bit in the interrupt register contains a high. A logic high in bit D3 causes an interrupt when an error rate of 1 in 100,000 is detected. Individual bits in the register can be set if bit D6 is a high or reset if bit D6 is a low. When enabling interrupts (D6 = H) any highs on the data bus bits D0 to D5 are written to the appropriate register bits, lows are ignored. When disabled (D6 = L) any low on data bus bits D0 through D5 are written into the appropriate register bits and highs are ignored. At power-up, the interrupt register is reset so no interrupts are enabled.

control register

The control registers can be written to at any time with the first three bits acting as the address. The control functions $\overline{AMI}$/HDB3, AIS INJ, LOOPING, and RESET are identical to the hardware-mode pin functions.

The other control register bits, as specified in Table 1, have the following functions:

CLKSENSE — changes the TXCKIN clock edge on which NRZIN is strobed. When low, the rising edge is used (as in the hardware mode); when high, the falling edge is used.

Z(0), Z(1), Z(2), Z(3) — define the number of consecutive lows needed to set the ZID output, according to Table 2.

PRINCIPLES OF OPERATION

TABLE 2

NUMBER OF CONSECUTIVE LOWS NEEDED TO SET ZID	CONTROL REGISTER BIT STATUS Z(3)	Z(2)	Z(1)	Z(0)
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
16	H	H	L	L
32	H	H	L	H
64	H	H	H	L
128 (as in hardware mode)	H	H	H	H

FRAMESIZE — controls the size of the frame used for the AIS flag. A low in this bit position gives a framesize of 256 bits and a high gives a framesize of 512 bits (as in the Hardware Mode).

FSEQ(0), FSEQ(1), FSEQ(2) — define the number of successive frames required to set the AIS flag, according to Table 3.

TABLE 3

NUMBER OF CONSECUTIVE FRAMES NEEDED TO SET AIS	CONTROL REGISTER BIT STATUS FSEQ(2)	FSEQ(1)	FSEQ(0)
1	L	L	L
2 (as in hardware mode)	L	L	H
3	L	H	L
4	L	H	H
5	H	L	L
6	H	L	H
7	H	H	L
8	H	H	H

AISZ(0), AISZ(1) — define the maximum number of lows allowed in a frame if AIS is to be set, according to Table 4.

TABLE 4

MAXIMUM NUMBER OF LOWS ALLOWED PER FRAME TO SET AIS	CONTROL REGISTER BIT STATUS AISZ(1)	AISZ(0)
4	L	L
1	L	H
2 (as in hardware mode)	H	L
3	H	H

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PRINCIPLES OF OPERATION

At power up all registers are initialized low. If the software mode is selected by pulling DBIN low, then the following default condition exists:

Number of consecutive lows needed to set ZID	=	undefined
Number of consecutive frames needed to set AIS	=	1
Maximum number of lows allowed per frame to set AIS	=	4
Number of bits per frame to set AIS	=	256

However, it is recommended that, in the software mode, the control register bits always be explicitly programmed.

status register

The status register can be read at any time by taking $\overline{CE}$ low and $\overline{DBIN}$ high. The status register is true when high. The values in the status register cannot change during a read operation if a diagnostic occurs at the same time. The register will be updated when the read is completed. The ERROR bit (D7) is latched when an error occurs and is reset after a read operation.

ternary data transmission

Ternary signals are used in telecommunications to transmit data over long distances because they offer improved transmission characteristics compared to binary signals. The requirements are:

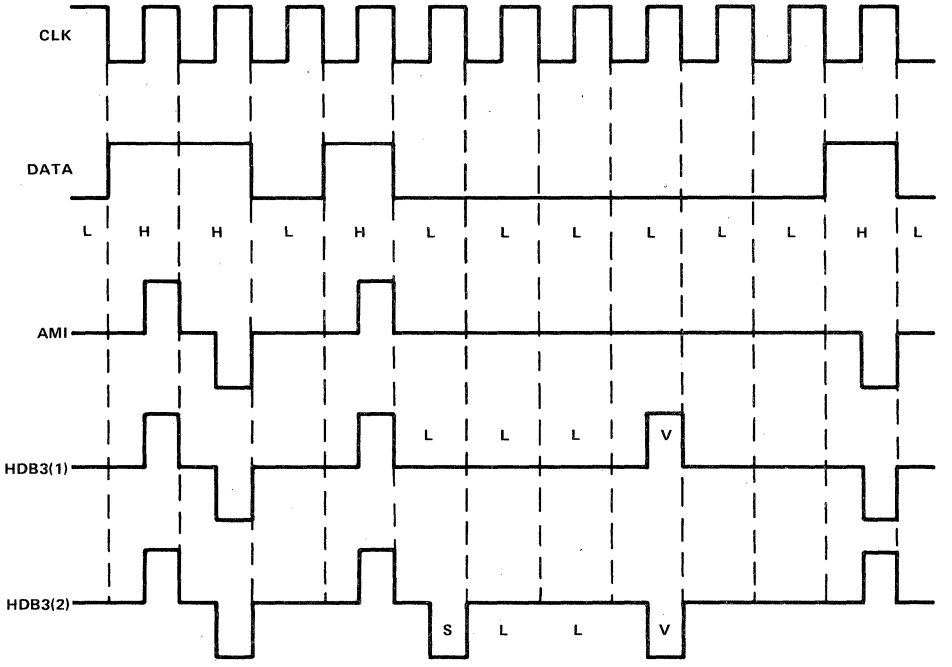
Narrow bandwidth for good signal-to-noise ratio.
Minimum high-frequency content to allow wider repeater spacing.
No dc component in the signal to allow inexpensive transformer coupling without distortion.
Timing information carried with the data to allow extraction of the clock.
Error detection to flag faults and enable their location.

The ternary signal is bipolar. It has a zero center level, which is the rest condition, and positive and negative levels of equal amplitude. The simplest form of coding is Alternate Mark Inversion (AMI) in which successive logic highs in the binary signal are transmitted alternately as positive or negative pulses. Logic lows are transmitted as a zero level. The disadvantage of this type of coding is that no timing information is contained in a succession of logic lows, requiring the remote receiver to use a high-Q (crystal-controlled) clock extraction circuit if long successions of lows are to be received.

To improve the timing content, high-density bipolar third-order coding (HDB3) can be used. This is identical to AMI except that four successive lows cause the insertion of a violation bit that is a logic high pulse of the same polarity as the previous logic high pulse (see Figure 3). This increases the timing information and allows the use of a low-Q LC tank circuit in the clock extractor. The extra bits are removed by the decoder, introducing a transmission delay of four cycles.

In order to maintain zero dc content, the violation bit must be the same polarity as the previous bit but of opposite polarity to the previous violation bit. To replace four consecutive lows, there are two possible sequences of pulses; LLLV if there is an odd number of logic highs since the last violation bit, or SLLV if there is an even number of logic highs. In this notation S represents a "stuffing" bit of opposite polarity than the previous pulse and V represents a "violation" bit of the same polarity.

PRINCIPLES OF OPERATION



NOTE 2: In the HDB3(1) signal, the previous violation bit was negative. In the HDB3(2) signal, the previous violation bit was positive.

FIGURE 5. TERNARY DATA TRANSMISSION TIMING DIAGRAM

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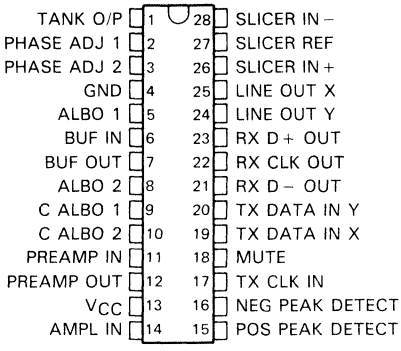
D2861, AUGUST 1985 – REVISED APRIL 1986

- **Transmits and Receives Serial Bipolar Data at up to 3 Mbit/s Using Two Twisted-Wire Pairs.**
- **Low-Q Clock Extraction**
- **Two ALBO (Automatic Line Build Out) Taps with a Range of 42 dB**
- **On-Chip Amplifier with 50-dB Open-Loop Voltage Amplification**
- **Phase Adjustment for Recovered Clock**
- **Direct Interface with the TCM2222 AMI/HDB3 (Alternate Mark Inversion/High-Density Bipolar, Third Order) Encoder/Decoder**
- **Receive Line Signal Loss Detection with Mute Output**
- **Bipolar Technology**

TCM2203
J
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TCM2203 is designed to perform the interface function between the bipolar data encoder/decoder (e.g., TCM2222) and the line. The TCM2203 consists of a receiver that extracts clock information and reshapes the data waveforms, and a transmitter that interfaces bipolar data to the line. Detection of receive signal loss is performed and a mute output is available. Auto-adaptive slicing level ensures excellent jitter and error performance.

The TCM2203 is characterized for operation from 0 °C to 70 °C.

PIN	NAME	DESCRIPTION
1	TANK O/P	Delivers a current pulse to the clock recovery tank circuit for every pulse received at AMPL IN
2	PHASE ADJ 1	Connections for a capacitor whose value determines the relative phase between recovered clock and data
3	PHASE ADJ 2	
4	GND	Power supply ground
5	ALBO 1	Automatic line build out number 1
6	BUF IN	Input to 6-dB buffer
7	BUF OUT	Output from 6-dB buffer
8	ALBO 2	Automatic line build out number 2
9	C ALBO 1	Connections for the ALBO control loop filter capacitor (typically, 10 μF)
10	C ALBO 2	
11	PREAMP IN	Input to 50-dB amplifier
12	PREAMP OUT	Output from 50-dB amplifier
13	V_{CC}	Supply voltage
14	AMPL IN	Input to 6-dB phase splitter. Regulated to 480 mV peak-to-peak, nominal.
15	POS PEAK DETECT	Connection for a capacitor that stores the peak amplitude of the positive recovered data (GND is the other connection)
16	NEG PEAK DETECT	Connection for a capacitor that stores the peak amplitude of the negative recovered data (GND is the other connection)
17	TX CLK IN	Transmit master clock input
18	MUTE	Takes on the high logic level when recovered data amplitude is less than 33% of the nominal value. Nominal value of 480 mV peak-to-peak is regulated at AMPL IN.
19	TX DATA IN X	Input for data to be gated with transmit clock and sent out on LINE OUT X
20	TX DATA IN Y	Input for data to be gated with transmit clock and sent out on LINE OUT Y
21	RX D− OUT	Negative recovered data output
22	RX CLK OUT	Recovered clock output
23	RX D+ OUT	Positive recovered data output
24	LINE OUT Y	Open-collector output of gated TX DATA IN Y input signal
25	LINE OUT X	Open-collector output of gated TX DATA IN X input signal
26	SLICER IN+	Positive clock slicer input
27	SLICER REF	Clock slicer reference connected to center tap of clock recovery transformer
28	SLICER IN−	Negative clock slicer input

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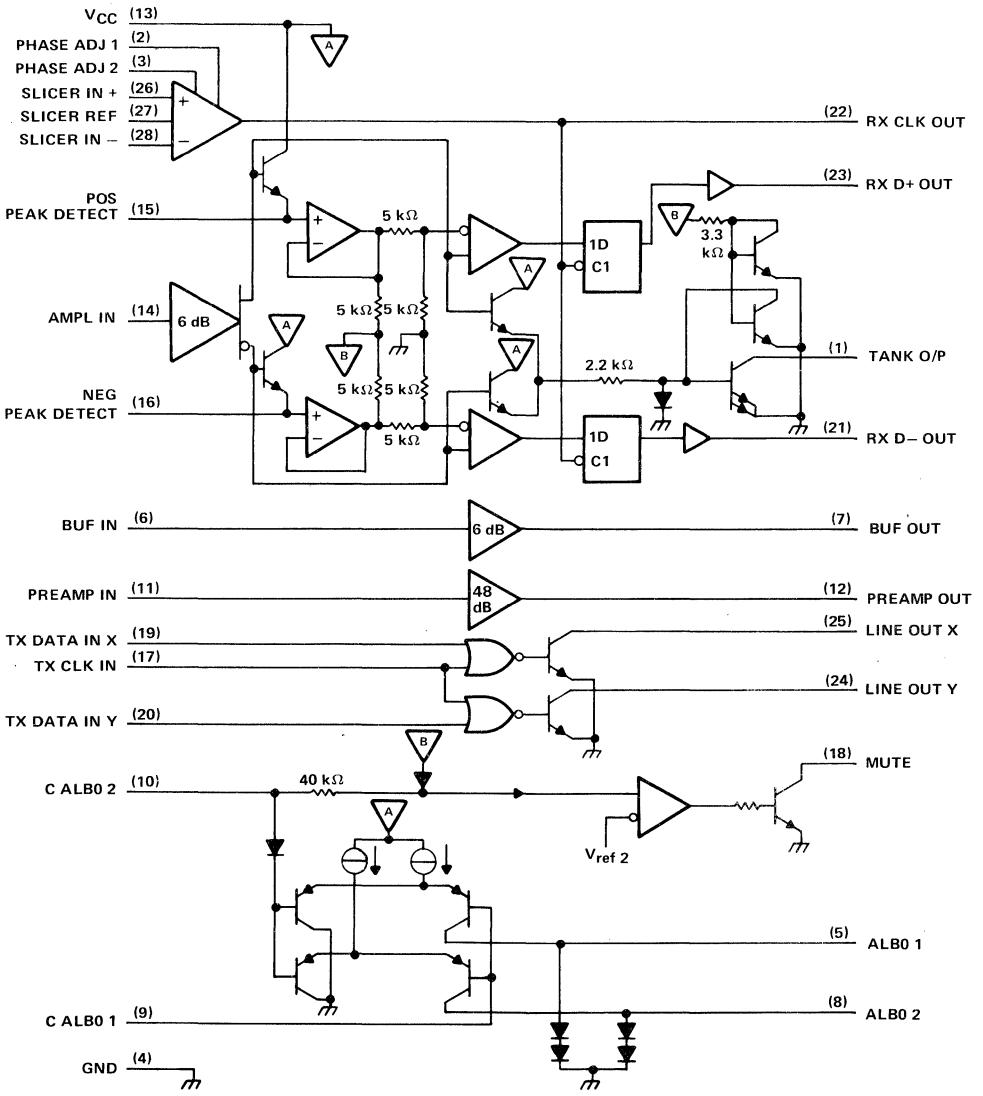
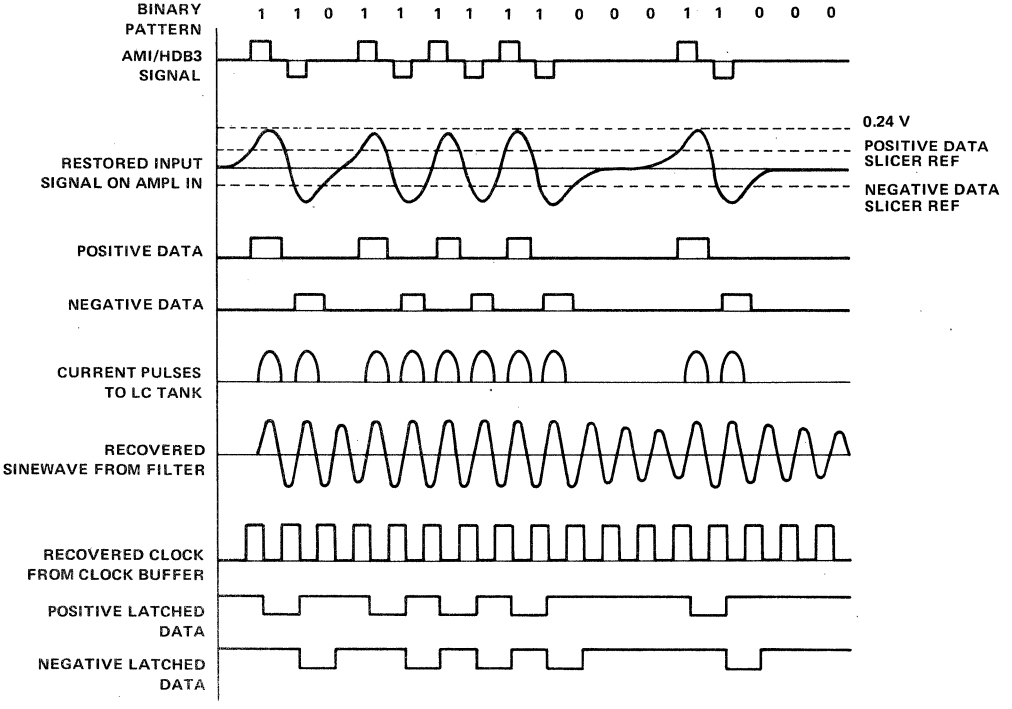
logic diagram (positive logic)



typical timing diagram



NOTE: A low logic level on RX DATA OUT represents a received pulse, or a "mark." RX DATA OUT is latched on the falling edge of RX CK OUT, and tracks the input signal when RX CK OUT is high.

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absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 15 V
Continuous total dissipation at 25°C free-air temperature . . . . . 1 W
Operating free-air temperature range . . . . . −10°C to 85°C

NOTE 1: Voltage is with respect to network ground.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5.0	5.5	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	SECTION	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
On-state impedance	ALBO			10	20	Ω
Off-state impedance			5	10		kΩ
Dynamic resistance matching error					2	%
Transconductance‡ (referenced to pin 14)		V_{P-P} = 480 mV		0.3		S
Input impedance	Buffer	f = 1 MHz	10	20		kΩ
Output impedance				40		Ω
Voltage amplification				6		dB
Output impedance	Preamplifier	f = 1 MHz		50		Ω
Open-loop voltage amplification		f = 1 MHz		48		dB
Unity-gain frequency				40		MHz
Input impedance	Phase splitter amplifier	f = 1 MHz		10		kΩ
Voltage amplification (each output)				6		dB
Capacitance-driving capability, peak detect pins					0.1	μF
Input impedance	Clock Slicer	f = 2 MHz	20	30		kΩ
Voltage amplification		f = 2 MHz		60		dB
Input-to-output delay		f = 2 MHz, PHASE ADJ CAP = 75 pF		60		ns
Peak-to-peak eye amplitude	Data Slicer	V_{CC} = 5 V		480		mV
Data slicing level				50%		
Clock slicing level§				66%		
Negative-going threshold voltage	Mute	V_{CC} = 5 V		3.26		V
Positive-going threshold voltage				3.66		
High-level output current, I_{OH}	RX D+ OUT, RX D− OUT	V_{OH} = 4 V			10	μA
Low-level output voltage, V_{OL}		I_{OL} = 2 mA		0.7	1	V
High-level output current, I_{OH}	LINE OUT X, LINE OUT Y	V_{OH} = 5 V			50	μA
Low-level output voltage, V_{OL}		I_{OL} = 20 mA		0.7	1	V
Output rise time, t_r	LINE OUT X, LINE OUT Y	R_L = 220 Ω		30	45	ns
Output fall time, t_f		R_L = 220 Ω		30	35	ns
Supply current, I_{CC}				25	40	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Transconductance is defined as the change in current for each diode string divided by the change in peak-to-peak voltage at pin 14.
§ Clock slicing level is the data level at which the TANK O/P puts out a current pulse.

TYPICAL CHARACTERISTICS

EYE DIAGRAM REGULATION
(AT INPUT OF 6- dB AMPLIFIER)

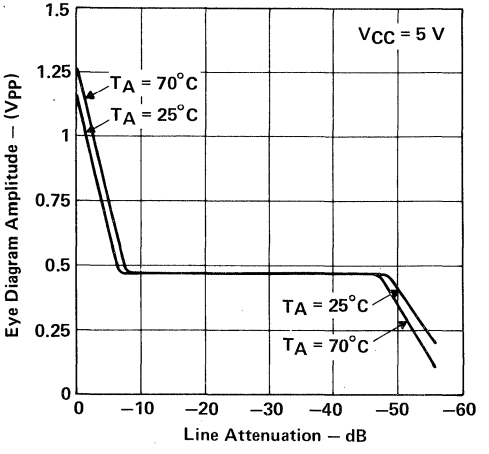

FIGURE 1

TYPICAL PREAMPLIFIER VOLTAGE
AMPLIFICATION CHARACTERISTICS

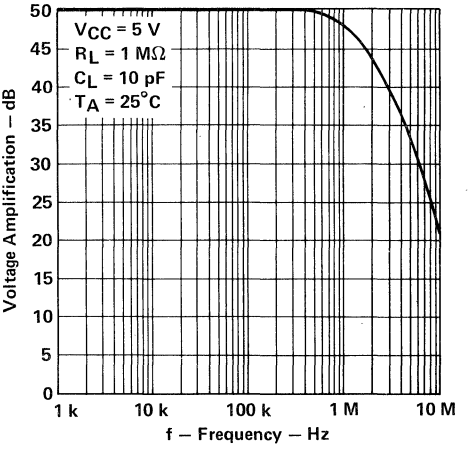

FIGURE 2

TYPICAL PREAMPLIFIER PHASE CHARACTERISTICS

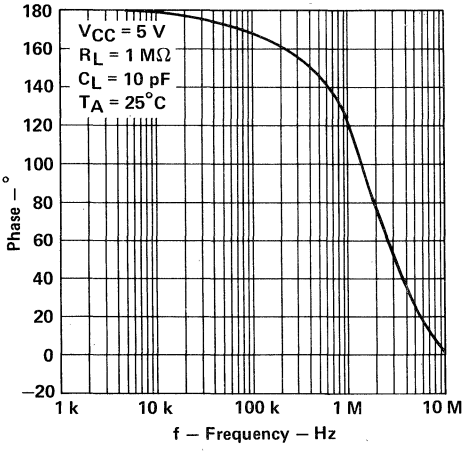

FIGURE 3

PREAMPLIFIER OPEN-LOOP VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

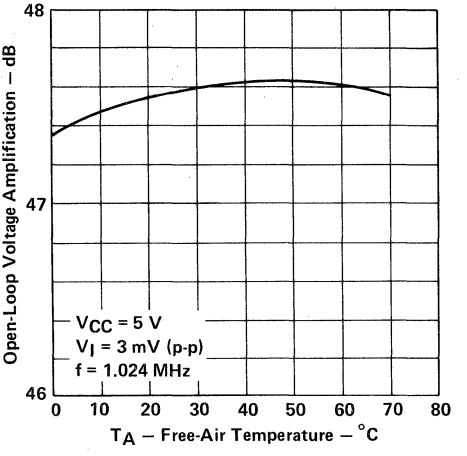

FIGURE 4

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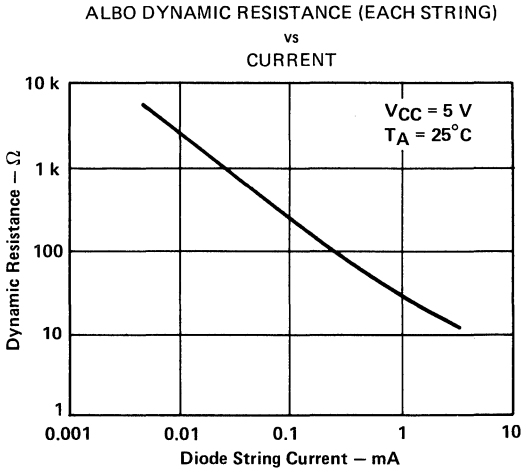

FIGURE 5

PRINCIPLES OF OPERATION

general

The TCM2203 is designed to form the interface between a bipolar decoder/encoder and the transmission line. It is optimized for 1.536 MHz, 1.544 MHz, and 2.048 MHz operation, but is capable of operating at 3.152 MHz and low frequency for special applications. The TCM2203 can be considered in two separate parts, a transmitting section and a receiving section.

receiving section

This section performs three functions: signal restoration, clock recovery, and data slicing. It also detects loss of incoming signal and flags this condition by taking the mute output high.

signal restoration

The incoming PCM signal is typically very distorted and exhibits considerable intersymbol interference. The input section must restore the signal to provide a clear eye diagram to the data and clock slicer. An amplifier with open-loop voltage amplification of 50 dB with externally adjusted gain, together with the bode networks and associated ALBO taps, give a dynamic range of up to 36 dB (6 dB to 42 dB). This allows positioning of the terminal at any line length (within the limits of ALBO dynamic range) from repeater or like transmitter.

Equalization of the line characteristics is performed by a simple external series LC network buffered by the 6-dB amplifier. The restored signal from the 6-dB phase splitter (controlled to 0.48 V peak-to-peak) is sent to two peak detectors that store the peak values on external capacitors. The average peak values are then summed to provide a signal level, which is compared to a V_{CC}-derived reference to form an error signal level. This error signal level controls the current in the ALBO strings. As ALBO string current increases, the dynamic resistance of the string decreases and more signal is shunted to ground. In this way, automatic gain control and automatic line build out are acheived. Typically, there is frequency response contouring associated with the automatic gain control to compensate for the responses of different lengths of line.

clock extraction

The received signal contains its own clock information, which must be extracted in the receive section. An averaged peak input signal is derived from the sum of the positive and negative peak detectors. The negative peak detector is actually the positive peak of AMPL IN inverted. Alternately, the peak average sum is equal to the sum of the averaged absolute values of the negative and positive peaks. When the negative or positive pulse at AMPL IN exceeds 66% of the averaged peak value, a current pulse occurs at the TANK O/P output. These current pulses are filtered by a tuned-primary transformer-coupled circuit to extract the clock and drive the slicer inputs. The slicer converts the sinewave into a binary square-wave clock signal. The transformer-coupled tuned-primary circuit sets the clock extraction Q. The slicer is a high-gain 60-dB comparator that minimizes conversion of amplitude modulation in the sine wave to phase modulation in the recovered square wave clock.

data slicing

The data comparators trigger whenever the signal goes above 50% of the average peak values from the peak detectors. This data is then presented to the data latches and latched into the output buffers by the falling edge of the recovered clock. When the RX CLK OUT is high, RX D− OUT and RX D+ OUT track the comparators. The clock buffer trigger circuit can be externally phase adjusted with a 5-pF to 75-pF trim capacitor across PHASE ADJ 1 and PHASE ADJ 2 to set the falling edge exactly to the center of the data pulses. This maximizes jitter acceptance and noise immunity.

receive signal loss detection

The average peak data values are half-summed to give a dc value that is compared to an internal reference relative to V_{CC}. When the value falls below 33% of the nominal value after ALBO gain control, the MUTE output goes high.

transmitting section

The transmitting section gates the signals applied to TX DATA IN X and TX DATA IN Y with the signal applied to TX CLK IN. The gated signals are then applied to the line outputs. The line output pulse duration is one-half of the bit period. The LINE OUT X and LINE OUT Y outputs are open-collector n-p-n transistors. Each collector will sink 20 milliamperes when the appropriate TX DATA IN input and TX CLK IN are at low levels.

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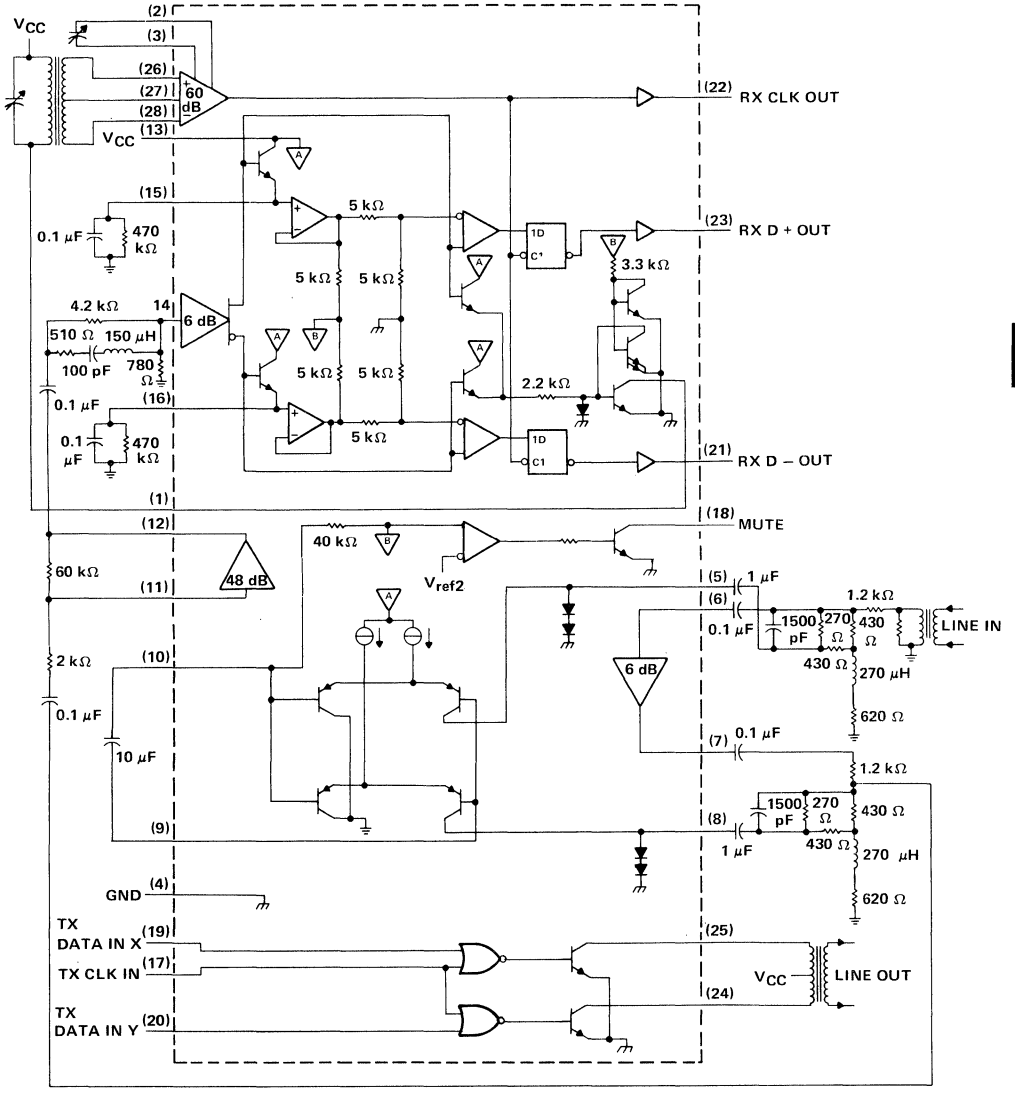
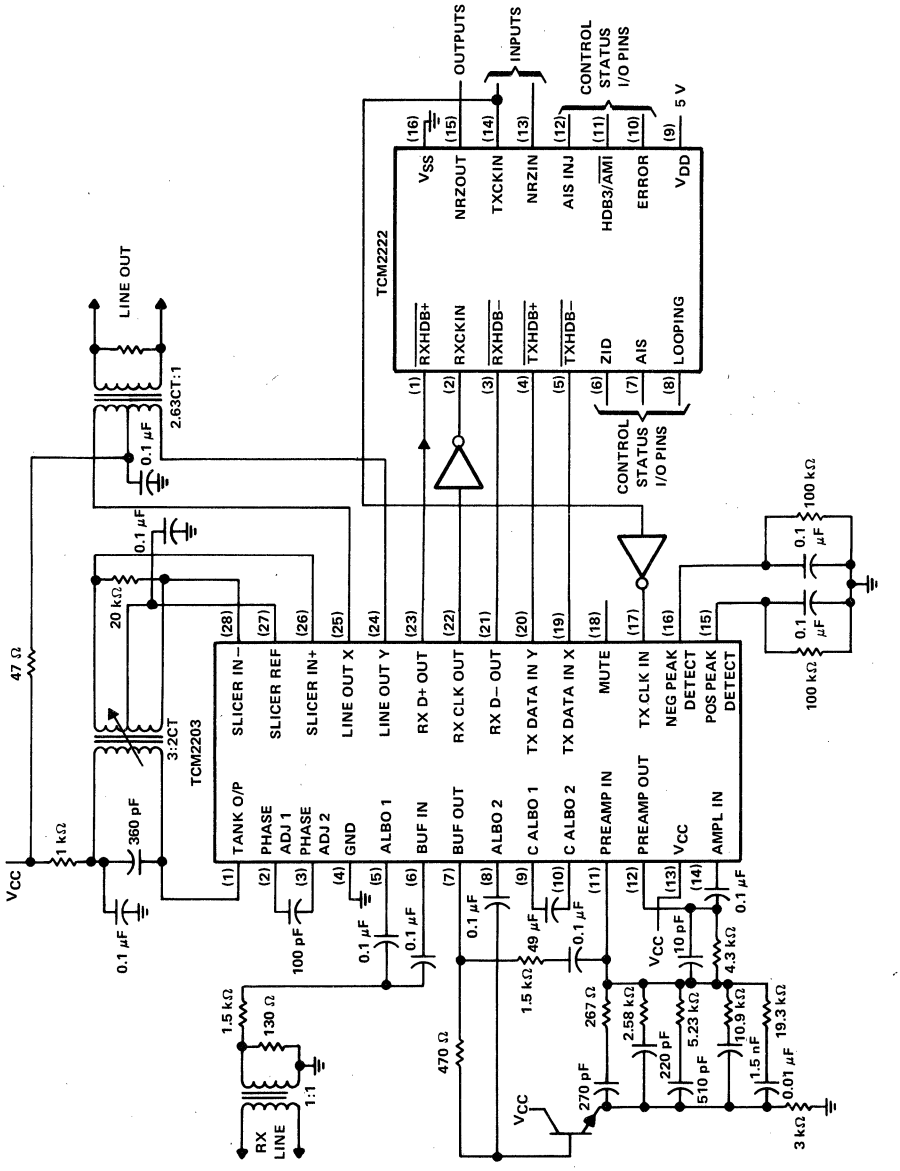
TYPICAL APPLICATION DATA



TYPICAL APPLICATION DATA



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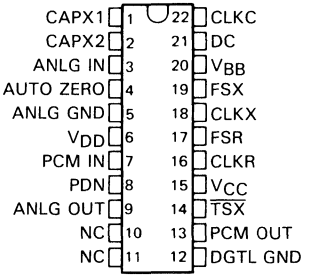
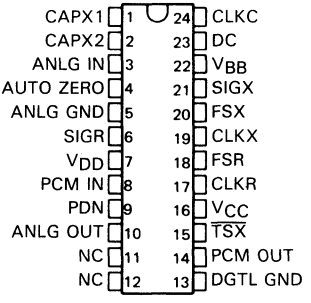
D2664, JUNE 1982—REVISED MARCH 1986

- **TCM2909 Provides μ-Law Companding in 22-Pin Package**
- **TCM2910A is Designed to be Interchangeable with Intel 2910A**
- **Compatible with CCITT Recommendations G.711 and G.712**
- **μ-255-Law Encoding and 8th-bit Signaling (TCM2910A only) Compatible with AT&T D-Type Channel Banks**
- **TTL-Compatible Digital Inputs and Outputs**
- **Optional Programmable Time-Slot Selection**
- **Low Operating Power Consumption:**
  Active . . . . . 230 mW Typical
  Power-Down Mode . . . . . 33 mW Typical
- **±5% Power Supplies: +12 V, +5 V, −5 V**
- **High-Reliability, Advanced N-Channel MOS Technology**
- **Low External Component Count**
- **PEP Processing Available**

TCM2909
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM2910A
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

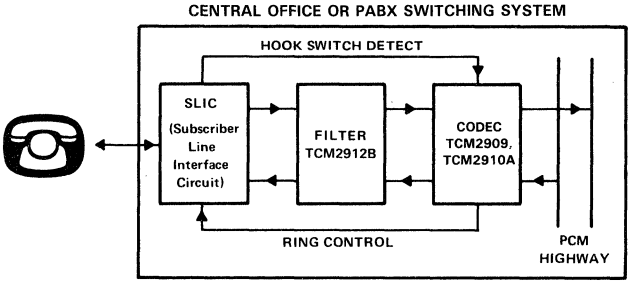
description

The TCM2909 and TCM2910A are single-chip pulse-code-modulated encoders/decoders (PCM codecs) that provide all the functions required to interface a full duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. Integrated into the codecs are circuits for signaling interface, PCM time-slot control logic, analog-to-digital (A/D) conversion, and digital-to-analog (D/A) conversion. Primary applications of the devices include:

- Line interface for digital transmission and switching of T1 Carrier, PABX, and Central Office telephone systems
- Subscriber line concentrators
- Digital encryption systems
- Digital voice-band data storage systems
- Digital signal processing

The TCM2909 and TCM2910A are characterized for operation from 0°C to 70°C.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



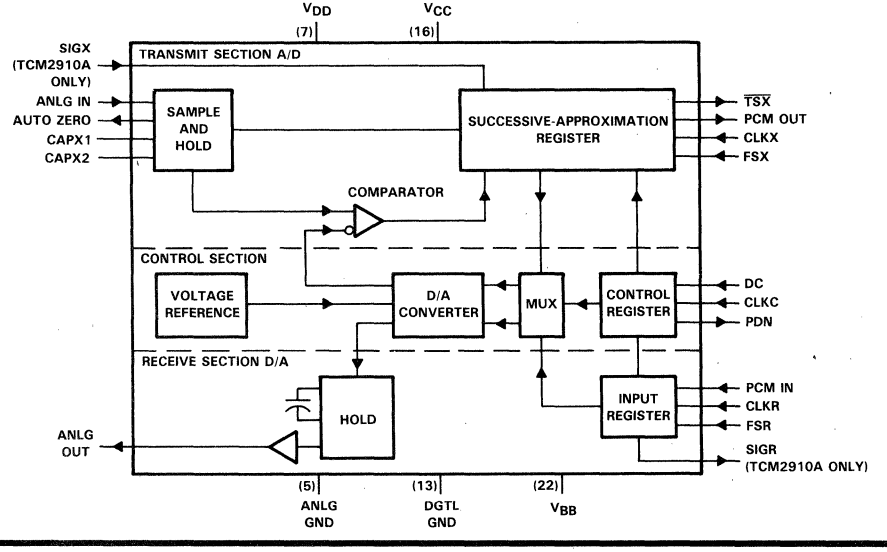
functional description

The TCM2909 and TCM2910A are designed to perform the transmit (encoding or A/D conversion) and receive (decoding or D/A) conversion) functions in a pulse-code-modulated system.

The functions of the codec are control, transmit, and receive. The control section consists of a precision voltage reference, a digital-to-analog converter, a multiplexer, and a control register. The voltage reference supplies the D/A-converter resistor ladder network with an accurate, stable reference. The analog output, in turn, is used to determine the A/D output as well as the D/A output. The control register multiplexes incoming receive and outgoing transmit data into the D/A converter.

The control section also enhances the basic codec function with programmable time-slot allocation and power-down circuits. These circuits allow dynamic allocation of both receive and transmit time slots. In small systems this feature could significantly reduce per-channel hardware for the first level of switching. In larger systems the time-slot selection circuits can be disabled, and time-slot allocation can be performed at a common system location. With either system design, the codec can be powered down during periods of inactivity, thereby significantly reducing average system power consumption.

functional block diagram



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NAME	PIN TCM2909	PIN TCM2910A	DESCRIPTION
ANLG GND	5	5	Analog return common to the transmit and receive analog circuits. Not connected to DGTL GND internally.
ANLG IN	3	3	Analog input to be encoded into a PCM word. The signal on this pin is sampled at the same rate as the transmit frame synchronization pulse, FSX, and the sample value is held in the external capacitors connected at the CAPX1 and CAPX2 pins.
ANLG OUT	9	10	Analog output. The voltage present on this pin is the decoded value of the PCM word received on PCM IN and is held constant between two conversions.
AUTO ZERO	4	4	This output is the same as the most significant bit of the encoded PCM word (5 V for negative, −5 V for positive inputs).
CAPX1	1	1	Connection for the transmit holding (analog sampling) capacitor.
CAPX2	2	2	Connection for the transmit holding (analog sampling) capacitor.
CLKC	22	24	Clock input to clock in the data on the DC pin that defines the mode of operation of the codec. When CLKC is connected to V_{CC}, DC becomes an active-low chip select. TTL-compatible.
CLKR	16	17	Clock input that defines the bit rate on the receive PCM highway (1.544 megabits per second for a T1 carrier). The maximum rate is 2.1 megabits per second at 50% duty cycle. TTL-compatible.
CLKX	18	19	Transmit clock input defining the bit rate on the transmit PCM highway. It is typically 1.544 megabits per second. Maximum rate is 2.1 megabits per second at 50% cycle. TTL-compatible.
DC	21	23	Data input to program the codec for either the direct or microcomputer mode of operation. TTL-compatible.
DGTL GND	12	13	Ground return common to the logic power supply, V_{CC}.
FSR	17	18	Frame synchronization pulse for the receive PCM highway. Resets the internal time-slot counter for the receive section. Maximum frame synchronization repetition rate is 12 kHz. Also used to differentiate between nonsignaling frames and signaling frames for the receive side. TTL-compatible.
FSX	19	20	Frame synchronization pulse for the transmit PCM highway. Resets the internal time-slot counter for the transmit section. Maximum repetition rate is 12 kHz. Also used to differentiate between nonsignaling frames and signaling frames on the transmit section. TTL-compatible.
NC	10	11	No internal connection. It is recommended that this pin be connected to ANLG GND.
NC	11	12	No internal connection. It is recommended that this pin be connected to ANLG GND.
PCM IN	7	8	Receive PCM highway (serial bus) interface. The codec serially receives a PCM word (8 bits) through this pin at the time defined by FSR, CLKR, and the contents of the receive control register.
PCM OUT	13	14	Output of the encoder onto the PCM highway. The 8-bit PCM word is serially sent out as defined by FSX, CLKX, and the control register. TTL three-state output capable of driving two TTL loads (4 mA).
PDN	8	9	Power-down output is active (high) when the codec is in the power-down state. The open-drain output is capable of sinking one TTL load (1.6 mA).
SIGR		6	Signaling output SIGR is updated with the 8th bit of the receive PCM word on signaling frames, and is latched between two signaling frames. TTL-compatible.
SIGX		21	Signaling input. This digital input is transmitted as the 8th bit of the PCM word on the PCM OUT pin in signaling frames. TTL-compatible.
$\overline{TSX}$	14	15	Normally high, the transmit time-slot output goes low while the codec is transmitting a PCM word on PCM OUT. Time-slot information is used for diagnostic purposes and also to gate the data on the PCM OUT pin to the PCM transmit highway. The open-drain output is capable of sinking two TTL loads (3.2 mA).
V_{BB}	20	22	Supply voltage (−5 V ±5%) referenced to ANLG GND.
V_{CC}	15	16	Supply voltage (5 V ±5%) referenced to DGTL GND.
V_{DD}	6	7	Supply voltage (12 V ±5%) referenced to ANLG GND.

operation

The TCM2909 and TCM2910A are capable of operating as transmitters and receivers in any of the 64 channels of a PCM system. The receive and transmit sections can be assigned to the same channel (time slot) or to different channels, and assignments can be changed under microcomputer control to meet changing system needs. Table 1 shows the control options.

TABLE 1. OPERATION CONTROL CONFIGURATIONS

CONTROL SIGNALS		OPERATION
CLKC	DC	
L	X	Undefined operation
V_{CC}	H	Power-down or standby operational status
V_{CC}	L	Direct-control operation. Receive and transmit in the first time slot.
↓	X	Microcomputer-control operation. Clock in one of 8 bits of the control word at the DC input.

Bits 1 and 2 (See Figure 3)

0	0	Load bits 3 through 8 into transmit and receive time-slot counters.
0	1	Load bits 3 through 8 into transmit counter only.
1	0	Load bits 3 through 8 into receive counter only.
1	1	Power down (Bits 3 through 8 are irrelevant).

Bits 3 through 8 for time-slot assignments 1 through 64. The time-slot numbers equal one more than the decimal equivalent represented by bits 3 (MSB) through 8 (LSB) using positive logic.

Time slot	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
1	0	0	0	0	0	0
2	0	0	0	0	0	1
•	•	•	•	•	•	•
6	0	0	0	1	0	1
•	•	•	•	•	•	•
63	1	1	1	1	1	0
64	1	1	1	1	1	1

H = high level, L = low level, see digital interface table.
X = irrelevant, ↓ = V_{CC}-to-low transition.

In microcomputer control operation, the control word at DC is divided into a mode selection (bits 1 and 2) and a time-slot assignment (bits 3 through 8). In mode 00 both the receive and transmit time-slot counters are addressed, and they both receive the same subsequent 6-bit time-slot assignment. In mode 01 the transmit time-slot counter is addressed for time-slot assignment. Mode 10 assigns a time-slot only for the receive section. Mode 11 puts the device in the standby operational status and ignores the remaining 6 bits of the control word. Specific functional considerations for microcomputer-control operation are:

- All 8 negative-going transitions of CLKC must occur within 125 microseconds for the frame rate of 8 kilobits per second. The first transition of CLKC may occur anywhere within a frame. The CLKC pin should be a TTL low level after time-slot assignment is completed.
- A dead period of 250 microseconds (2 frames) must be observed between the first positive transition of CLKC in a time-slot assignment and that of any subsequent time-slot assignment.
- It is recommended that either mode 00 or mode 01 be transmitted to the control register during power-up or system initialization to ensure that a valid time-slot is always transmitted.

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- The receive or the transmit section of the codec will operate only after both sections have been assigned a time-slot. Therefore, transmit-only and receive-only time-slot allocation is not allowed.
- Clocking the control register while the codec is active may cause an increase in idle-channel noise.

Direct-control operation is implemented by connecting the CLKC pin to +5 volts (V_{CC}) and using the DC pin as the chip select pin. When the DC pin is held low, the device transmits in the channel following FSX and receives in the channel following FSR. On the other hand, when the DC pin is held high, the device is in the power-down state. Operational considerations for direct time-slot allocation are:

- At least two framing pulses must occur after DC goes low to ensure that the codec is in direct-control status.
- Three frames (375 microseconds) are required to enter direct operation after power supply requirements are met and all clocks are available.
- After DC is brought high, two framing pulses are required to put the codec into the standby mode.
- The TCM2909 or TCM2910A can replace a 2910 codec even though the CLKC characteristics are not the same for the two devices.

encoding mode

The analog input signal sampled at the ANLG IN pin is held by an external capacitor on pins CAPX1 and CAPX2. This sampling is done synchronously with the transmit time-slot assigned to the device. The eight-bit digital PCM word will be transmitted on the PCM OUT pin in the frame immediately following the frame in which the analog signal was sampled. See Table 3.

decoding mode

When the assigned receive time-slot occurs, the eight-bit digital PCM word is retrieved from the PCM highway on the PCM IN pin. The word is converted from digital to analog and held with an internal capacitor until the next assigned receive time-slot update. See Table 3.

signaling

These devices are compatible with per-channel signaling and are capable of differentiating between the signaling and nonsignaling frames. A signaling frame is one in which the eighth bit of the PCM word contains signaling information while the seven most significant bits are normal information bits. The signaling frame is designated by the framing pulse (FSX or FSR) whose length is extended to two full clock periods as shown in the timing diagrams. A framing pulse of a nonsignaling frame is one full clock period in length. During a transmit signaling frame, the level present on the SIGX pin (of the TCM2910A) is substituted for the 8th bit of the PCM word. During a receive signaling frame the value of the 8th bit of the PCM word of the receive channel will be put on the SIGR pin (of the TCM2910A) and the signal level will remain unchanged until it is updated by the next signaling frame. The remaining 7 bits will be decoded according to the procedure in CCITT Recommendation G.733. See Figure 1 and Figure 2 for transmit and receive timing diagrams.

framing

These devices are compatible with the D3/D4 framing format (T1 framing), which inserts a 193rd bit after the 24th serial channel (8 bits per channel) frame. The extra bit raises the clock frequency (CLKX and CLKR) from 1.536 MHz to 1.544 MHz.

standby operation

The codec provides for powering down to standby status from both microcomputer-control and direct-control operation. The power consumption is reduced from 230 mW to 33 mW. Standby operation results in the powering down of all the codec functions except the DC, CLKC, SIGX†, SIGR†, and PDN inputs. Also, PCM OUT is forced into a high-impedance state thus helping to ensure that the PCM bus will not be driven. The SIGR† output is held low to provide a known condition until changed by a signaling frame after reactivation.

In microcomputer-control operation, the power-down state is invoked by clocking in 11 at the DC inputs as described in Table 1. In direct operation the power-down state is called by taking the DC pin high and connecting clock CLKC pin to V_{CC}. Recovery from the power-down condition is accomplished by forcing DC to the low level and allowing at least 2 frame synchronization pulses to occur.

internal reset

The TCM2909 and TCM2910A are designed to aid the user by eliminating certain system power-interruption problems. Three of the most common of these problems are:

(1) Plugging a card into a "hot" system thus causing spikes on the common power supplies
(2) Various transients such as caused by duplicated power supply faults or power feeder faults
(3) Transients and spikes that result from turning the power supplies on.

These devices are tolerant of transients in the negative power supply (V_{BB}) provided that V_{BB} remains more negative than −3.5 volts. The device will go into the power-down (standby) status if, during power up (single-card or system), V_{CC} or V_{DD} is supplied after V_{BB} or if a transient causes the positive power supplies to drop below approximately 2 volts. Since $\overline{TSX}$ is inhibited in standby operation, any codec in this status can be detected easily.

companding

The amplitude distribution of a speech message is not uniform. Moreover, the probability of occurrence for a small amplitude is greater than the probability for large amplitudes. Advantage can be taken of this fact by "compressing" digital resolution into the lower signal amplitude during transmission and "expanding" the signal upon the reception, thus increasing the overall signal-to-noise ratio. CCITT has defined this function and entitled it the μ-law.

$$f(x) = \text{sgn}(x)\,\frac{\ln + [1 + \mu|x|]}{\ln (1 + \mu)} \quad \text{for: } -1 \leq x \leq 1$$

where $\mu = 255$, x is the normalized input, and sgn(x) is the sign of x. A continuous implementation of f(x) would be impossible, therefore a piecewise continuous approximation of f(x) is used. The approximation divides the function into 16 segments, and each segment is divided into 16 equal intervals except for the first interval of the first segment. Refer to CCITT Recommendation G.711 for the segment and interval implementation details of the μ-law used for these circuits.

† TCM2910A only

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absolute maximum ratings

V_{CC}, V_{DD}, ANLG GND, and DGTL GND with respect to V_{BB} . . . . . −0.3 V to 20 V
All inputs and outputs with respect to V_{BB} . . . . . −0.3 V to 20 V
Temperature under bias . . . . . −10°C to 80°C
Storage temperature range . . . . . −65°C to 150°C

NOTE: Stresses in excess of absolute maximum ratings may permanently damage the device. Functional operation outside the recommended operating conditions is not guaranteed. Prolonged exposure to absolute maximum ratings may have an adverse effect on device characteristics.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)	11.4	12	12.6	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Ground voltages (ANLG GND and DGTL GND)		0		V
Auto-zero resistor, R1 (see Figures 9 and 10)			150	kΩ
Auto-zero resistor, R2 (see Figures 9 and 10)			330	Ω
Auto-zero resistor, R3 (see Figures 9 and 10)			470	kΩ
Analog coupling capacitor, C1 (see Figures 9 and 10)			0.1	μF
Analog coupling capacitor, C2 (see Figure 10)			0.3	μF
Analog sampling capacitor, CAPX, for 8-kHz sampling rate (see Figures 9 and 10)	1600	2000	2400	pF
Operating free-air temperature, T_A	0		70	°C

NOTE 1: Voltages at the analog input, analog output, and V_{DD} terminals are with respect to the analog ground terminal. All other voltages are referenced to the digital ground terminal unless otherwise noted.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.6	V
I_{IH}	High-level input current		V_I = 5.5 V		10	μA
I_{IL}	Low-level input current		V_I = 0 V		−10	μA
V_{OH}	High-level output voltage (see Note 2)	PCM OUT	I_{OH} = 15 mA	2.4		V
		SIGR†	I_{OH} = 80 μA	2.4		
V_{OI}	Low-level output voltage	PCM OUT	I_{OL} = 4 mA		0.4	V
		SIGR†	I_{OL} = 0.5 mA		0.4	
		PDN	I_{OL} = 1.6 mA		0.4	
		$\overline{TSX}$	I_{OL} = 3.2 mA		0.4	

analog interface

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Analog-input impedance (between ANLG IN and CAPX1) in series with CAPX to ANLG GND during sampling of ANLG IN	V_I = −3.1 V to 3.1 V	125	300	500	Ω
Small-signal impedance at ANLG OUT	V_O = −3.1 V to 3.1 V	100	180	300	Ω
Decoder output offset voltage	Serial 11111111 to PCM IN	−50		50	mV
Encoder input offset voltage (see Note 3)	Serial 11111111 from PCM OUT	−5	1.5	5	mV
Peak negative output voltage at auto zero§	400 kΩ to ANLG GND	V_{BB}+2	V_{BB}		V
Peak positive output voltage at auto zero		V_{CC}−2	V_{CC}		V

power supplies

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{DD1}	V_{DD} standby current	V_{DD} = 12.6 V, V_{CC} = 5.25 V, V_{BB} = −4.75 V, f_{CLK} = 2.048 MHz, See Note 4		0.7	1.1	mA
I_{CC1}	V_{CC} standby current			4	7	mA
I_{BB1}	V_{BB} standby current			−1.4	−2.5	mA
I_{DD2}	V_{DD} operating current			11	16	mA
I_{CC2}	V_{CC} operating current			13	21	mA
I_{BB2}	V_{BB} operating current			−4	−7.5	mA

† TCM2910A only.
‡ Typical values are at V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.
§ Limits are expressed as magnitudes. For example, if V_{BB} = −5 V, the typical value is −5 V and the minimum value is −3 V.

NOTES: 2. PDN and $\overline{TSX}$ outputs are open-drain n-channel transistors that only sink current to DGTL GND. External pull-up devices are required to source current.
3. External auto-zero must be used when the required input offset is less than ±4 code steps or approximately 2.7 mV. The external auto-zero circuit shown in Figure 10 will bias the codec at the zero-crossing point and reduce the input offset voltage to zero.
4. These measurements apply to the microcomputer and direct modes. All output pins are left open, the dc input (pin 23) is at 5 V for standby current and at 0 V for operating current. All other input pins are grounded with the clocks operating.

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operating characteristics over recommended ranges of supply voltages and operating free-air temperature, R_L = 600 Ω (unless otherwise noted)

gain and dynamic range

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Digital milliwatt response	Nominal supply voltages, T_A = 25°C, See Note 5 and Figure 6	5.53	5.63	5.73	dBm
Temperature coefficient of digital milliwatt response	Nominal supply voltages, See Note 5		−0.001	−0.002	dB/°C
Change in digital milliwatt response	Supply voltages changing ±5%, T_A = 25°C, See Note 5			±0.07	dB
RMS input dynamic voltage range using dc and ac tests	Nominal supply voltages, T_A = 25°C, See Note 6 and Figure 6	2.17	2.20	2.23	V
Temperature coefficient of RMS input dynamic voltage range	Nominal supply voltages, See Note 6			−0.5	mV/°C
Change in RMS input dynamic voltage range	Supply voltages changing ±5%, T_A = 25°C, See Note 6			±18	mV
RMS output dynamic voltage range	Nominal supply voltages, T_A = 25°C	2.13	2.16	2.19	V
Temperature coefficient of RMS output dynamic voltage range	Nominal supply voltages			−0.5	mV/°C
Change in RMS output dynamic voltage range	Supply voltages changing ±5%, T_A = 25°C			±18	mV
Self-loop gain	P_I = 0 dBm0 at 1.02 kHz, See Note 7 and Figure 5		−0.2		dB

† Typical values are at V_{DD} = 12 V, V_{CC} = 5 V, V_{BB} = −5 V, and T_A = 25°C.

NOTES: 5. The input to PCM IN is a repetitive digital word sequence specified in CCITT Recommendation G.711. Measurement is made at ANLG OUT. Limits are not corrected for (six x)/x degradation and no C-message-weighted filter is used. See Table 2.

6. In the dc procedure, the positive and negative clipping levels are measured and dynamic voltage range is calculated. In the ac procedure, a sinusoidal input signal to ANLG IN is used and input dynamic voltage range is measured directly.

7. The codec acts as both encoder and decoder (PCM OUT = PCM IN) in a digital loop-back configuration. Specified gain is in addition to normal (sin x)/x insertion loss. See Note 8.

8. In the term (sin x)/x

$$x = \pi \frac{\text{measurement frequency}}{\text{sampling frequency}}$$

gain tracking error at f = 1.02 kHz

PARAMETER	TEST CONDITIONS	MOST NEG.	MOST POS.	UNIT
End-to-end gain tracking error (see Figure 4)	P_I = −37 dBm0 to 0 dBm0	−0.4	0.4	dB
	P_I = −50 dBm0 to −37 dBm0	−0.8	0.8	
	P_I = −55 dBm0 to −50 dBm0	−2.4	2.4	
Half-channel gain tracking error (encoder only with ideal decoder) See Figure 6	P_I = −37 dBm0 to 0 dBm0	−0.3	0.3	dB
	P_I = −50 dBm0 to −37 dBm0	−0.9	0.9	
	P_I = −55 dBm0 to −50 dBm0	−1.5	1.5	
Half-channel gain tracking error (decoder only with ideal encoder) See Figure 6	P_I = −37 dBm0 to 0 dBm0	−0.3	0.3	dB
	P_I = −50 dBm0 to −37 dBm0	−0.9	0.9	
	P_I = −55 dBm0 to −50 dBm0	−1.5	1.5	

operating characateristics over recommended ranges of supply voltages and operating free-air temperature, R_L = 600 Ω (unless otherwise noted) (continued)

transmission characteristics (see Figure 6), f = 1.02 kHz (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
Signal-to-total-distortion ratio, C-message weighting, end-to-end			See Figure 7		
Signal-to-total-distortion ratio, C-message weighting, (half-channel)			See Figures 6 & 7		
Harmonic distortion (2nd or 3rd overtone) measured at ANLG OUT, P_I = 0 dBm0 See Figure 6.			−48	−44	dB
Encoder idle-channel noise measured at mid-tread (no quantizing noise) C-message weighting with no signaling	No external auto zero See Figure 9		2	10	dBrnc0
	With external auto zero See Figure 10		8		
Encoder idle-channel noise measured at the riser (quantizing noise included) C-message weighting, no signaling				17	dBrnc0
Encoder idle-channel noise measured at mid-tread (no quantizing noise), C-message weighting, 6th and 12th frame signaling per AT&T System requirements	No external auto zero See Figure 9		10	13	dBrnc0
	With external auto zero See Figure 10		13		
Decoder idle-channel noise, no sign-bit toggling, no signaling, quiet code (serial 11111111 to PCM IN)			−10	7	dBrnc0
Decoder idle-channel noise with sign-bit toggling, no signaling, quiet code (serial 11111111 to PCM IN)			13	17	dBrnc0

power supply rejection and crosstalk attenuation

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
SVRR1	V_{DD} supply voltage rejection ratio	Decoder alone,	See Note 9	45	55		dB
SVRR2	V_{BB} supply voltage rejection ratio	Decoder alone,	See Note 9	35	38		dB
SVRR3	V_{CC} supply voltage rejection ratio	Decoder alone,	See Note 9	50	80		dB
SVRR4	V_{DD} supply voltage rejection ratio	Encoder alone		50	75		dB
SVRR5	V_{BB} supply voltage rejection ratio	Encoder alone		45	70		dB
SVRR6	V_{CC} supply voltage rejection ratio	Encoder alone		50	85		dB
SVRR7	V_{DD} supply voltage rejection ratio	Self loop,	See Note 10	40	50		dB
SVRR8	V_{BB} supply voltage rejection ratio	Self loop,	See Note 10	35	38		dB
SVRR9	V_{CC} supply voltage rejection ratio	Self loop,	See Note 10	50	80		dB
a_x	Crosstalk attenuation	See Figure 8,	See Note 11	75	>80		dB

clock timing requirements over recommended ranges of operating conditions (see Note 12)

	PARAMETER	MIN	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	485		ns
t_r, t_f	Rise and fall times for CLKX, CLKR, and CLKC		5	30	ns
$t_{w(CLK)}$	Clock pulse duration for CLKX, CLKR, and CLKC	215		ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	45		55	%

† Typical values are for T_A = 25°C and nominal power supply voltages.

NOTES:
9. With the test device acting as a decoder, a 200-mV peak-to-peak, 1,02 kHz signal is applied to the appropriate supply pin and measurements are made at the remote encoder output with the decoder in idle-channel conditions.
10. With the test device acting as encoder and decoder, a 200-mV peak-to-peak, 1.02-kHz signal is applied to the appropriate supply pin and measurements are made at the decoder output with the encoder in idle-channel conditions.
11. The analog input power is 0 dBm0 at 1.02 kHz and the decoder is under idle-channel conditions. Measurement is made at ANLG OUT.
12. All timing parameters are referenced to 2 V except t_{pd3} and t_{pd5}, which reference a high-impedance state.

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transmit timing requirements over recommended ranges of operating conditions (see Note 12)

PARAMETER		MIN	MAX	UNIT
$t_{conv(X)}$	Analog input conversion time referenced to leading edge of transmit time slot (see Note 13)	20		time slots
$t_{d(FSX)}$	Frame sync delay time	20	150	ns
$t_{su(SIGX)}$	Setup time before Bit 7 falling edge	0		ns
$t_{h(SIGX)}$	Hold time after Bit 8 falling edge	100		ns

receive timing requirements over recommended ranges of operating conditions (see Note 12)

PARAMETER		MIN	MAX	UNIT
$t_{conv(R)}$	Analog output update from leading edge of the channel time slot	7 1/16		time slots
$t_{d(FSR)}$	Frame sync delay time	20	150	ns
$t_{su(PCM\ IN)}$	Receive data setup time	20		ns
$t_{h(PCM\ IN)}$	Receive data hold time	60		ns

control (microcomputer operation) timing requirements over recommended ranges of operating conditions

PARAMETER		MIN	MAX	UNIT
$t_{su(DC)}$	Control data setup time	100		ns
$t_{h(DC)}$	Control data hold time	100		ns

propagation delay times over recommended ranges of operating conditions (see Note 12 and timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock Bit 1 to Bit 1 data valid at PCM OUT (data enable time on time-slot entry)	C_L = 0 to 100 pF	50	180	ns
t_{pd2}	From falling edge of transmit clock Bit n to Bit n+1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	80	230	ns
t_{pd3}	From falling edge of transmit clock Bit 8 to Bit 8 Hi-Z at PCM OUT (data float time on time-slot exit)	C_L = 0, See Note 13	75	245	ns
t_{pd4}	From rising edge of transmit clock Bit 1 to $\overline{TSX}$ active (low) (time-slot enable time)	C_L = 0 to 100 pF	30	220	ns
t_{pd5}	From falling edge of transmit clock Bit 8 to $\overline{TSX}$ inactive (high) (time-slot disable time)	C_L = 0, See Note 13	70	225	ns
t_{pd6}	From falling edge of receive clock Bit 8 on signaling frames to updated signaling bit on SIGR output (receive signaling update time)			1000	ns

NOTES: 12. All timing parameters are referenced to 2 V except t_{pd3} and t_{pd5}, which reference a high-impedance state.
13. The 20-time-slot minimum ensures that the complete A/D conversion will take place under any combination of receive interrupt of asynchronous operation of the codec. If only the transmit channel is operated, the A/D conversion can be completed in a minimum of 11 time slots.

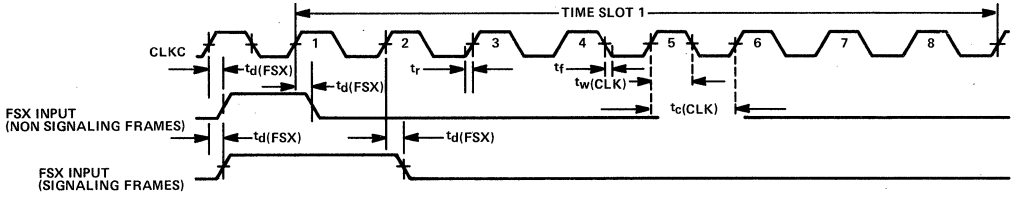

FIGURE 1a. TRANSMIT FRAME SYNCHRONIZATION TIMING

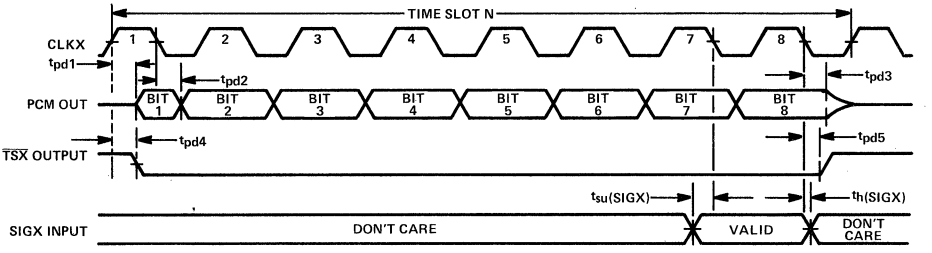

FIGURE 1b. TRANSMIT OUTPUT TIMING

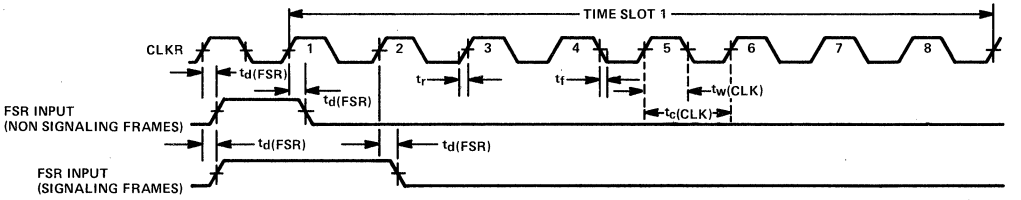

FIGURE 2a. RECEIVE FRAME SYNCHRONIZATION TIMING

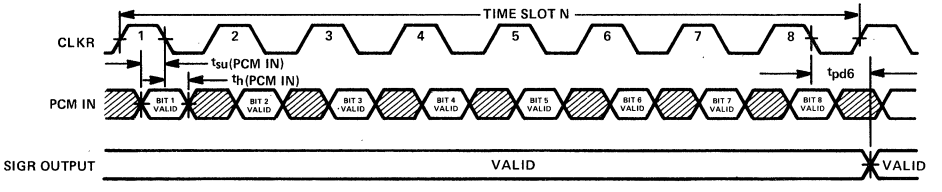

FIGURE 2b. RECEIVE INPUT TIMING

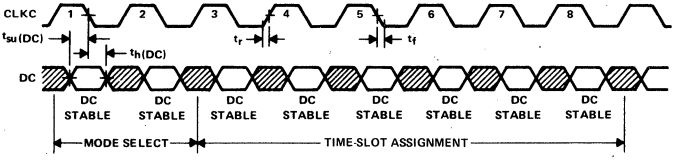

FIGURE 3. CONTROL TIMING

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PARAMETER MEASUREMENT INFORMATION

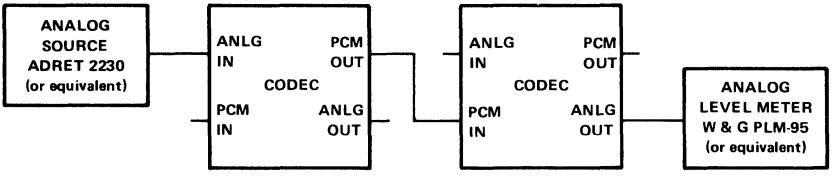

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FIGURE 4. END-TO-END GAIN TEST CIRCUIT

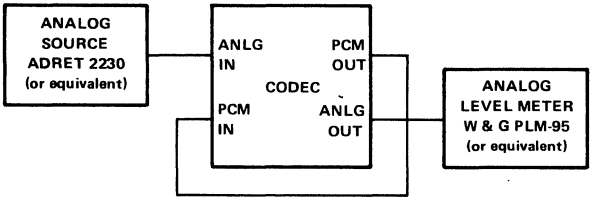

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FIGURE 5. SELF-LOOP GAIN TEST CIRCUIT

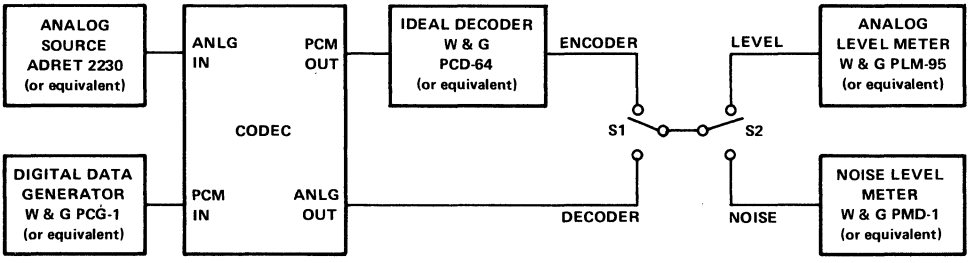

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FIGURE 6. TRANSMISSION PARAMETER TEST CIRCUIT

PARAMETER MEASUREMENT INFORMATION

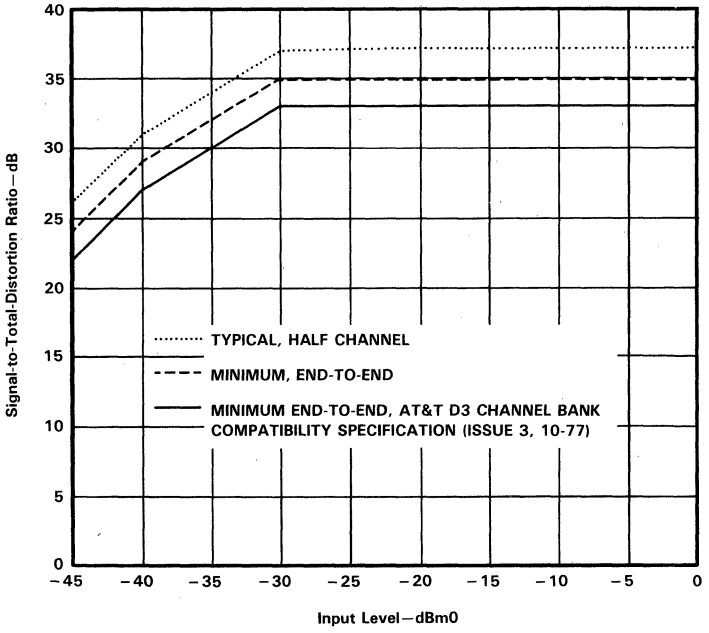

FIGURE 7. SIGNAL-TO-TOTAL DISTORTION RATIO

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PARAMETER MEASUREMENT INFORMATION

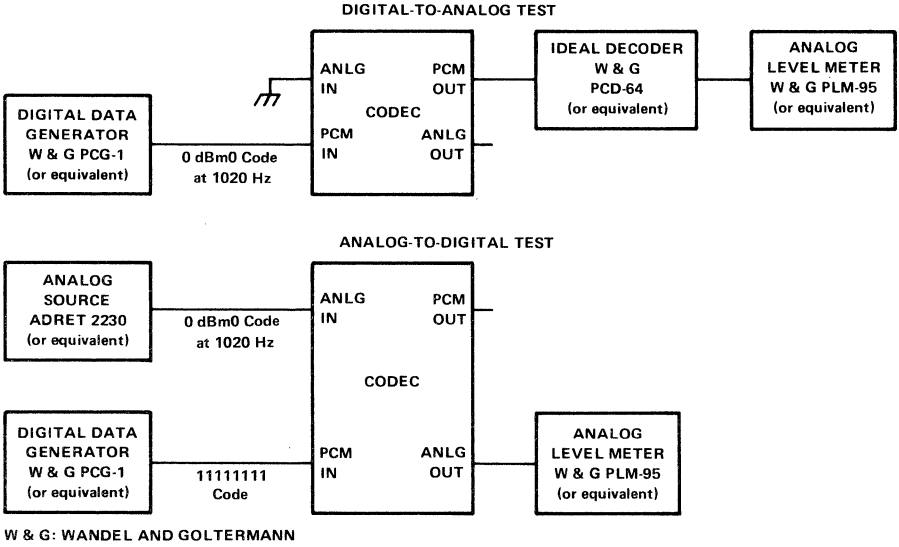

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FIGURE 8. CROSSTALK ATTENUATION TEST CIRCUIT

TABLE 2. μ-LAW DIGITAL WORD SEQUENCE FOR THE DIGITAL MILLIWATT RESPONSE PER CCITT RECOMMENDATION G.711

		Bit Number							
		1	2	3	4	5	6	7	8
Word Number	1	0	0	0	1	1	1	1	0
	2	0	0	0	0	1	0	1	1
	3	0	0	0	0	1	0	1	1
	4	0	0	0	1	1	1	1	0
	5	1	0	0	1	1	1	1	0
	6	1	0	0	0	1	0	1	1
	7	1	0	0	0	1	0	1	1
	8	1	0	0	1	1	1	1	0

TYPICAL APPLICATION INFORMATION

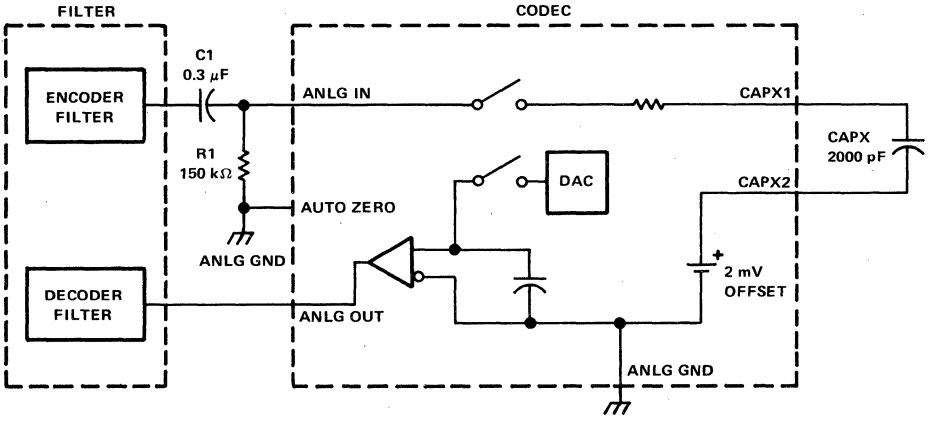

FIGURE 9. ANALOG INTERFACE WITHOUT EXTERNAL AUTO ZERO

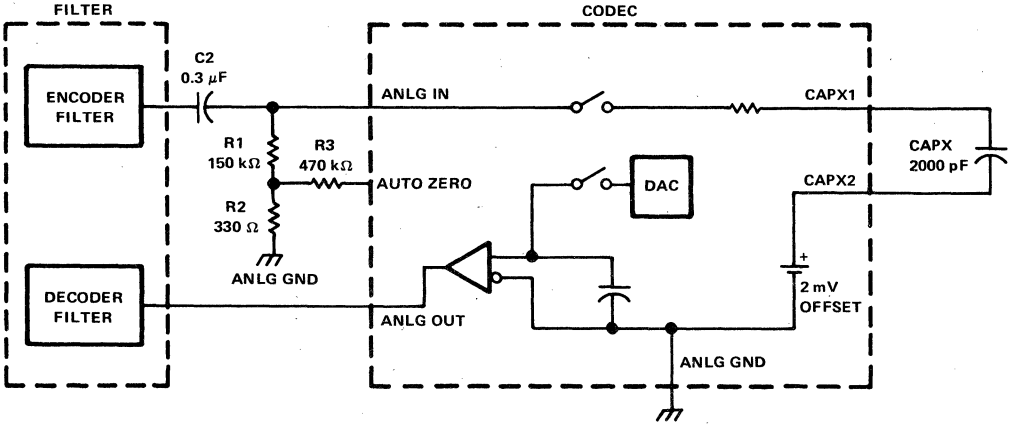

FIGURE 10. ANALOG INTERFACE WITH EXTERNAL AUTO ZERO

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TYPICAL APPLICATION INFORMATION

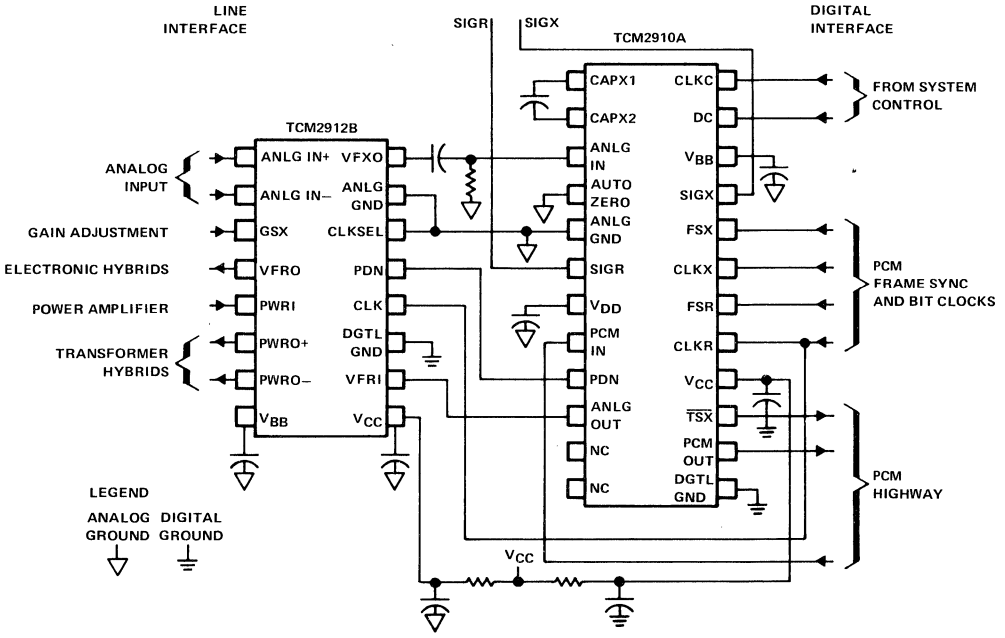

FIGURE 11. TCM2910A INTERFACE WITH TCM2912B FILTER

TABLE 3a. μ-LAW POSITIVE INPUT VALUES
Reproduced from CCITT† (Volume III — 2 on Line Transmission) Recommendation G.711 on Pulse Code Modulation of Voice Frequencies

1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note A)	Character signal (see Note B) Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (see Note C)	Decoder output value number
		8159	$(128)^D$	(8159)			
					1 0 0 0 0 0 0 0	8031	127
			127	7903			
8	16 × 256				(see Note E)		
			113	4319			
					1 0 0 0 1 1 1 1	4191	112
		4063	112	4063			
7	16 × 128				(see Note E)		
			97	2143			
					1 0 0 1 1 1 1 1	2079	96
		2015	96	2015			
6	16 × 64				(see Note E)		
			81	1055			
					1 0 1 0 1 1 1 1	1023	80
		991	80	991			
5	16 × 32				(see Note E)		
			65	511			
					1 0 1 1 1 1 1 1	495	64
		479	64	479			
4	16 × 16				(see Note E)		
			49	239			
					1 1 0 0 1 1 1 1	231	48
		223	48	223			
3	16 × 8				(see Note E)		
			33	103			
					1 1 0 1 1 1 1 1	99	32
		95	32	95			
2	16 × 4				(see Note E)		
			17	35			
					1 1 1 0 1 1 1 1	33	16
		31	16	31			
	15 × 2				(see Note E)		
			2	3			
1					1 1 1 1 1 1 1 0	2	1
	1 × 1		1	1	1 1 1 1 1 1 1 1		
			0	0		0	0

NOTES: A. 8159 normalized value units correspond to the value of the on-chip voltage reference.
B. The PCM word on the highways is the same as the one shown in column 6.
C. The voltage output on the ANLG OUT lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.
D. X_{128} is a virtual decision value.
E. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.

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TABLE 3b. μ-LAW NEGATIVE INPUT VALUES
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1	2	3	4	5	6	7	8
Segment number	Number of intervals × interval size	Value at segment end points	Decision value number n	Decision value x_n (see Note A)	Character signal (see Note B) — Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (see Note C)	Decoder output value number
↑			0	0		0	0
	1 × 1		1	−1	0 1 1 1 1 1 1 1		
1			2	−3	0 1 1 1 1 1 1 0	−2	1
	15 × 2				(see Note D)		
		−31	16	−31			
			17	−35	0 1 1 0 1 1 1 1	−33	16
2	16 × 4				(see Note D)		
		−95	32	−95			
			33	−103	0 1 0 1 1 1 1 1	−99	32
3	16 × 8				(see Note D)		
		−223	48	−223			
			49	−239	0 1 0 0 1 1 1 1	−231	48
4	16 × 16				(see Note D)		
		−479	64	−479			
			65	−511	0 0 1 1 1 1 1 1	−495	64
5	16 × 32				(see Note D)		
		−991	80	−991			
			81	−1055	0 0 1 0 1 1 1 1	−1023	80
6	16 × 64				(see Note D)		
		−2015	96	−2015			
			97	−2143	0 0 0 1 1 1 1 1	−2079	96
7	16 × 128				(see Note D)		
		−4063	112	−4063			
			113	−4319	0 0 0 0 1 1 1 1	−4191	112
8	16 × 256				(see Note D)		
			126	−7647	0 0 0 0 0 0 0 1	−7775	126
			127	−7903	0 0 0 0 0 0 0 0	−8031	127
		−8159	(128)E	(−8159)			

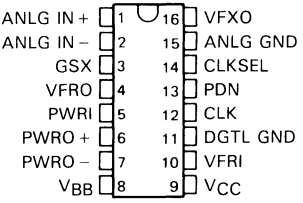
NOTES: A. 8159 normalized value units correspond to the value of the on-chip voltage reference.
B. The PCM word on the highways is the same as the one shown in column 6.
C. The voltage output on the ANLG OUT lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.
D. The PCM word corresponding to positive input values between two successive decision values numbered n and n + 1 (see column 4) is (255 − n) expressed as a binary number.
E. X_{128} is a virtual decision value.

†The International Telegraph and Telephone Consultative Committee. Published by the International Telecommunication Union, Geneva, Switzerland.

D2788, SEPTEMBER 1983—REVISED MAY 1986

- High-Pass Transmit Filter for Rejection of All Low-Frequency Noise:
  - 16 Hz . . . . . 70 dB Typical
  - 50 Hz . . . . . 35 dB Typical
  - 60 Hz . . . . . 30 dB Typical
- 6th-Order Low-Pass Transmit Filter for Improved Performance
- Low Standby Power Consumption
- Improved Envelope Delay Characteristics
- Excellent Power Supply Rejection Ratio
- CCITT G.712 as well as AT&T D3/D4 Compatible
- TTL- and CMOS-Compatible
- Reliable N-Channel MOS Process
- Pin-For-Pin Functional Replacement for Intel 2912A
- TCM2912C Offers Improved Noise Performance
- TCM2912C — Three-State PWRO+ and PWRO− Outputs

J
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NOTE

TCM2912B IS NOT RECOMMENDED FOR NEW DESIGN.

FOR NEW DESIGN REFER TO TCM2912C.

description

The TCM2912B and TCM2912C are monolithic integrated circuits designed to implement the transmit and receive signal filters of a PCM line or trunk termination. The transmit and receive passband filter sections are implemented using switched capacitor techniques.

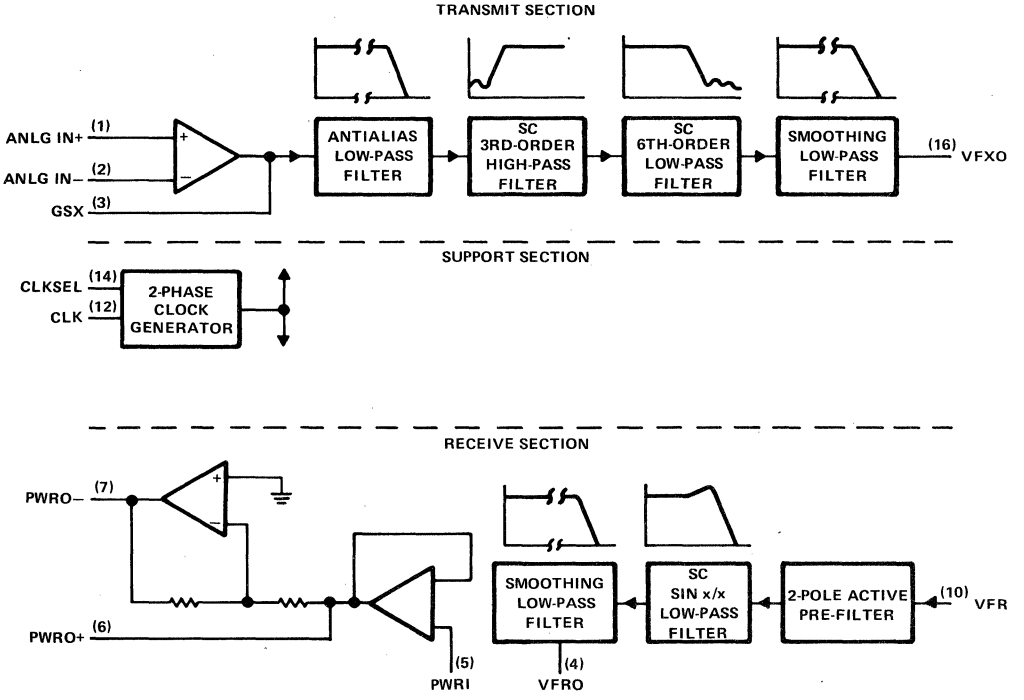
The TCM2912B and TCM2912C are primarily used in telephone system applications for switching, transmission, and remote concentration. The transmit section provides a high-pass filter to ensure rejection of all low-frequency noise as well as the anti-aliasing function required for an 8 kHz sampling system. A sixth-order low-pass filter is provided in the transmit section for improved performance. The receive section has a smoothing low-pass filter and sin x/x correction required for interface with TCM2910A or TCM2911A codecs. The TCM2912B and TCM2912C eliminate high-frequency switching noise for direct interface with transformer or electronic hybrids. The power-down mode (standby) can be directly controlled by TCM2910A or TCM2911A type codecs. In the power-down mode (standby), the TCM2912B VFXO, GSX, and VFRO outputs are in a high-impedance state and the PWRO+ and PWRO− outputs are in a low-impedance state to V_{CC}. When the TCM2912C is in the power-down mode, all outputs are in a high-impedance state.

The -3 versions are identical to the standard versions except that gain relative to gain at 1 kHz is −0.7 dBm minimum.

The TCM2912B and TCM2912C are characterized for operation from 0°C to 70°C.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

system block diagram



The TCM2912B and TCM2912C system block diagram is divided into three sections: transmit, receive, and support. The transmit section provides bandpass filtering to eliminate unwanted switching and low-frequency noise signals. The receive section provides a 2-pole active pre-filter to filter out high-frequency components that are present on the analog output of the codec. Since the filter is a sampled data system, the components could alias down into the voice band and create low-frequency gain tracking and S/Q problems. Following the pre-filter is a sixth-order low-pass filter that provides sin x/x correction for the codec. The receive section provides sin x/x correction for the codec and elimination of high-frequency switching signals. The receive section has optional output buffers. The support section provides clock generation.

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PIN NAME	NO.	DESCRIPTION
ANLG GND	15	Analog return common to the transmit and receive analog circuits. Not connected to DGTL GND internally.
ANLG IN−	2	Inverting input of the gain adjustment operational amplifier on the transmit filter
ANLG IN+	1	Analog input of the transmit filter. The ANLG IN+ signal comes from the 2- to 4-wire hybrid in the case of a 2-wire line and goes through the high-pass filter and antialiasing filter before being sent to the codec for encoding.
CLK	12	Clock input. Three clock frequencies can be used: 1.536 MHz, 1.544 MHz, or 2.048 MHz. Frequency is selected by CLKSEL (pin 14).
CLKSEL	14	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency at pin 12 (CLK). When tied to V_{BB}, CLK is 1.536 MHz. When tied to ground, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 2.048 MHz.
DGTL GND	11	Digital ground return for internal clock generator.
GSX	3	Output of the gain adjustment operational amplifier on the transmit filter. Used for gain setting of the transmit filter.
PDN	13	Control input for standby power-down mode. An internal pullup to 5 volts is provided for interface to the codec PDN outputs.
PWRI	5	High-impedance input to the power driver amplifiers on the receive side of interface to transformer hybrids. When taken to the low level (tied to V_{BB}), the power amplifiers are powered down.
PWRO−	7	Inverting side of power amplifiers. Power driver output capable of directly driving transformer hybrids.
PWRO+	6	Noninverting side of the power amplifiers. Power driver output capable of directly driving transformer hybrids.
V_{BB}	8	−5 V ±5% referenced to ANLG GND
V_{CC}	9	5 V ±5% referenced to ANLG GND
VFRI	10	Analog input of the receive filter, interface to the codec analog output for PCM applications. The receive filter provides the sin x/x correction needed for sample-and-hold-type codec outputs to give unity gain. The input voltage range is directly compatible with TCM2910A and 2911A type codecs.
VFRO	4	Analog output of the receive filter. Provides a direct interface to electronic hybrids. For a transformer hybrid application, VFRO is tied to PWRI and a dual balanced output is provided on pins PWRO+ and PWRO−.
VFXO	16	Analog output of the transmit filter. The output voltage range is directly compatible with the TCM2910A and TCM2911A type codecs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 14 V
Output voltage, V_O all outputs (see Note 1) . . . . . −0.3 V to 14 V
Output current, I_O (all outputs) . . . . . ±50 mA
Continuous total dissipation at 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. Voltage values are with respect to V_{BB}.
2. For operation above 25°C free-air temperature, derate linearly to 880 mW at 70°C at the rate of 11 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage (see Note 3)		−4.75	−5	−5.25	V
–	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage	All inputs except CLKSEL	2.2			V
V_{IL}	Low-level input voltage	All inputs except CLKSEL and PWRI			0.8	V
		PWRI	V_{BB}		$V_{BB}+0.5$	
	Clock select input voltage	For 2.048 MHz	$V_{CC}-0.5$		V_{CC}	V
		For 1.544 MHz	ANLG GND − 0.5		0.8	
		For 1.536 MHz	V_{BB}		$V_{BB}+0.5$	
R_L	Load resistance	At GSX, VFXO, or VFRO	10			kΩ
		At PWRO+ or PWRO− (single-ended)	300			Ω
		At PWRO+ and PWRO− (differential)	600			
C_L	Load capacitance	At GSX, VFXO, or VFRO			25	pF
		At PWRO+ or PWRO− (single-ended)			100	
		At PWRO+ and PWRO− (differential)			200	
T_A	Operating free-air temperature		0		70	°C

NOTE 3: Voltages at analog inputs, analog outputs, V_{CC}, and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

digital interface

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_I	Input current	PDN	V_I = GND to V_{CC}		−100	μA
		CLKSEL	V_I = V_{BB} to 2.2 V		1	
		CLK	V_I = 0.8 V to 2.2 V		1	

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

supply current

PARAMETER			TEST CONDITIONS	TCM2912B			TCM2912C			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC}	Supply current from V_{CC}	Standby	PDN at 2.2 V			0.2			0.4	mA
		Operating	Power amplifiers active		10	15		12	15	
		Operating	Power amplifiers inactive, PWRI at V_{BB}		7	9		9	11	
I_{BB}	Supply current from V_{BB}	Standby	PDN = 2.2 V			−0.2			−0.4	mA
		Operating	Power amplifiers active		−10	−15		−12	−15	
		Operating	Power amplifiers inactive, PWRI at V_{BB}		−7	−9		−9	−11	

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input leakage current at ANLG IN+, ANLG IN−	V_I = −2.2 V to 2.2 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN−				±25	mV
Output voltage swing at GSX	R_L = 10 kΩ	±2.5			V
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −1.6 V to 1.6 V (−3 dBm0)	60			dB
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −2.2 V to 2.2 V (0 dBm0)	60	90		dB
DC open-loop voltage amplification at GSX		72	77		dB
Open-loop unity gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

transmit filter

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
DC output offset voltage at VFXO	ANLG IN+ connected to ANLG GND, Amplifiers at unity gain			±100	mV
Output voltage swing at 1 kHz at VFXO	RL ≥ 10 kΩ	±3.2			V
Output resistance at VFXO			1	2	Ω

receive filter

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
DC output offset voltage at VFRO	VFRI connected to ANLG GND			±100	mV
Output voltage swing at VFRO	R_L = 10 kΩ	±3.2			V
Input leakage current at VFRI	V_I = −3.2 V to 3.2 V			1	μA
Input resistance at VFRI		1			MΩ
Output resistance at VFRO			1	2	Ω

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

receive filter driver amplifier

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Output voltage across R_L at PWRO+, PWRO−	Single ended connection, R_L connected to ANLG GND	R_L = 10 kΩ	±3.2			V
		R_L = 600 Ω	±2.9			
		R_L = 300 Ω	±2.5			
Differential output voltage swing at PWRO+, PWRO−	Balanced connection, R_L connected between PWRO+ and PWRO−	R_L = 20 kΩ	±6.4			V
		R_L = 1200 Ω	+5.8			
		R_L = 600 Ω	+5			
DC output offset voltage at PWRO+, PWRO−	PWRI connected to ANLG GND				±50	mV
Input leakage current at PWRI	V_I = −3.2 V to 3.2 V				±0.5	μA
Input resistance at PWRI			10			MΩ
Output resistance at PWRO+, PWRO−	$I_O \leq 10$ mA, V_O = −3 V to 3 V			1	2	Ω

power supply rejection (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SVRR1	V_{CC} supply voltage rejection ratio	Transmit channel only	30	45		dB
SVRR2	V_{BB} supply voltage rejection ratio	Transmit channel only	30	45		dB
SVRR3	V_{CC} supply voltage rejection ratio	Receive channel only	30	45		dB
SVRR4	V_{BB} supply voltage rejection ratio	Receive channel only	30	45		dB

† All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: With the test device acting as a transmitter (or receiver), a 200-mV peak-to-peak 1.02-kHz signal is applied to the appropriate supply pin and measurements are made at the VFXO (or VFRO) output with the receiver (or transmitter) and power amplifiers in idle channel conditions.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

transmit filter transfer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Gain relative to gain at 1 kHz with 0-dBm0 input signal		Gain-setting operational amplifier at unity gain, 0-dBm0 reference measured at VFXO (see Note 5)	16.67 Hz		−80	−60	dBm
			50 Hz			−30	
			60 Hz			−25	
			200 Hz	−1.2		−0.125	
			300 Hz to 3 kHz	−0.125		0.125	
			3.3 kHz	−0.35		0.1	
			3.4 kHz (TCM2912-3)	−0.7		−0.1	
			3.4 kHz (TCM2912)	−1		−0.1	
			4 kHz			−14	
			4.6 kHz and above			−35	
Absolute passband gain at VFXO		f = 1 kHz, R_L = 10 kΩ		2.8	3	3.2	dB
Gain variation with temperature		f = 1 kHz, Signal level = 0 dBm0			0.0008		dB/°C
Gain variation with supply voltage		f = 1 kHz, Signal level = 0 dBm0, Supply variation = ±5%			0.04		dB/V
Crosstalk attenuation, receive to transmit at VFXO		VFRI = 1.6 V rms, f = 1 kHz, ANLG IN− connected to GSX, ANLG IN+ connected to ANLG GND		70	80		dB
Single-frequency distortion products		f = 1 kHz, Signal level = 0 dBm0 at VFXO				−48	dB
		f = 1 kHz, Signal level = 3 dBm0 at VFXO, Gain-setting operational amplifier at 20-dB gain				−45	
Total C-message noise at VFXO	TCM2912B	Gain-setting operational amplifer at unity gain			5	7	dBrnC0
		Gain-setting operational amplifier at 20-dB gain			6	8	
	TCM2912C	Gain-setting operational amplifier at unity gain			4	6	dBrnC0
		Gain setting operational amplifier at 20-dB gain			4	6	
Differential envelope delay time		f = 1 kHz to 2.6 kHz			60	80	μs
Absolute delay time					100	150	μs

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.
NOTE 5: A 0-dBm0 signal is equivalent to 1.1 V rms at ANLG IN+ and 1.6 V rms output at VFXO.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

receive filter transfer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Gain relative to 1 kHz with 0 dBm0 input signal		0 dBm0 measured at VFRO	below 200 Hz	−0.2		0.125	dBm
			200 Hz	−0.2		0.125	
			300 Hz to 3 kHz	−0.125		0.125	
			3.3 kHz	−0.35		0.03	
			3.4 kHz (TCM2912-3)	−0.7		−0.1	
			3.4 kHz (TCM2912)	−1		−0.1	
			4 kHz			−14	
			4.6 kHz and above			−35	
Absolute passband gain at VFRO		f = 1 kHz, R_L = 10 kΩ		−0.2		0.2	dB
Gain variation with temperature		f = 1 kHz, Signal level = 0 dBm0			0.0002		dB/°C
Gain variation with supply voltage		f = 1 kHz, Signal level = 0 dBm0, Supply variation = ±5%			0.04		dB/V
Crosstalk attenuation, transmit to receive at VFRO		ANLG IN− connected to GSX, ANLG IN+ at 1.1 V rms, f = 1 kHz, VFRI connected to ANLG GND		70	76		dB
Single-frequency distortion products		f = 1 kHz, Input signal = 0 dBm0				−48	dB
		f = 1 kHz, Input signal = 3 dBm0				−45	
Total C-message noise at VFRO	TCM2912B	Measured at VFRO			4	7	dBrnC0
	TCM2912C				4	6	
Differential envelope delay time		f = 1 kHz to 2.6 kHz			25	80	μs
Absolute delay time	VFRO				110	140	μs
	PWRO−				120	180	

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C

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TRANSFER CHARACTERISTICS OF THE
TRANSMIT SECTION

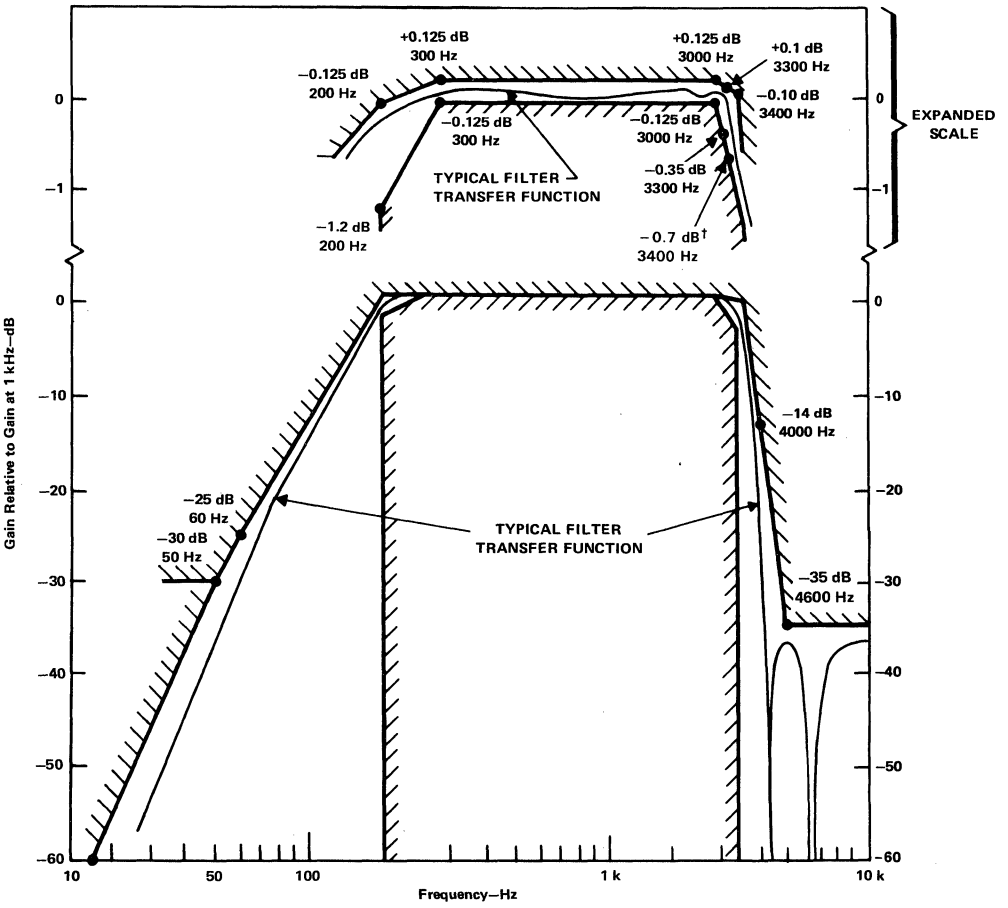


FIGURE 1

† Applies to the TCM2912B-3 and TCM2912C-3 only.

TRANSFER CHARACTERISTICS OF THE
RECEIVE SECTION

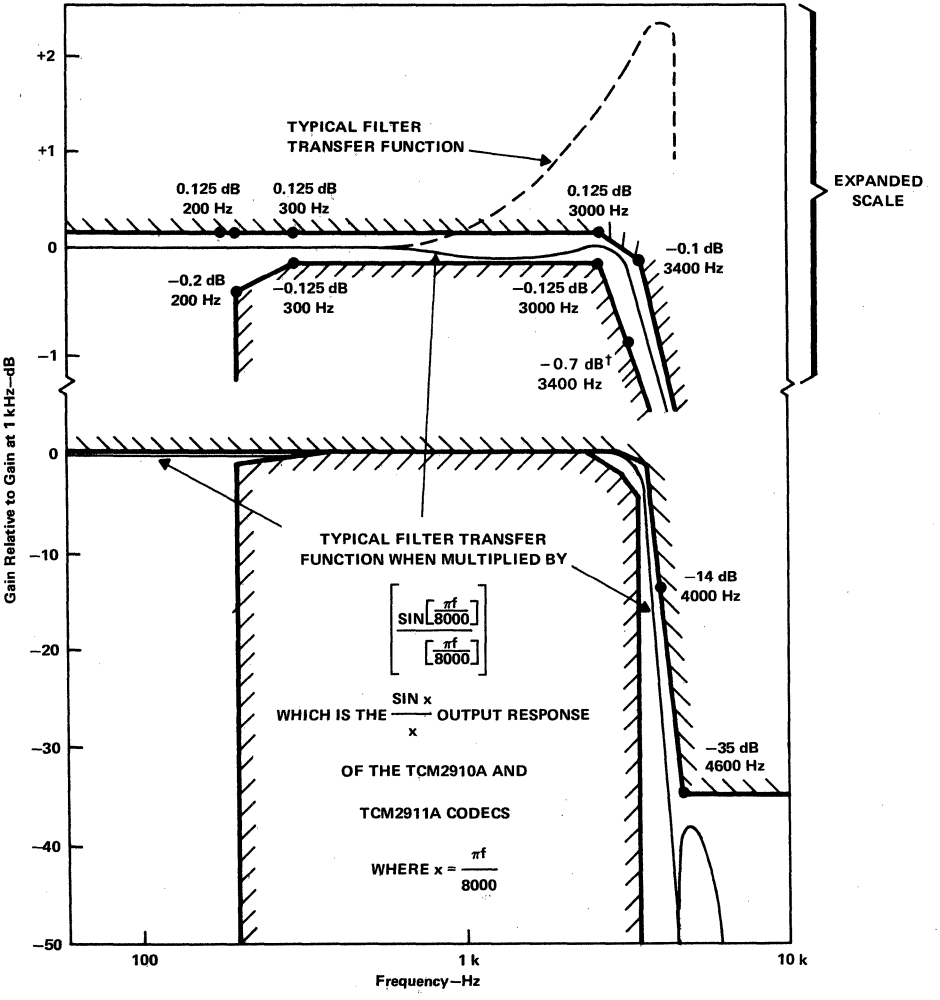
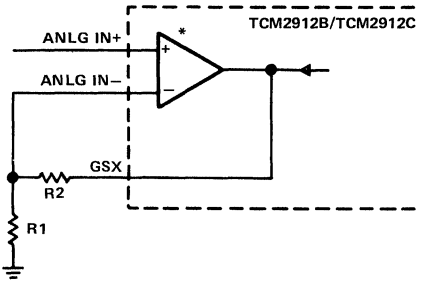


FIGURE 2

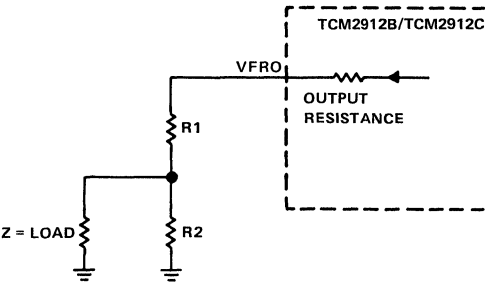
† Applies to the TCM2912B-3 and TCM2912C-3 only.

TYPICAL APPLICATION DATA



*GAIN = 1 (R2/R1)

FIGURE 3. PASSBAND GAIN ADJUSTMENT



$$R_T = R1 + \frac{R2 \cdot Z}{R2+Z} = 10\ k\Omega$$

FIGURE 4. OUTPUT GAIN ADJUSTMENT FOR RECEIVE FILTER IF DRIVER AMPLIFIER IS NOT USED.

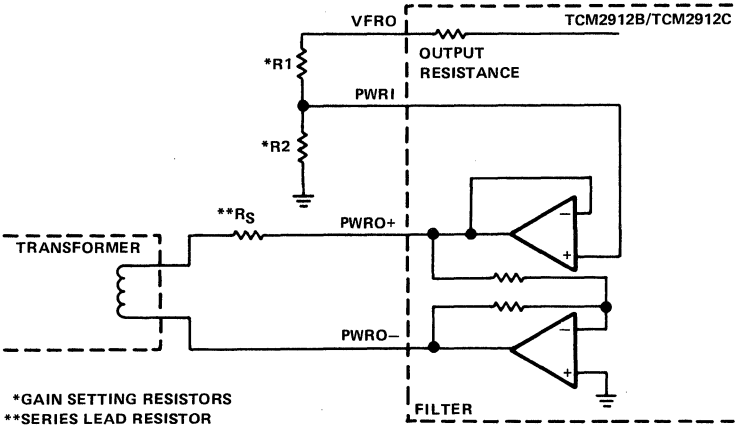


FIGURE 5. TYPICAL CONNECTION FOR OUTPUT DRIVER AMPLIFIER WITH EXTERNAL GAIN ADJUST

TYPICAL CHARACTERISTICS

DEPARTURE FROM LINEAR PHASE
TCM2912B
TRANSMIT SECTION

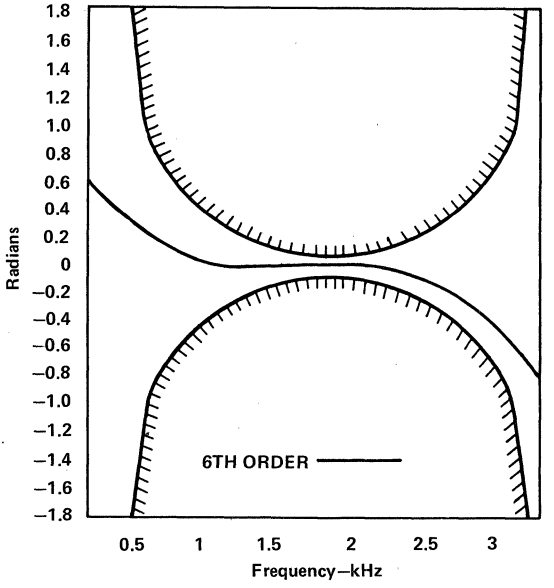


FIGURE 6

FROM: *DIGITAL CHANNEL BANK REQUIREMENTS AND OBJECTIVES*, AT&T, JUNE 1978, PUB 43801, PARAGRAPH 13.4.

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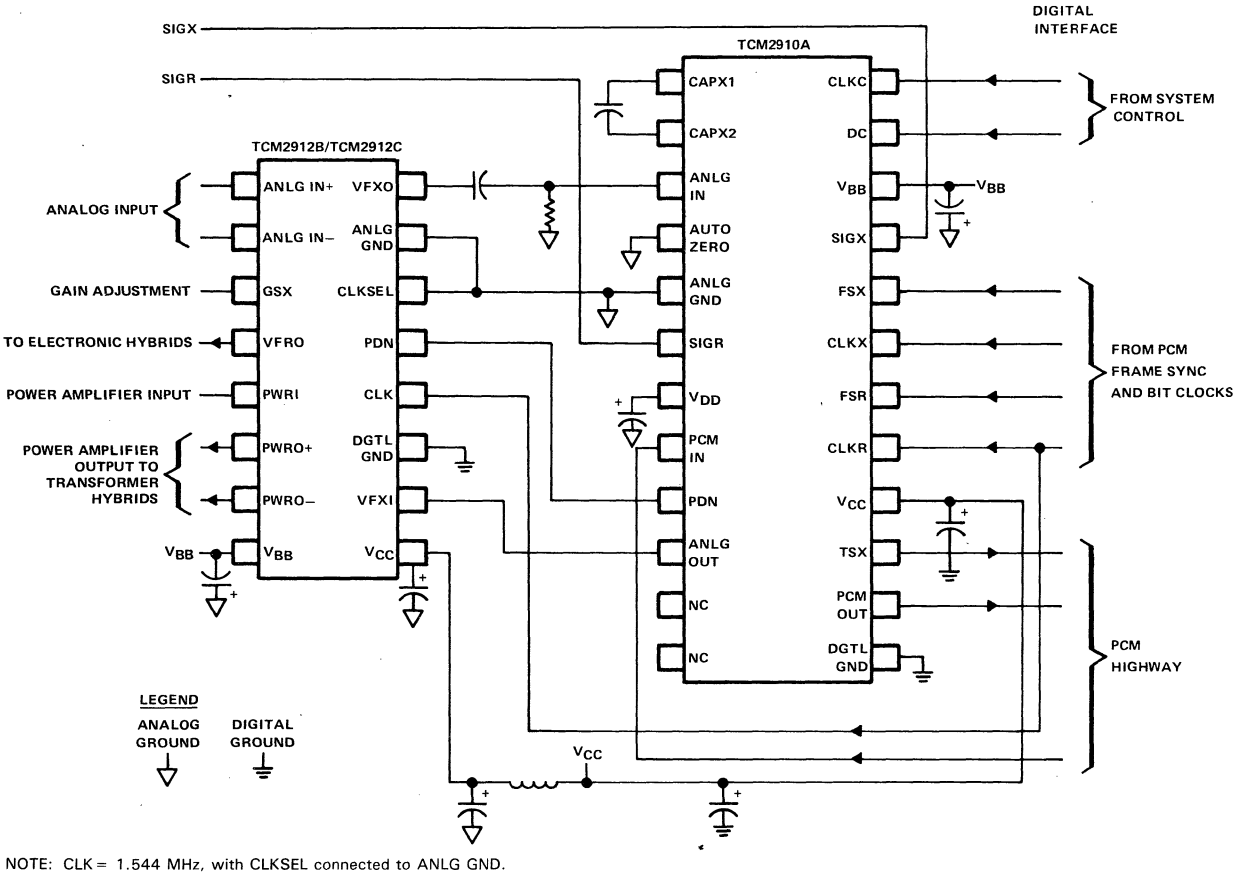

NOTE: CLK = 1.544 MHz, with CLKSEL connected to ANLG GND.

FIGURE 7. TCM2912B/TCM2912C INTERFACE WITH TCM2910A CODEC

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TCM2913, TCM2914, TCM2916, TCM2917
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

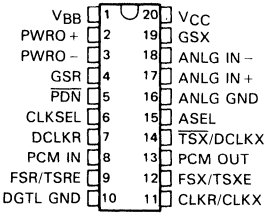
D2765, SEPTEMBER 1983—REVISED MAY 1986

- Replaces Use of TCM2910A and TCM2911A in Tandem with TCM2912B
- No External Components Needed for Sample, Hold, and Auto Zero Functions
- Low Power Consumption:
  Operating Mode . . . 140 mW Typical
  Power-Down Mode . . . 5 mW Typical
- Excellent Power Supply Rejection Ratio Over Frequency Range of 0 to 50 kHz
- Precision Internal Voltage References
- Reliable Advanced N-Channel MOS Technology
- Direct Replacement for Intel 2913, 2914, 2916, and 2917.

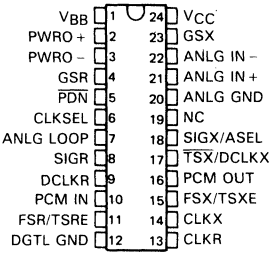
FEATURE TABLE

FEATURE	2913	2914	2916	2917
Number of Pins:				
24		X		
20	X			
16			X	X
μ-law/A-law Coding:				
μ-law	X	X	X	
A-law	X	X		X
Data Timing Rates:				
Variable Mode				
64 kHz to 2.048 MHz	X	X	X	X
Fixed Mode				
1.536 MHz	X	X		
1.544 MHz	X	X		
2.048 MHz	X	X	X	X
Loopback Test Capability		X		
8th-Bit Signaling		X		

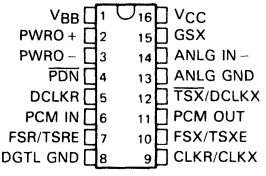
TCM2913
J DUAL-IN-LINE PACKAGE
(TOP VIEW)



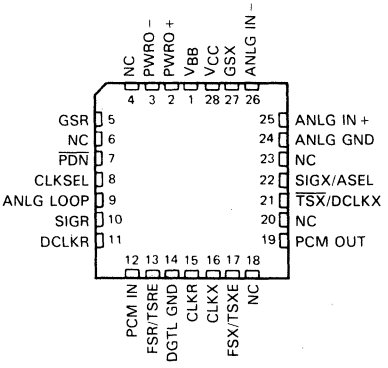
TCM2914
J DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM2916, TCM2917
J DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM2914 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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description

The TCM2913, TCM2914, TCM2916, and TCM2917 are single-chip pulse-code-modulated encoders and decoders (PCM codecs) and PCM line filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. These devices are intended to replace the TCM2910A and TCM2911A in tandem with the TCM2912B or TCM2912C. Primary applications of the devices include:

- Line Interface for Digital Transmission and Switching of T1 Carrier, PABX, and Central Office Telephone Systems
- Subscriber Line Concentrators
- Digital Encryption Systems
- Digital Voice Band Data Storage Systems
- Digital Signal Processing

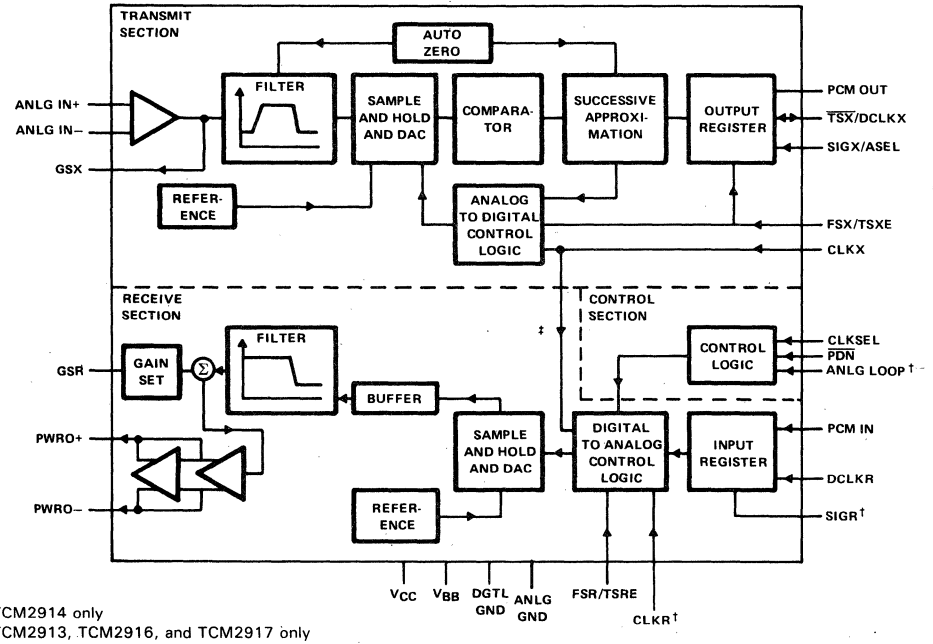
These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM2913, TCM2914, TCM2916, and TCM2917 provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

The TCM2913, TCM2914, TCM2916, and TCM2917 are characterized for operation from 0°C to 70°C.

The TCM2913-3 version is identical to the standard version except that maximum encoder milliwatt response and digital milliwatt response are ±0.40 dBm0.

functional block diagram



†TCM2914 only
‡TCM2913, TCM2916, and TCM2917 only

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PIN			NAME	DESCRIPTION
TCM2913	TCM2914†	TCM2916 TCM2917		
1	1 [1]	1	V_{BB}	Most negative supply voltage; input is −5 V ±5%.
2	2 [2]	2	PWRO+	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
3	3 [3]	3	PWRO−	Inverting output of power amplifier; functionally identical with and complementary to PWRO+.
4	4 [5]		GSR	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
5	5 [7]	4	$\overline{PDN}$	Power-down select. The device is inactive with a TTL low-level input to this pin and active with a TTL high-level input to the pin.
6	6 [8]		CLKSEL	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency. When tied to V_{BB}, CLK is 2.048 MHz. When tied to ground, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 1.536 MHz.
	7 [9]		ANLG LOOP	Provides loopback test capability. When this input is TTL high, PWRO+ is internally connected to ANLG IN.
	8 [10]		SIGR	Signaling bit output, receive channel; in a fixed-data-rate mode, outputs the logical state of the 8th bit (LSB) of the PCM word in the most recent signaling frame.
7	9 [11]	5	DCLKR	Selects fixed or variable data-rate operation. When this pin is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode, and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz.
8	10 [12]	6	PCM IN	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
9	11 [13]	7	FSR/TSRE	Frame synchronization clock input/time slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and non-signaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the timeslot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
10	12 [14]	8	DGTL GND	Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
11	13 [15]	9	CLKR	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together for TCM2913, TCM2916, and TCM2917.

†Pin numbers shown in square brackets are for the FN package.

PIN			NAME	DESCRIPTION
TCM2913	TCM2914†	TCM2916 TCM2917		
11	14 [16]	9	CLKX	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable data rate mode. CLKR and CLKX are internally connected for the TCM2913, TCM2916, and TCM2917.
12	15 [17]	10	FSX/TSXE	Frame synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analagous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is TTL low for 300 ms.
13	16 [19]	11	PCM OUT	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
14	17 [21]	12	$\overline{\text{TSX}}$/DCLKX	Transmit channel time slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this pin is an open-drain output to be used as an enable signal for a three-state buffer. In the variable-data rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
15	18 [22]		SIGX/ASEL	Used to select between A-law and μ-law operation. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or ground, μ-law is selected. When not connected to V_{BB}, it is a TTL-level input that is transmitted as the eighth bit (LSB) of the PCM word during signaling frames on the PCM OUT pin (TCM2914 only). SIGX/ASEL is internally connected to V_{BB} on TCM2916 and to ground on TCM2917.
16	20 [24]	13	ANLG GND	Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
17	21 [25]		ANLG IN+	Noninverting analog input to uncommitted transmit operational amplifier. Internally connected to ANLG GND on TCM2916 and TCM2917.
18	22 [26]	14	ANLG IN−	Inverting analog input to uncommitted transmit operational amplifier.
19	23 [27]	15	GSX	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
20	24 [28]	16	V_{CC}	Most positive supply voltage; input is 5 V ± 5%.

†Pin numbers shown in square brackets are for the FN package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 15 V
Output voltage, V_O . . . . . −0.3 V to 15 V
Input voltage, V_I . . . . . −0.3 V to 15 V
Digital ground voltage . . . . . −0.3 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range (under bias) . . . . . −10°C to 80°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. Voltage values for maximum ratings are with respect to V_{BB}.
2. For operation above 25°C free-air temperature, derate linearly to 770 mW at 80°C at the rate of 11 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
	Clock select input voltage	For 2.048 MHz	V_{BB}		$V_{BB}+0.5$	V
		For 1.544 MHz	0		0.5	
		For 1.536 MHz	$V_{CC}-0.5$		V_{CC}	
R_L	Load resistance	At GSX	10			kΩ
		At PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	At GSX			50	pF
		At PWRO+ and/or PWRO−			100	
T_A	Operating free-air temperature		0		70	°C

NOTE 3: Voltages at analog inputs and outputs, V_{CC}, and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating			14	19	mA
		Standby	FSX, FSR = V_{IL} after 300 ms		1.2	2.4	
		Power-down	PDN = V_{IL} after 10 μs		0.5	1	
I_{BB}	Supply current from V_{BB}	Operating			−18	−24	mA
		Standby	FSX, FSR = V_{IL} after 300 ms		−1.2	−2.4	
		Power-down	PDN = V_{IL} after 10 μs		−0.5	−1	
	Power dissipation	Operating			140	226	mW
		Standby	FSX, FSR = V_{IL} after 300 ms		12	25	
		Power down	PDN = V_{IL} after 10 μs		5	10.5	

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

digital interface

PARAMETER			TEST CONDITONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_{OH} = −9.6 mA	2.4			V
		SIGR	I_{OH} = −1.2 mA	2.4			
V_{OL}	Low-level output voltage at DX, TSX, SIGR		I_{OL} = 3.2 mA			0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	μA
I_{IL}	Low-level input current, any digial input		V_I = 0 to 0.8 V			10	μA
C_i	Input capacitance				5	10	pF
C_o	Output capacitance				5		pF

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±25	mV
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V	55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+, PWRO− (single-ended)	Relative to ANLG GND		120		mV
Output resistance at PWRO+, PWRO−			1		Ω

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

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gain and dynamic range, V_{CC} = 5 V, V_{BB} = −5 V, T_A = 25°C (unless otherwise noted) (see Notes 4, 5, and 6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 V rms	Standard versions		±0.08	±0.18	dBm0
			TCM2913-3		±0.18	±0.40	
Encoder milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ±5%				±0.07	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711, Output signal = 1 kHz	Standard versions		±0.08	±0.18	dBm0
			TCM2913-3		±0.18	±0.40	
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ±5%				±0.07	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω			2.76		dBm
	A-law				2.79		
	μ-law	R_L = 900 Ω			1		
	A-law				1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω			5.76		dBm
	A-law				5.79		
	μ-law	R_L = 900 Ω			4		
	A-law				4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 V rms, or an output of 1.503 V rms.
5. The input amplifier is set for unity gain, noninverting. GSX is connected to ANLG IN−. Signal input is ANLG IN+. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
6. Receive output is measured single-ended in the maximum-gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO− and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = −10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain tracking error, sinusoidal input	−3 to −40 dBm0		±0.25	dB
	−40 to −50 dBm0		±0.5	
	−50 to −55 dBm0		±1.2	
Receive gain tracking error, sinusoidal input	−3 to −40 dBm0		±0.25	dB
	−40 to −50 dBm0		±0.5	
	−50 to −55 dBm0		±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		15	dBrnC0
Transmit noise, C-message weighted with eighth-bit signaling (TCM2914 only)	ANLG IN+ = ANLG GND, ANLG IN− = GSX, 6th frame signaling		18	dBrnC0
Transmit noise, psophometrically weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		−75	dBm0p
Receive noise, C-message weighted quiet code	PCM IN = 11111111 (μ-law) PCM IN = 10101010 (A-law) measured at PWRO+		11	dBrnC0
Receive noise, C-message weighted sign bit toggled	Input to PCM IN is zero code with sign bit toggled at 1-kHz rate		12	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level		−79	dBm0p

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply voltage rejection ratio, transmit channel	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	f = 30 to 50 kHz			−45		
V_{BB} supply voltage rejection ratio, transmit channel	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	f = 30 to 50 kHz			−55		
V_{CC} supply voltage rejection ratio, receive channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	f = 30 to 50 kHz			−45		
V_{BB} supply voltage rejection ratio, receive channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	f = 30 to 50 kHz			−45		
Crosstalk attenuation, transmit-to-receive (single-ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, unity gain, PCM IN = lowest decode level measured at PWRO+	71			dB
Crosstalk attenuation, receive-to-transmit (single-ended)		PCM IN = 0 dBm0, f = 1.02 kHz, ANLG IN+ = ANLG GND, measured at PCM OUT	71			dB

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

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distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal to distortion ratio, sinusoidal input (see Note 7)	ANLG IN+ = 0 to −30 dBm0	36			dB
	ANLG IN+ = −30 to −40 dBm0	30			
	ANLG IN+ = −40 to −45 dBm0	25			
Receive signal to distortion ratio, sinusoidal input (see Note 7)	ANLG IN+ = 0 to −30 dBm0	36			dB
	ANLG IN+ = −30 to −40 dBm0	30			
	ANLG IN+ = −40 to −45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Intermodulation distortion, end-to-end Spurious out-of-band signals, end-to-end	CCITT G.712 (7.1)			−35	dBm0
	CCITT G.712 (7.2)			−49	
	CCITT G.712 (6.1)			−25	dBm0
	CCITT G.712 (9)			−40	
Transmit absolute delay time to PCM OUT	Fixed data rate, CLKS = 2.048 MHz, Input to ANLG IN+ = 1.02 kHz at 0 dBm0		245		μs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		170		μs
	f = 600 Hz to 100 Hz		95		
	f = 100 Hz to 2600 Hz		45		
	f = 2600 Hz to 2800 Hz		105		
Receive absolute delay time to PCM OUT	Fixed data rate, f_{CLKR} = 2.048 MHz, Digital input is DMW codes		190		μs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		45		μs
	f = 600 Hz to 100 Hz		35		
	f = 1000 Hz to 2600 Hz		85		
	f = 2600 Hz to 2800 Hz		110		

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTES: 7. CCITT G.712 — Method 2.
8. CCITT G.712 — Method 1.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at PCM IN is 0 dBm0	16.67 Hz		−30	dB
		50 Hz		−25	
		60 Hz		−23	
		200 Hz	−1.8	0.125	
		300 Hz to 3 kHz	−0.125	0.125	
		3.3 kHz	−0.35	0.03	
		3.4 kHz	−0.7	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−32	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature(see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz		0.125	dB
		200 Hz	−0.5	0.125	
		300 Hz to 3 kHz	−0.125	0.125	
		3.3 kHz	−0.35	0.03	
		3.4 kHz	−0.7	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−30	

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see timing diagrams)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLKX and CLKR			5	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 9)	220			ns
$t_{w(DCLK)}$	Pulse duration for DCLK (f_{DCLK} = 64 Hz to 2.048 MHz) (see Note 9)	220			ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	45	50	55	%

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(SIGX)}$	Setup time before Bit 7 falling edge (TCM2914 only)	0		ns
$t_{h(SIGX)}$	Hold time after Bit 8 falling edge (TCM2914 only)	0		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to Bit 1 data valid at PCM OUT (data enable time on time slot entry) (see Note 10)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock Bit n to Bit n + 1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock Bit 8 to Bit 8 Hi-Z at PCM OUT (data float time on time slot exit) (see Note 10)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock Bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock Bit 8 to TSX inactive (high) (time slot disable time) (see Note 10)	C_L = 0	60	190	ns
t_{pd6}	From rising edge of channel time slot to SIGR update (TCM2914 only)		0	2	μs

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame sync delay time	100	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 7 falling edge (TCM2914 only)	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 8 falling edge (TCM2914 only)	60		ns

NOTES: 9. FSX CLK must be phase locked with the CLKX. FSR CLK must be phase locked with CLKR.
10. Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

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transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

	PARAMETER	MIN	MAX	UNIT
$t_{d(TSDX)}$	Timeslot delay time from DCLKX (see Note 11)	140	$t_{d(DCLKX)} - 140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)} - 100$	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	488	15620	ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 12 and timing diagrams)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd8}	Data delay from timeslot enable to PCM OUT	C_L = 0 to 100 pF	0	50	ns
t_{pd9}	Data delay from time slot disable to PCM OUT	C_L = 0 to 100 pF	0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	140	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

	PARAMETER	MIN	MAX	UNIT
$t_{d(TSDR)}$	Timeslot delay time from DCLKR (see Note 13)	140	$t_{d(DCLKR)} - 140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)} - 100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 8 falling edge	60		ns
$t_{c(DCLKR)}$	Clock period for DCLKR	488	15620	ns
	Timeslot end receive time	0		ns

64-kilobit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame sync minimum down time	FSR = TTL high for remainder of frame	1952		ns
t_{DCLK}	Pulse duration data clock			10	μs

NOTES: 11. t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.
12. Timing parameters t_{pd8} and t_{pd9} are referenced to a high-impedance state.
13. t_{FSLR} minimum requirement overrides the $t_{d(TSDR)}$ maximum requirement for 64-kHz operation.

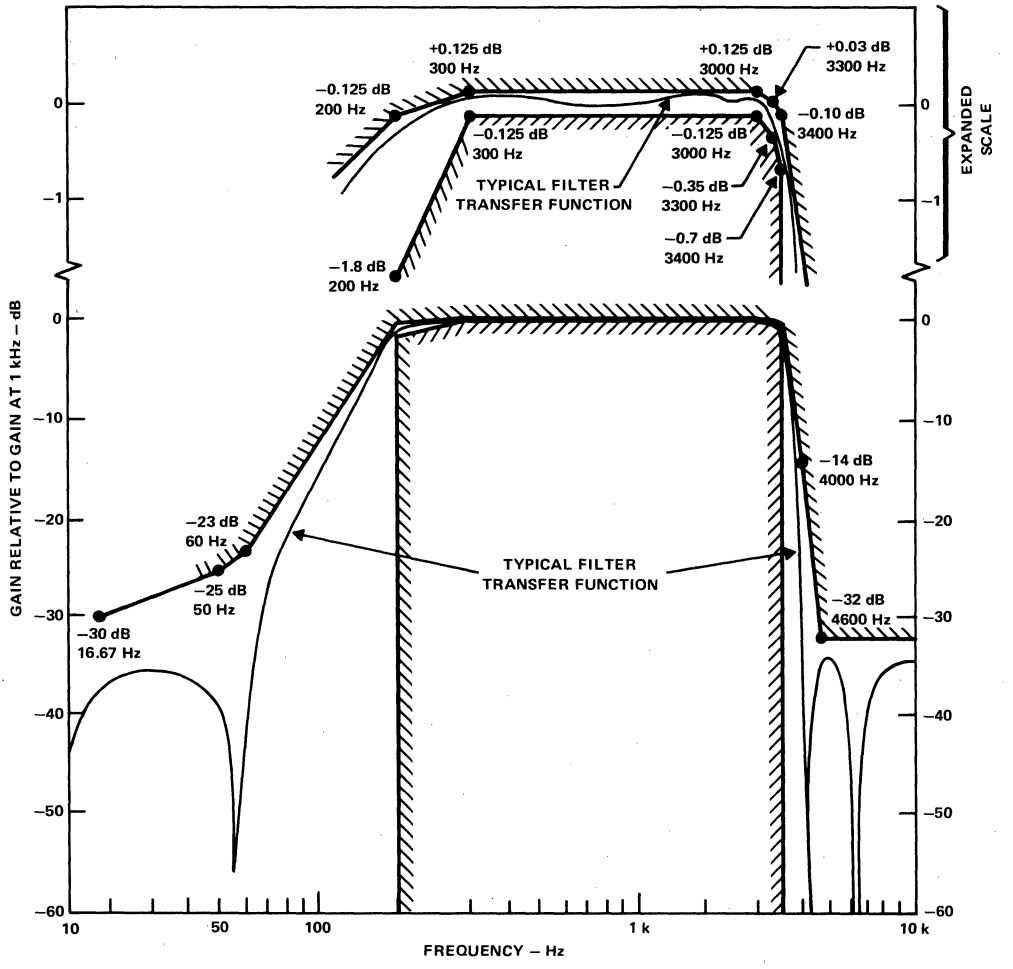

FIGURE 1. TRANSFER CHARACTERISTICS OF THE TRANSMIT FILTER

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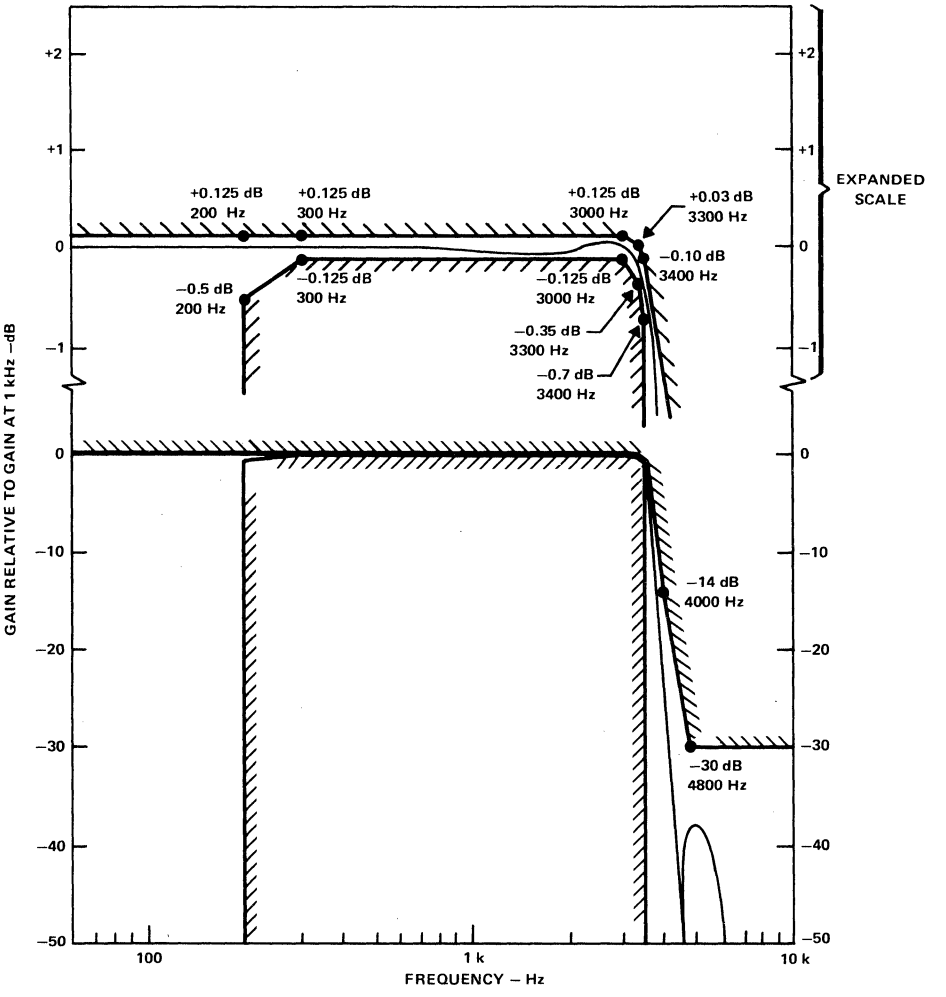

NOTE: This is a typical transfer function of the receiver filter component.

FIGURE 2. TRANSFER CHARACTERISTIC OF THE RECEIVE FILTER

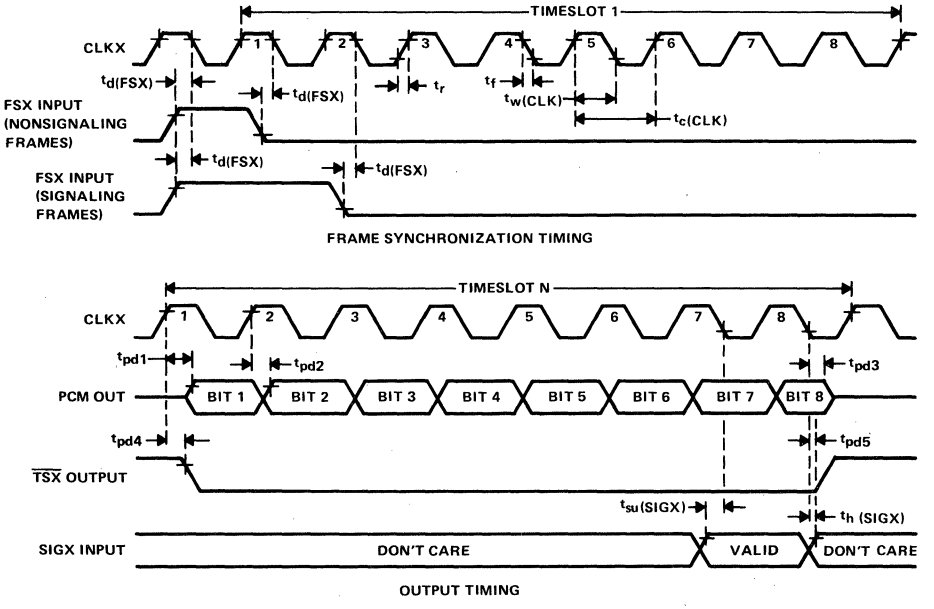

FIGURE 3. TRANSMIT TIMING (FIXED-DATA-RATE)

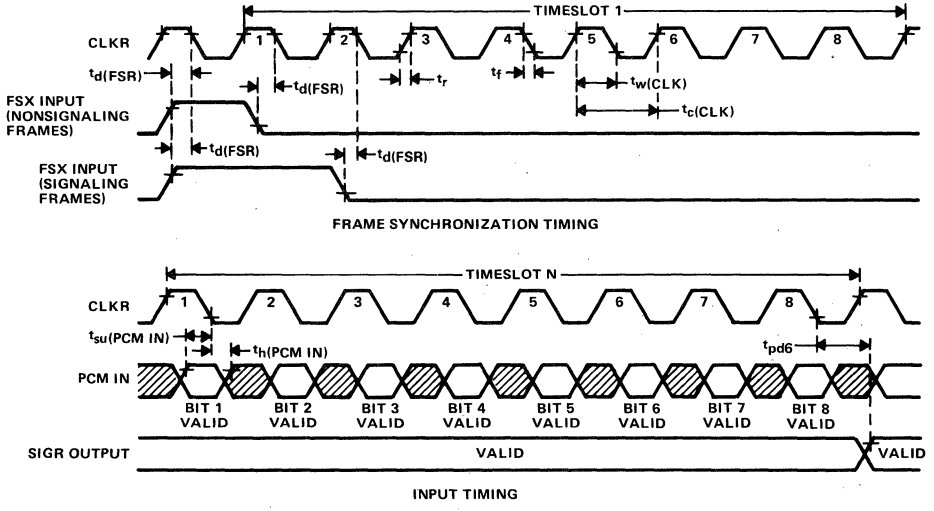

FIGURE 4. RECEIVE TIMING (FIXED-DATA-RATE)

NOTE: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

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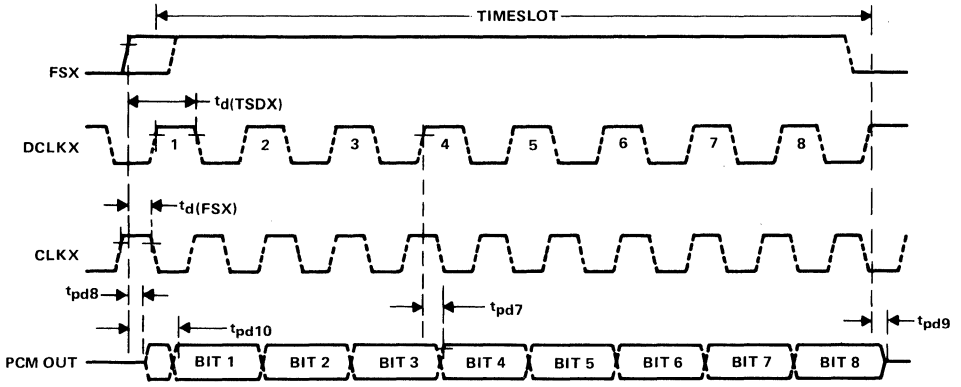
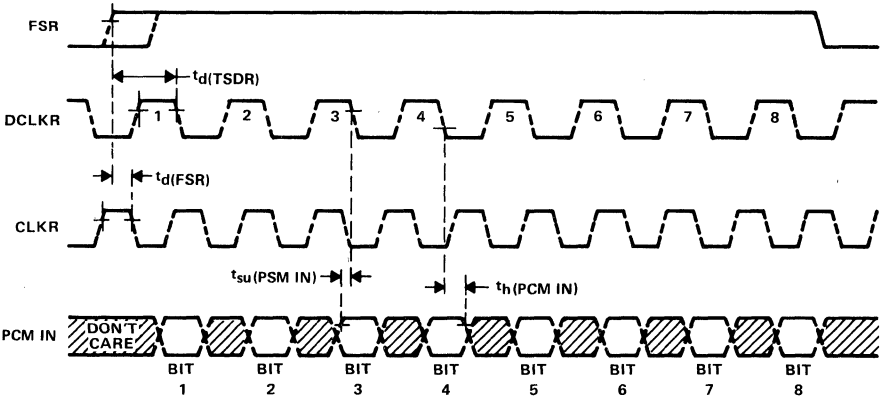


FIGURE 5. TRANSMIT TIMING (VARIABLE-DATA-RATE)



NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which reference a high-impedance state.

FIGURE 6. RECEIVE TIMING (VARIABLE-DATA-RATE)

GENERAL OPERATION

system reliability features

The TCM2913, TCM2914, TCM2916, or TCM2917 is powered up in four steps:
V_{CC} and V_{BB} supply voltages are applied.
All clocks are connected.
TTL high is applied to $\overline{PDN}$.
FSX and/or FSR synchronization pulses are applied.

On the transmit channel, digital outputs PCM out and $\overline{TSX}$ are held in high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIGR is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIGR will remain low until it is updated by a signaling frame.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ will be placed in a high-impedance state approximately 20 μs after an interruption of CLKX. SIGR will be held low approximately 20 μs after an interruption of CLKR. These interruptions could possibly occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external TTL low signal is applied to the $\overline{PDN}$ pin. It is not sufficient to remove the TTL high voltage to $\overline{PDN}$. In the absence of a signal, the $\overline{PDN}$ pin floats to TTL high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 5 mW.

The standby modes give the user the option of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held at TTL low. For transmit-only operation, FSX is high and FSR is held low. For receive-only operation, FSR is high and FSX is held low. See Table 1 for power down and standby procedures.

TABLE 1. POWER DOWN AND STANDBY PROCEDURES

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ = TTL low	5 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to TTL low within 10 μs.
Entire device on standby	FSX and FSR are TTL low	12 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to TTL low within 300 ms.
Only transmit on standby	FSX is TTL low FSR is TTL high	70 mW	$\overline{TSX}$ and PCM OUT are placed in a high-impedance state within 300 ms.
Only receive on standby	FSR is TTL low FSX is TTL high	110 mW	SIGR is placed in a high-impedance state within 300 ms.

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fixed-data-rate timing (see Figure 7)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clocks CLKX and CLKR, frame synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency and distinguish between signaling and nonsignaling frames by their pulse width. A frame synchronization pulse one master clock wide designates a nonsignaling frame, while a double width sync pulse enables the signaling function (TCM2914 only). Data is transmitted on the PCM OUT pin on the first eight positive transitions of CLKX following the rising edge of FSX. Data is received on the PCM IN pin on the first eight falling edges of CLKR following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The clock selection pin (CLKSEL) is used to select the frequency of CLKX and CLKR (TMC2913 and TCM2914 only). The TCM2913 and TCM2914 fixed data rate mode can operate with frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz. The TCM2916 and TCM2917 fixed data rate mode operates at 2.048 MHz only.

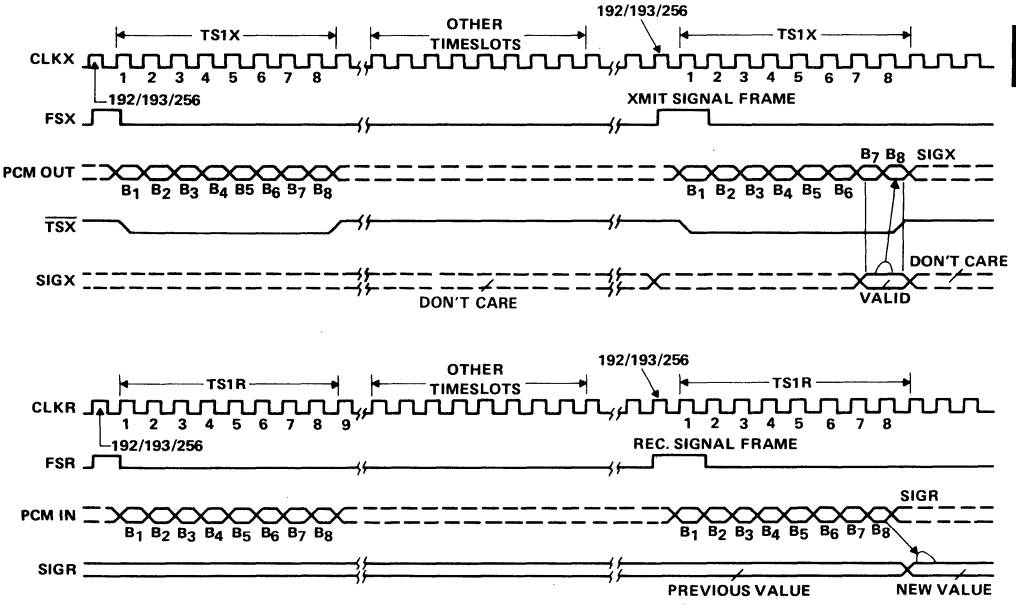

FIGURE 7. SIGNALING TIMING (FIXED-DATA-RATE ONLY)

variable data rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks can be asynchronous in the TCM2914, but must be synchronous in the TCM2913, TCM2916, and TCM2917. Master clocks in types TCM2913 and TCM2914 are restricted to frequencies of operation of 1.536 MHz, 1.544 MHz, or 2.048 MHz as in the fixed-data-rate timing mode. The master clock for the TCM2916 and TCM2917 is restricted to 2.048 MHz.

While FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

signaling

The TCM2914 (only) provides 8th-bit signaling in the fixed-data-rate timing mode. Transmit and receive signaling frames are independent of each other and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the signal present on SIGX is substituted for the least significant bit (LSB) of the encoded PCM word. In a receive signaling frame, the codec will decode the seven most significant bits in accordance with CCITT G.733 recommendations, and output the logical state of the LSB on the SIGR pin until it is updated in the next signaling frame. Timing relationships for signaling operations are shown n Figure 9. The signaling path is used to transmit digital signaling information such as ring control, rotary dial pulses, and off-hook and disconnect supervision. The voice path is used to transmit prerecorded messages as well as the call progress tones; dial tone, ring-back tone, busy tone, and re-order tone.

asynchronous operation

The TCM2914 can be operated with asynchronous clocks in either the fixed- or variable-data-rate modes. In order to avoid crosstalk problems associated with special interrupt circuits, the design of the TCM2913 and TCM2914 includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-data-rate mode the rising edge of CLKX must occur within $t_{d(FSX)}$ ns before the rise of FSX, while the leading edge of DCLKX must occur within t_{TSDX} ns of the rise of FSX. CLKX and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see variable data rate timing diagrams). This approach requires the provision of two separate master clocks but avoids the use of a synchronizer, which can cause intermittent data conversion errors.

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analog loopback

A distinctive feature of the TCM2914 is its analog loopback capability. With this feature, the user can test the line circuit remotely by comparing the signals sent into the receive channel (PCM IN) with those generated on the transmit channel (PCM OUT). The test is accomplished by sending a control signal that internally connects the analog input and output ports. When ANLG LOOP is TTL high, the receive output (PWRO +) is internally connected to ANLG IN +, GSR is internally connected to PWRO −, and ANLG IN − is internally connected to GSX (see Figure 8).

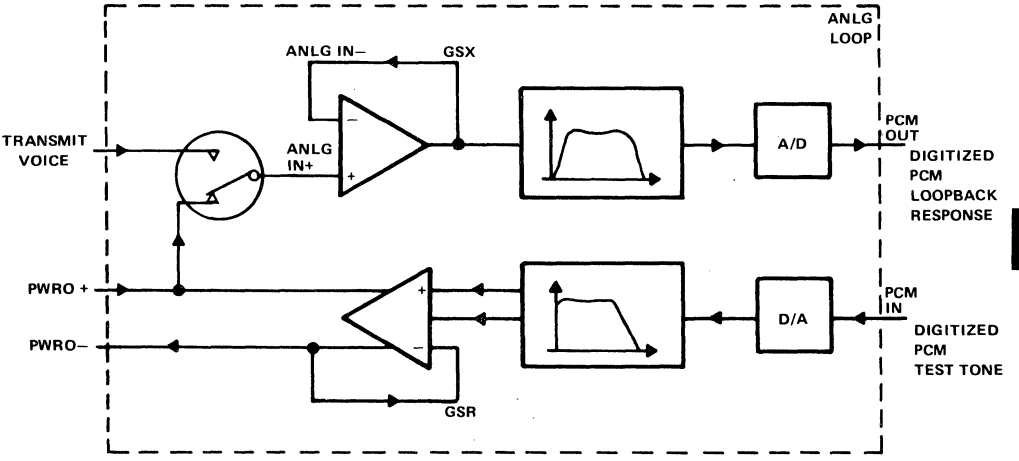

FIGURE 8. TCM2914 ANALOG LOOPBACK CONFIGURATION

Due to the difference in the transmit and receive transmission levels, a 0 dBm0 code into PCM IN will emerge from PCM OUT as a 3-dBm0 code, an implicit gain of 3 dB. Because of this, the maximum signal that can be tested by analog loopback is 0 dBm0.

precision voltage references

No external components are required with the TCM2913, TCM2914, TCM2916, and TCM2917 to provide the voltage references. Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage. These references are calibrated during the manufacturing process.Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain setting operational amplifiers to a final precision value. Manufacturing tolerances can be achieved of typically ±0.04 dB in absolute gain for each half channel, providing the user a significant margin to compensate for error in other board components.

conversion laws

The TCM2913 and TCM2914 provide pin-selectable μ-law operation as specified by CCITT G.711 recommendation. A-law operation is selected when the ASEL pin is connected to V_{BB}. Signaling is not allowed during A-law operation. The TCM2916 is μ-law only. The TCM2917 is A-law only.

The μ-law operation is effectively selected by not selecting A-law operation. If the ASEL pin is connected to V_{CC} or GND, the device is in μ-law operation. If μ-law operation is selected, SIGX is a TTL-level input that can be used in the fixed data rate timing mode to modify the LSB of the PCM output in signaling frames.

transmit operation

transmit filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. The load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on the ANLG IN + pin can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The TCM2913, TCM2914, TCM2916, and TCM2917 specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder performs an analog-to-digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clocks bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at the PCM IN pin on the first eight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides passband flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

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receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single-ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output will directly drive a bridged load. The output stage is capable of driving loads as low as 300 ohms single-ended to a level of 12 dBm or 600 ohms differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GSR input. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO−, the receive level is at maximum. When GSR is connected to PWRO+, the level is minimum. The output transmission level is adjusted between 0 and −12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO−.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

TYPICAL APPLICATION DATA

output gain set design considerations (see Figure 9)

PWRO+ and PWRO− are low-impedance complementary outputs. The voltages at the nodes are:
V_{O+} at PWRO+
V_{O-} at PWRO−
$V_O = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:
The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant which has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response (V_A = 3.06 V rms).

$$\text{Where } A = \frac{V_O = A \cdot V_A}{1 + (R1/R2)}{4 + (R1/R2)}$$

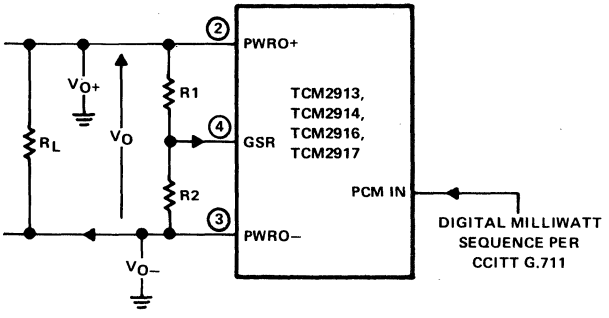


FIGURE 9. GAIN-SETTING CONFIGURATION

TCM29C13, TCM29C14, TCM29C16, TCM29C17
COMBINED SINGLE-CHIP PCM CODEC AND FILTER

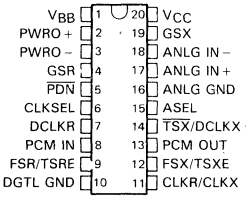
D2765, APRIL 1986

- **Replaces Use of TCM2910A and TCM2911A in Tandem with TCM2912B/C**
- **Reliable Silicon-Gate CMOS Technology**
- **Low Power Consumption:**
  Operating Mode . . . 80 mW Typical
  Power-Down Mode . . . 5 mW Typical
- **Excellent Power Supply Rejection Ratio Over Frequency Range of 0 to 50 kHz**
- **No External Components Needed for Sample, Hold, and Auto-Zero Functions**
- **Precision Internal Voltage References**
- **Direct Replacement for Intel 2913, 2914, 2916, and 2917**
- **Formerly TCM4913, TCM4914, TCM4916, TCM4917, Respectively**

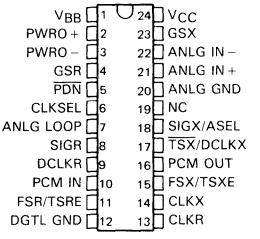
FEATURE TABLE

FEATURE	29C13	29C14	29C16	29C17
Number of Pins:				
24		X		
20	X			
16			X	X
μ-law/A-law Coding:				
μ-law	X	X	X	
A-law	X	X		X
Data Timing Rates:				
Variable Mode				
64 kHz to 2.048 MHz	X	X	X	X
Fixed Mode				
1.536 MHz	X	X		
1.544 MHz	X	X		
2.048 MHz	X	X	X	X
Loopback Test Capability		X		
8th-Bit Signaling		X		

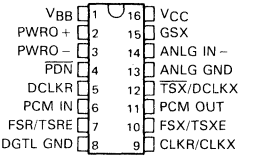
TCM29C13
J DUAL-IN-LINE PACKAGE
(TOP VIEW)



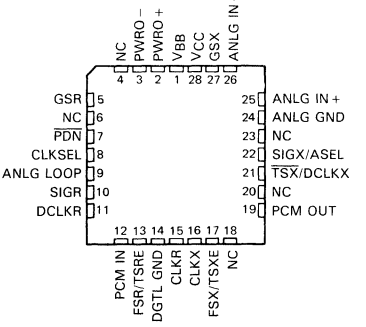
TCM29C14
J DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM29C16, TCM29C17
J DUAL-IN-LINE PACKAGE
(TOP VIEW)



TCM29C14 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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description

The TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are single-chip pulse-code-modulated encoders and decoders (PCM codecs) and PCM line filters. These devices provide all the functions required to interface a full-duplex (4-wire) voice telephone circuit with a time-division-multiplexed (TDM) system. These devices are intended to replace the TCM2910A or TCM2911A in tandem with the TCM2912B/C. Primary applications of the devices include:

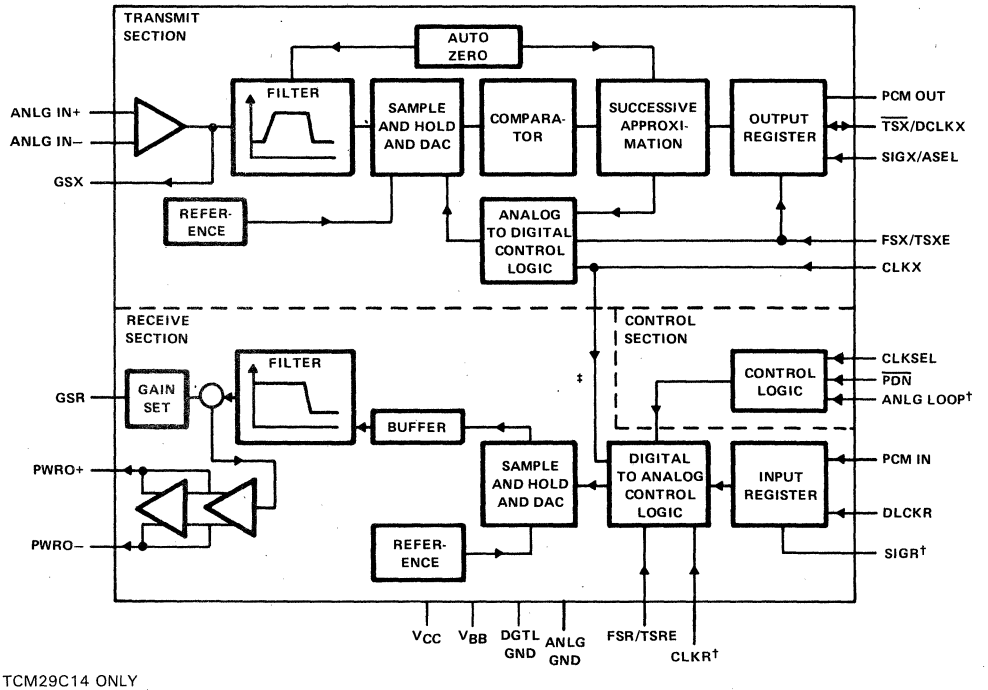
- Line Interface for Digital Transmission and Switching of T1 Carrier, PABX, and Central Office Telephone Systems
- Subscriber Line Concentrators
- Digital Encryption Systems
- Digital Voice Band Data Storage Systems
- Digital Signal Processing

These devices are designed to perform the transmit encoding (A/D conversion) and receive decoding (D/A conversion) as well as the transmit and receive filtering functions in a pulse-code-modulated system. They are intended to be used at the analog termination of a PCM line or trunk.

The TCM29C13, TCM29C14, TCM29C16, and TCM29C17 provide the bandpass filtering of the analog signals prior to encoding and after decoding. These combination devices perform the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

The TCM29C13, TCM29C14, TCM29C16, and TCM29C17 are characterized for operation from 0°C to 70°C.

functional block diagram



†TCM29C14 ONLY
‡TCM29C13, TCM29C16, AND TCM29C17 ONLY

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PIN			NAME	DESCRIPTION
TCM29C13	TCM29C14†	TCM29C16 TCM29C17		
1	1 [1]	1	V_{BB}	Most negative supply voltage; input is −5 V ±5%.
2	2 [2]	2	PWRO+	Noninverting output of power amplifier. Can drive transformer hybrids or high-impedance loads directly in either a differential or a single-ended configuration.
3	3 [3]	3	PWRO−	Inverting output of power amplifier; functionally identical with and complementary to PWRO+.
4	4 [5]		GSR	Input to the gain-setting network on the output power amplifier. Transmission level can be adjusted over a 12-dB range depending upon the voltage at GSR.
5	5 [7]	4	$\overline{PDN}$	Power-down select. The device is inactive with a TTL low-level input to this pin and active with a TTL high-level input to the pin.
6	6 [8]		CLKSEL	Clock frequency selection. Input must be connected to V_{BB}, V_{CC}, or ground to reflect the master clock frequency. When tied to V_{BB}, CLK is 2.048 MHz. When tied to ground, CLK is 1.544 MHz. When tied to V_{CC}, CLK is 1.536 MHz.
	7 [9]		ANLG LOOP	Provides loopback test capability. When this input is high, PWRO+ is internally connected to ANLG IN.
	8 [10]		SIGR	Signaling bit output, receive channel; in a fixed-data-rate mode, outputs the logical state of the 8th bit (LSB) of the PCM word in the most recent signaling frame.
7	9 [11]	5	DCLKR	Selects fixed or variable data-rate operation. When this pin is connected to V_{BB}, the device operates in the fixed-data-rate mode. When DCLKR is not connected to V_{BB}, the device operates in the variable-data-rate mode, and DCLKR becomes the receive data clock, which operates at frequencies from 64 kHz to 2.048 MHz
8	10 [12]	6	PCM IN	Receive PCM input. PCM data is clocked in on this pin on eight consecutive negative transitions of the receive data clock, which is CLKR in fixed-data-rate timing and DCLKR in variable-data-rate timing.
9	11 [13]	7	FSR/TSRE	Frame synchronization clock input/time slot enable for receive channel. In the fixed-data-rate mode, FSR distinguishes between signaling and non-signaling frames by a double- or single-length pulse, respectively. In the variable-data-rate mode, this signal must remain high for the duration of the timeslot. The receive channel enters the standby state when FSR is TTL low for 300 ms.
10	12 [14]	8	DGTL GND	Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
11	13 [15]	9	CLKR	Receive master clock and data clock for the fixed-data-rate mode. Receive master clock only for variable-data-rate mode. CLKR and CLKX are internally connected together for TCM29C13, TCM29C16, and TCM29C17.

†Pin numbers shown in square brackets are for the FN package.

PIN			NAME	DESCRIPTION
TCM29C13	TCM29C14†	TCM29C16 TCM29C17		
11	14 [16]	9	CLKX	Transmit master clock and data clock for the fixed-data-rate mode. Transmit master clock only for variable data rate mode. CLKR and CLKX are internally connected for the TCM29C13, TCM29C16, and TCM29C17.
12	15 [17]	10	FSX/TSXE	Frame synchronization clock input/time-slot enable for transmit channel. Operates independently of, but in an analagous manner to, FSR/TSRE. The transmit channel enters the standby state when FSX is low for 300 ms.
13	16 [19]	11	PCM OUT	Transmit PCM output. PCM data is clocked out on this output on eight consecutive positive transitions of the transmit data clock, which is CLKX in fixed-data-rate timing and DCLKX in variable-data-rate timing.
14	17 [21]	12	$\overline{\text{TSX}}$/DCLKX	Transmit channel time slot strobe (output) or data clock (input) for the transmit channel. In the fixed-data-rate mode, this pin is an open-drain output to be used as an enable signal for a three-state buffer. In the variable-data rate mode, DCLKX becomes the transmit data clock, which operates at TTL levels from 64 kHz to 2.048 MHz.
15	18 [22]		SIGX/ASEL	Used to select between A-law and μ-law operation. When connected to V_{BB}, A-law is selected. When connected to V_{CC} or ground, u-law is selected. When not connected to V_{BB}, it is a TTL-level input that is transmitted as the eighth bit (LSB) of the PCM word during signaling frames on the PCM OUT pin (TCM29C14 only). SIGX/ASEL is internally connected to V_{BB} on TCM29C16 and to ground on TCM29C17.
16	20 [24]	13	ANLG GND	Analog ground return for all internal voice circuits. Not internally connected to DGTL GND.
17	21 [25]		ANLG IN+	Noninverting analog input to uncommitted transmit operational amplifier. Internally connected to ANLG GND on TCM29C16 and TCM29C17.
18	22 [26]	14	ANLG IN−	Inverting analog input to uncommitted transmit operational amplifier.
19	23 [27]	15	GSX	Output terminal of internal uncommitted operational amplifier. Internally, this is the voice signal input to the transmit filter.
20	24 [28]	16	V_{CC}	Most positive supply voltage, input is 5 V ± 5%.

†Pin numbers shown in square brackets are for the FN package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 V to 15 V
Output voltage, V_O . . . . . −0.3 V to 15 V
Input voltage, V_I . . . . . −0.3 V to 15 V
Digital ground voltage . . . . . −0.3 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1375 mW
Operating free-air temperature range (under bias) . . . . . −10°C to 80°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds . . . . . 300°C

NOTES: 1. Voltage values for maximum ratings are with respect to V_{BB}.
2. For operation above 25°C free-air temperature, derate linearly to 770 mW at 80°C at the rate of 11 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)		4.75	5	5.25	V
V_{BB}	Supply voltage		−4.75	−5	−5.25	V
	DGTL GND voltage with respect to ANLG GND			0		V
V_{IH}	High-level input voltage, all inputs except CLKSEL		2.2			V
V_{IL}	Low-level input voltage, all inputs except CLKSEL				0.8	V
	Clock select input voltage	For 2.048 MHz	V_{BB}		$V_{BB}+0.5$	V
		For 1.544 MHz	0		0.5	V
		For 1.536 MHz	$V_{CC}-0.5$		V_{CC}	V
R_L	Load resistance	At GSX	10			kΩ
		At PWRO+ and/or PWRO−	300			Ω
C_L	Load capacitance	At GSX			50	pF
		AT PWRO+ and/or PWRO−			100	pF
T_A	Operating free-air temperature		0		70	°C

NOTE 3: Voltages at analog inputs and outputs, V_{CC}, and V_{BB} terminals are with respect to the ANLG GND terminal. All other voltages are referenced to the DGTL GND terminal unless otherwise noted.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

supply current, f_{DCLK} = 2.048 MHz, outputs not loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current from V_{CC}	Operating			6		mA
		Standby	FSX or FSR at V_{IL} after 300 ms		0.5		
		Power-down	$\overline{PDN}$ V_{IL} after 10 μs		0.3		
I_{BB}	Supply current from V_{BB}	Operating			−6		mA
		Standby	FSX or FSR at V_{IL} after 300 ms		0.5		
		Power-down	$\overline{PDN}$ V_{IL} after 10 μs		−0.3		
	Power dissipation	Operating			60		mW
		Standby	FSX or FSR at V_{IL} after 300 ms		5		
		Power down	$\overline{PDN}$ V_{IL} after 10 μs		3		

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (continued)

digital interface

PARAMETER			TEST CONDITONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	DX	I_{OH} = −9.6 mA	2.4			V
		SIGR	I_{OH} = −1.2 mA	2.4			
V_{OL}	Low-level output voltage at DX, TSX, SIGR		I_{OL} = 3.2 mA			0.4	V
I_{IH}	High-level input current, any digital input		V_I = 2.2 V to V_{CC}			10	μA
I_{IL}	Low-level input current, any digial input		V_I = 0 to 0.8 V			10	μA
C_i	Input capacitance				5	10	pF
C_o	Output capacitance				5		pF

transmit amplifier input

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±100	nA
Input offset voltage at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V			±25	mV
Common-mode rejection at ANLG IN+, ANLG IN−	V_I = −2.17 V to 2.17 V	55			dB
Open-loop voltage amplification at GSX		5000			
Open-loop unity-gain bandwidth at GSX			1		MHz
Input resistance at ANLG IN+, ANLG IN−		10			MΩ

receive filter output

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output offset voltage PWRO+, PWRO− (single-ended)	Relative to ANLG GND		80		mV
Output resistance at PWRO+, PWRO−			1		Ω

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

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gain and dynamic range, V_{CC} = 5 V, V_{BB} = −5 V, T_A = 25°C (unless otherwise noted) (see Notes 4, 5, and 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Encoder milliwatt response (transmit gain tolerance)		Signal input = 1.064 V rms for μ-law Signal input = 1.068 V rms for A-law		±0.04	±0.2	dBm0
Encoder milliwatt response (nominal supplies and temperature)		T_A = 0°C to 70°C, Supplies = ±5%			±0.08	dB
Digital milliwatt response (receive tolerance gain) relative to zero-transmission level point		Signal input per CCITT G.711, Output signal = 1 kHz		±0.04	±0.2	dBm0
Digital milliwatt response variation with temperature and supplies		T_A = 0°C to 70°C, Supplies = ±5%			±0.08	dB
Zero-transmission-level point, transmit channel (0 dBm0)	μ-law	R_L = 600 Ω		2.76		dBm
	A-law			2.79		
	μ-law	R_L = 900 Ω		1.00		
	A-law			1.03		
Zero-transmission-level point, receive channel (0 dBm0)	μ-law	R_L = 600 Ω		5.76		dBm
	A-law			5.79		
	μ-law	R_L = 900 Ω		4.00		
	A-law			4.03		

NOTES: 4. Unless otherwise noted, the analog input is a 0-dBm0, 1020-Hz sine wave, where 0 dBm0 is defined as the zero-reference point of the channel under test. This corresponds to an analog signal input of 1.064 V rms, or an output of 1.503 V rms.
5. The input amplifier is set for unity gain, noninverting. GSX is connected to ANLG IN−. Signal input is ANLG IN+. The digital input is a PCM bit stream generated by passing a 0-dBm0, 1020-Hz sine wave through an ideal encoder.
6. Receive output is measured single-ended in the maximum-gain configuration. To set the output amplifier for maximum gain, GSR is connected to PWRO− and the output is taken at PWRO+. All output levels are (sin x)/x corrected.

gain tracking over recommended ranges of supply voltage and operating free-air temperature, reference level = −10 dBm0

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit gain tracking error, sinusoidal input	−3 to −40 dBm0		±0.25	dB
	−40 to −50 dBm0		±0.5	
	−50 to −55 dBm0		±1.2	
Receive gain tracking error, sinusoidal input	−3 to −40 dBm0		±0.25	dB
	−40 to −50 dBm0		±0.5	
	−50 to −55 dBm0		±1.2	

noise over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Transmit noise, C-message weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		15	dBrnC0
Transmit noise, C-message weighted with eighth-bit signaling (TCM29C14 only)	ANLG IN+ = ANLG GND, ANLG IN− = GSX, 6th frame signaling		18	dBrnC0
Transmit noise, psophometrically weighted	ANLG IN+ = ANLG GND, ANLG IN− = GSX		−75	dBm0p
Receive noise, C-message weighted quiet code	PCM IN = 11111111 (μ-law) PCM IN = 10101010 (A-law) measured at PWRO+		11	dBrnC0
Receive noise, C-message weighted sign bit toggled	Input to PCM IN is zero code with sign bit toggled at 1-kHz rate		12	dBrnC0
Receive noise, psophometrically weighted	PCM = lowest positive decode level		−79	dBm0p

power supply rejection and crosstalk attenuation over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC} supply voltage rejection ratio, transmit channel	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	f = 30 to 50 kHz			−45		
V_{BB} supply voltage rejection ratio, transmit channel	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, f measured at PCM OUT		−30		dB
	f = 30 to 50 kHz			−55		
V_{CC} supply voltage rejection ratio, receive channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	f = 30 to 50 kHz			−45		
V_{BB} supply voltage rejection ratio, receive channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal = 200 mV p-p, narrow-band, f measured at PWRO+		−20		dB
	f = 30 to 50 kHz			−45		
Crosstalk attenuation, transmit-to-receive (single-ended)		ANLG IN+ = 0 dBm0, f = 1.02 kHz, unity gain, PCM IN = lowest decode level, measured at PWRO+	71			dB
Crosstalk attenuation, receive-to-transmit (single-ended)		PCM IN = 0 dBm0, f = 1.02 kHz, Measured at PCM OUT	71			dB

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

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distortion over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit signal to distortion ratio, sinusoidal input (see Note 7)	ANLG IN+ = 0 to −30 dBm0	36			dB
	ANLG IN+ = −30 to −40 dBm0	30			
	ANLG IN+ = −40 to −45 dBm0	25			
Receive signal to distortion ratio, sinusoidal input (see Note 7)	ANLG IN+ = 0 to −30 dBm0	36			dB
	ANLG IN+ = 0 to −40 dBm0	30			
	ANLG IN+ = 0 to −45 dBm0	25			
Transmit single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Receive single-frequency distortion products	AT&T Advisory #64 (3.8), Input signal = 0 dBm0			−46	dBm0
Intermodulation distortion, end-to-end Spurious out-of-band signals, end-to-end	CCITT G.712 (7.1)			−35	dBm0
	CCITT G.712 (7.2)			−49	
	CCITT G.712 (6.1)			−25	dBm0
	CCITT G.712 (9)			−40	
Transmit absolute delay time to PCM OUT	Fixed data rate, f_{CLKX} = 2.048 MHz, Input to ANLG IN+ = 1.02 kHz at 0 dBm0		245		μs
Transmit differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		170		μs
	f = 600 Hz to 100 Hz		95		
	f = 100 Hz to 2600 Hz		45		
	f = 2600 Hz to 2800 Hz		105		
Receive absolute delay time to PCM OUT	Fixed data rate, f_{CLKR} = 2.048 MHz, Digital input is DMW codes		190		μs
Receive differential envelope delay time relative to transmit absolute delay time	f = 500 Hz to 600 Hz		45		μs
	f = 600 Hz to 100 Hz		35		
	f = 1000 Hz to 2600 Hz		85		
	f = 2600 Hz to 2800 Hz		110		

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTES: 7. CCITT G.712 — Method 2.
8. CCITT G.712 — Method 1.

transmit filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input amplifier set for unity gain, Noninverting maximum gain output, Input signal at PCM IN is 0 dBm0	16.67 Hz		−30	dB
		50 Hz		−25	
		60 Hz		−23	
		200 Hz	−1.8	−0.125	
		300 Hz to 3 kHz	−0.125	0.125	
		3.3 kHz	−0.35	0.03	
		3.4 kHz	−0.7	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−32	

receive filter transfer over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Gain relative to gain at 1.02 kHz	Input signal at PCM IN is 0 dBm0	Below 200 Hz		0.125	dB
		200 Hz	−0.5	0.125	
		300 Hz to 3 kHz	−0.125	0.125	
		3.3 kHz	−0.35	0.03	
		3.4 kHz	−0.7	−0.1	
		4 kHz		−14	
		4.6 kHz and above		−30	

clock timing requirements over recommended ranges of supply voltage and operating free-air temperature (see timing diagrams)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(CLK)}$	Clock period for CLKX, CLKR (2.048-MHz systems)	488			ns
t_r, t_f	Rise and fall times for CLKX and CLKR	5		30	ns
$t_{w(CLK)}$	Pulse duration for CLKX and CLKR (see Note 9)	195			ns
$t_{w(DCLK)}$	Pulse duration for DCLK (f_{DCLK} = 64 Hz to 2.048 MHz) (see Note 9)	195			ns
	Clock duty cycle [$t_{w(CLK)}/t_{c(CLK)}$] for CLKX and CLKR	40	50	60	%

transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSX)}$	Frame sync delay time	0	$t_{c(CLK)}-100$	ns
$t_{su(SIGX)}$	Setup time before Bit 7 falling edge (TCM29C14 only)	0		ns
$t_{h(SIGX)}$	Hold time after Bit 8 falling edge (TCM29C14 only)	0		ns

propagation delay times over recommended ranges of operating conditions, fixed-data-rate mode (see timing diagrams)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{pd1}	From rising edge of transmit clock to Bit 1 data valid at PCM OUT (data enable time on time slot entry) (see Note 10)	C_L = 0 to 100 pF	0	145	ns
t_{pd2}	From rising edge of transmit clock Bit n to Bit n + 1 data valid at PCM OUT (data valid time)	C_L = 0 to 100 pF	0	145	ns
t_{pd3}	From falling edge of transmit clock Bit 8 to Bit 8 Hi-Z at PCM OUT (data float time on time slot exit) (see Note 10)	C_L = 0	60	215	ns
t_{pd4}	From rising edge of transmit clock Bit 1 to TSX active (low) (time slot enable time)	C_L = 0 to 100 pF	0	145	ns
t_{pd5}	From falling edge of transmit clock Bit 8 to TSX inactive (high) (timeslot disable time) (see Note 10)	C_L = 0	60	190	ns
t_{pd6}	From rising edge of channel time slot to SIGR update (TCM29C14 only)		0	2	μs

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, fixed-data-rate mode (see timing diagrams)

PARAMETER		MIN	MAX	UNIT
$t_{d(FSR)}$	Frame sync delay time	0	$t_{c(CLK)}-100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 7 falling edge (TCM29C14 only)	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 8 falling edge (TCM29C14 only)	60		ns

†All typical values are at V_{BB} = −5 V, V_{CC} = 5 V, and T_A = 25°C.

NOTES: 9. FSX CLK must be phase locked with the CLKX. FSR CLK must be phase locked with CLKR.
10. Timing parameters t_{pd1}, t_{pd3}, and t_{pd5} are referenced to the high-impedance state.

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transmit timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

	PARAMETER	MIN	MAX	UNIT
$t_{d(TSDX)}$	Timeslot delay time from DCLKX (see Note 11)	140	$t_{d(DCLKX)} - 140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)} - 100$	ns
$t_{c(DCLKX)}$	Clock period for DCLKX	488	15620	ns

propagation delay times over recommended ranges of operating conditions, variable-data-rate mode (see Note 12 and timing diagrams)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd7}	Data delay time from DCLKX	C_L = 0 to 100 pF	0	100	ns
t_{pd8}	Data delay from timeslot enable to PCM OUT	C_L = 0 to 100 pF	0	50	ns
t_{pd9}	Data delay from time slot disable to PCM OUT	C_L = 0 to 100 pF	0	80	ns
t_{pd10}	Data delay time from FSX	$t_{d(TSDX)}$ = 80 ns	0	140	ns

receive timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode (see timing diagrams)

	PARAMETER	MIN	MAX	UNIT
$t_{d(TSDR)}$	Timeslot delay time from DCLKR (see Note 13)	140	$t_{d(DCLKR)} - 140$	ns
$t_{d(FSX)}$	Frame sync delay time	100	$t_{c(CLK)} - 100$	ns
$t_{su(PCM\ IN)}$	Setup time before Bit 7 falling edge	10		ns
$t_{h(PCM\ IN)}$	Hold time after Bit 8 falling edge	60		ns
$t_{c(DCLKR)}$	Clock period for DCLKR	488	15620	ns
	Timeslot end receive time	0		ns

64-kilobit operation timing requirements over recommended ranges of supply voltage and operating free-air temperature, variable-data-rate mode

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{FSLX}	Transmit frame sync minimum down time	FSX = TTL high for remainder of frame	488		ns
t_{FSLR}	Receive frame sync minimum down time	FSR = TTL high for remainder of frame	1952		ns
t_{DCLK}	Pulse duration, data clock			10	μs

NOTES: 11. t_{FSLX} minimum requirement overrides the $t_{d(TSDX)}$ maximum requirement for 64-kHz operation.
12. Timing parameters t_{pd8} and t_{pd9} are referenced to a high-impedance state.
13. t_{FSLR} minimum requirement overrides the $t_{d(TSDR)}$ maximum requirement for 64-kHz operation.

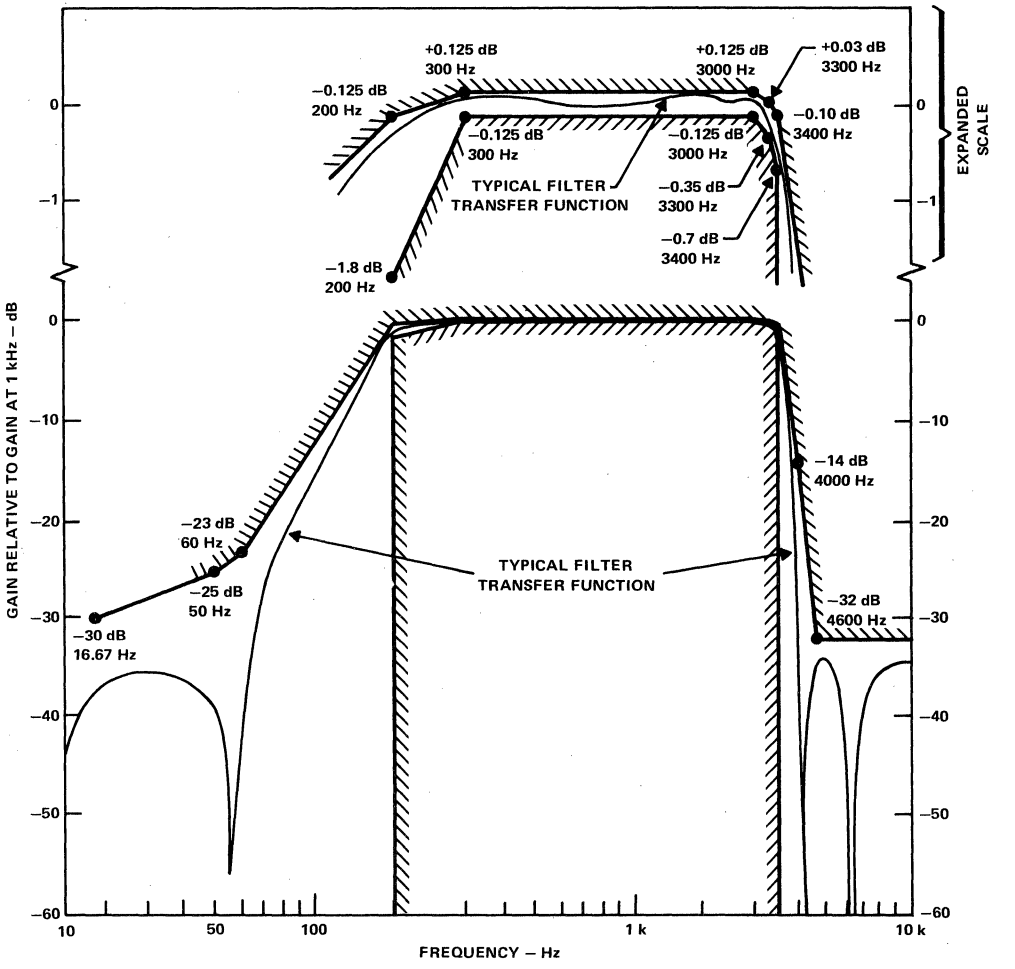

FIGURE 1. TRANSFER CHARACTERISTICS OF THE TRANSMIT FILTER

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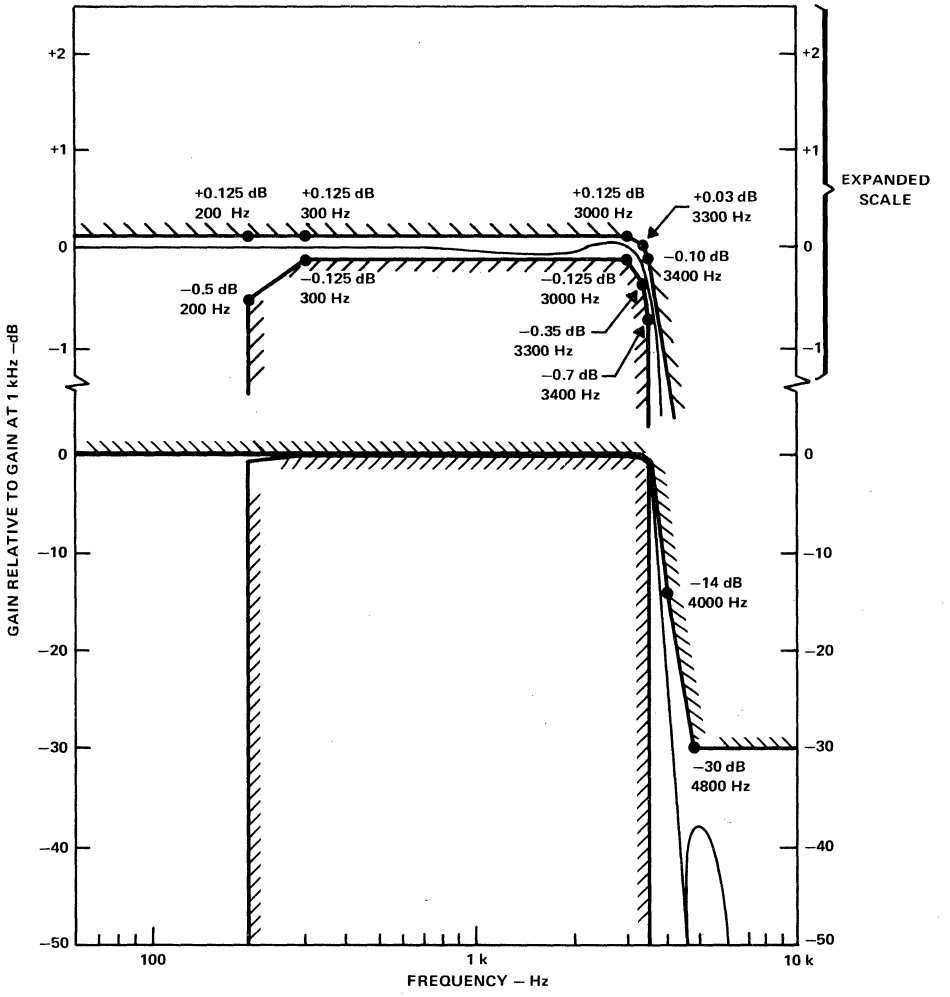

NOTE: This is a typical transfer function of the receive filter component.

FIGURE 2. TRANSFER CHARACTERISTIC OF THE RECEIVE FILTER

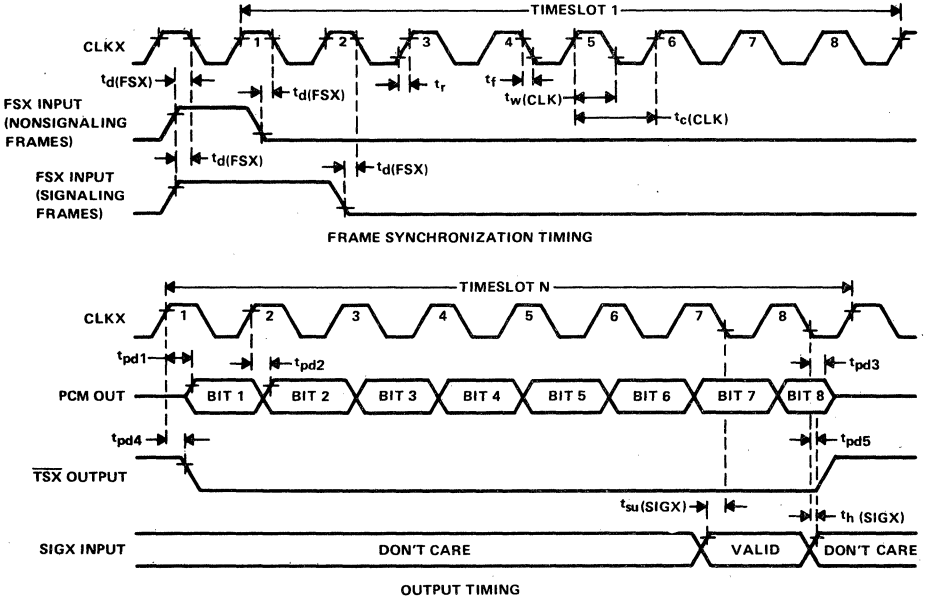

FIGURE 3. TRANSMIT TIMING (FIXED-DATA-RATE)

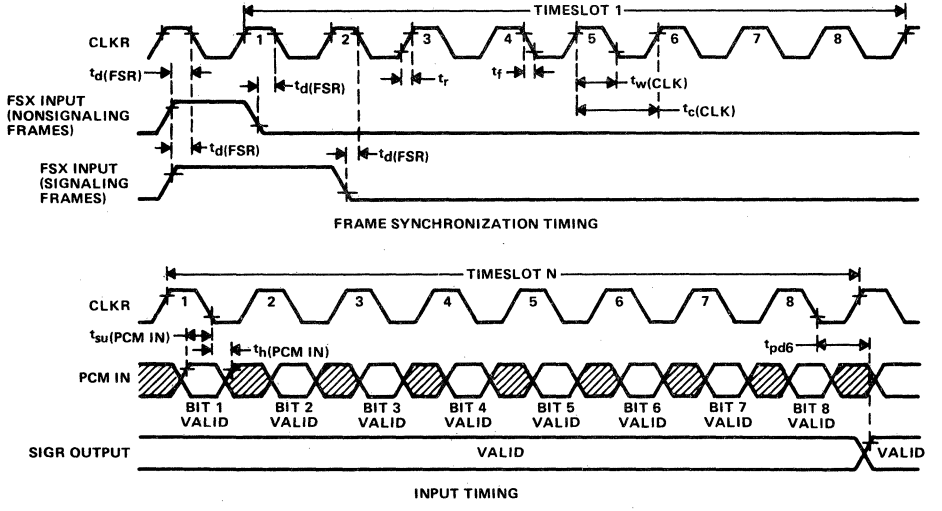

FIGURE 4. RECEIVE TIMING (FIXED-DATA-RATE)

NOTE: Inputs are driven from 0.45 V to 2.4 V. Time intervals are referenced to 2 V if the high level is indicated and 0.8 V if the low level is indicated.

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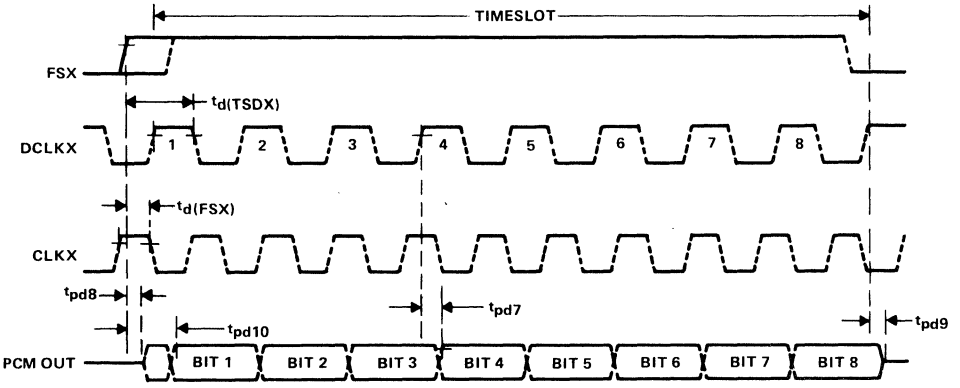
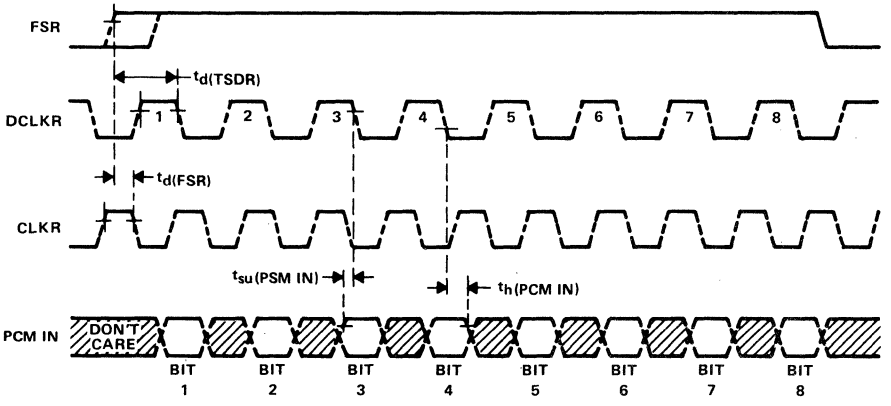


FIGURE 5. TRANSMIT TIMING (VARIABLE-DATA-RATE)



NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{pd8} and t_{pd9}, which reference a high-impedance state.

FIGURE 6. RECEIVE TIMING (VARIABLE-DATA-RATE)

GENERAL OPERATION

system reliability features

The TCM29C13, TCM29C14, TCM29C16, or TCM29C17 is powered up in four steps:

V_{CC} and V_{BB} supply voltages are applied.
All clocks are connected.
TTL high is applied to $\overline{PDN}$.
FSX and/or FSR synchronization pulses are applied.

On the transmit channel, digital outputs PCM OUT and $\overline{TSX}$ are held in a high-impedance state for approximately four frames (500 μs) after power up or application of V_{BB} or V_{CC}. After this delay, PCM OUT, $\overline{TSX}$, and signaling are functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 60 ms to reach their equilibrium value due to the autozero circuit settling time. Thus valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIGR is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}. SIGR will remain low until it is updated by a signaling frame.

To further enhance system reliability, PCM OUT and $\overline{TSX}$ will be placed in a high-impedance state approximately 20 μs after an interruption of CLKX. SIGR will be held low approximately 20 μs after an interruption of CLKR. These interruptions could possibly occur with some kind of fault condition.

power-down and standby operations

To minimize power consumption, a power-down mode and three standby modes are provided.

For power down, an external low signal is applied to the $\overline{PDN}$ pin. It is not sufficient to remove the high voltage to $\overline{PDN}$. In the absence of a signal, the $\overline{PDN}$ pin floats to high and the device remains active. In the power-down mode, the average power consumption is reduced to an average of 5 mW.

The standby modes give the user the option of putting the entire device on standby, putting only the transmit channel on standby, or putting only the receive channel on standby. To place the entire device on standby, both FSX and FSR are held at low. For transmit-only operation, FSX is high and FSR is held low. For receive-only operation, FSR is high and FSX is held low. See Table 1 for power down and standby procedures.

TABLE 1. POWER DOWN AND STANDBY PROCEDURES

DEVICE STATUS	PROCEDURE	TYPICAL POWER CONSUMPTION	DIGITAL OUTPUT STATUS
Power down	$\overline{PDN}$ is low	3 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to low within 10 μs.
Entire device on standby	FSX and FSR are low	3 mW	$\overline{TSX}$ and PCM OUT are in a high-impedance state; SIGR goes to low within 300 ms.
Only transmit on standby	FSX is low, FSR is high	50 mW	$\overline{TSX}$ and PCM OUT are placed in a high-impedance state within 300 ms.
Only receive on standby	FSR is low, FSX is high	30 mW	SIGR is placed in a high-impedance state within 300 ms.

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fixed-data-rate timing (see Figure 7)

Fixed-data-rate timing is selected by connecting DCLKR to V_{BB}. It uses master clocks CLKX and CLKR, frame synchronizer clocks FSX and FSR, and output $\overline{TSX}$. FSX and FSR are 8-kHz inputs that set the sampling frequency and distinguish between signaling and nonsignaling frames by their pulse durations. A frame synchronization pulse one master clock period long designates a nonsignaling frame, while a double-length sync pulse enables the signaling function (TCM29C14 only). Data is transmitted on the PCU OUT pin on the first eight positive transitions of CLKX following the rising edge of FSX. Data is received on the PCM IN pin on the first eight falling edges of CLKR following FSX. A digital-to-analog (D/A) conversion is performed on the received digital word and the resulting analog sample is held on an internal sample-and-hold capacitor until transferred to the receive filter.

The clock selection pin (CLKSEL) is used to select the frequency of CLKX and CLKR (TCM29C13 and TCM29C14 only). The TCM29C13 and TCM29C14 fixed-data-rate mode can operate with frequencies of 1.536 MHz, 1.544 MHz, or 2.048 MHz. The TCM29C16 and TCM29C17 fixed data rate mode operates at 2.048 MHz only.

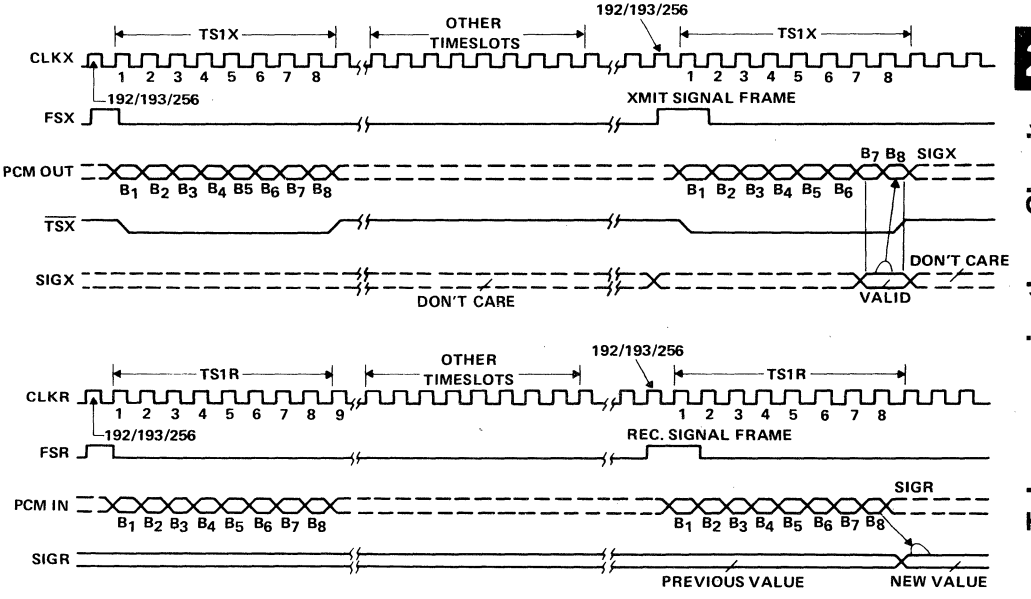

FIGURE 7. SIGNALING TIMING (FIXED-DATA-RATE ONLY)

variable data rate timing

Variable-data-rate timing is selected by connecting DCLKR to the bit clock for the receive PCM highway rather than to V_{BB}. It uses master clocks CLKX and CLKR, bit clocks DCLKX and DCLKR, and frame synchronization clocks FSX and FSR.

Variable-data-rate timing allows for a flexible data frequency. The frequency of the bit clocks can be varied from 64 kHz to 2.048 MHz. The bit clocks can be asynchronous in the TCM29C14, but must be synchronous in the TCM29C13, TCM29C16, and TCM29C17. Master clocks in types TCM29C13 and TCM29C14 are restricted to frequencies of operation of 1.536 MHz, 1.544 MHz, or 2.048 MHz as in the fixed-data-rate timing mode. The master clock for the TCM29C16 and TCM29C17 is restricted to 2.048 MHz.

While FSX/TSXE input is high, PCM data is transmitted from PCM OUT onto the highway on the next eight consecutive positive transitions of DCLKX. Similarly, while the FSR/TSRE input is high, the PCM word is received from the highway by PCM IN on the next eight consecutive negative transitions of DCLKR.

The transmitted PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as DCLKX is pulsed and FSX is held high. This feature, which allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, is available only with variable-data-rate timing. Signaling is allowed only in the fixed-data-rate mode because the variable-data-rate mode provides no means with which to specify a signaling frame.

signaling

The TCM29C14 (only) provides 8th-bit signaling in the fixed-data-rate timing mode. Transmit and receive signaling frames are independent of each other and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the signal present on SIGX is substituted for the least significant bit (LSB) of the encoded PCM word. In a receive signaling frame, the codec will decode the seven most significant bits in accordance with CCITT G.733 recommendations, and output the logical state of the LSB on the SIGR pin until it is updated in the next signaling frame. Timing relationships for signaling operations are shown n Figure 9. The signaling path is used to transmit digital signaling information such as ring control, rotary dial pulses, and off-hook and disconnect supervision. The voice path is used to transmit prerecorded messages as well as the call progress tones; dial tone, ring-back tone, busy tone, and re-order tone.

asynchronous operation

The TCM29C14 can be operated with asynchronous clocks in either the fixed- or variable-data-rate modes. In order to avoid crosstalk problems associated with special interrupt circuits, the design of the TCM29C13 and TCM29C14 includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow completely independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame. Specifically, in the variable-data-rate mode the rising edge of CLKX must occur within $t_{d(FSX)}$ ns before the rise of FSX, while the leading edge of DCLKX must occur within t_{TSDX} ns of the rise of FSX. CLKX and DCLKX are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (see variable data rate timing diagrams). This approach requires the provision of two separate master clocks but avoids the use of a synchronizer, which can cause intermittent data conversion errors.

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analog loopback

A distinctive feature of the TCM29C14 is its analog loopback capability. With this feature, the user can test the line circuit remotely by comparing the signals sent into the receive channel (PCM IN) with those generated on the transmit channel (PCM OUT). The test is accomplished by sending a control signal that internally connects the analog input and output ports. WhenANLG LOOP is TTL high, the receive output (PWRO+) is internally connected to ANLG IN+, GSR is internally connected to PWRO−, and ANLG IN− is internally connected to GSX (see Figure 8).

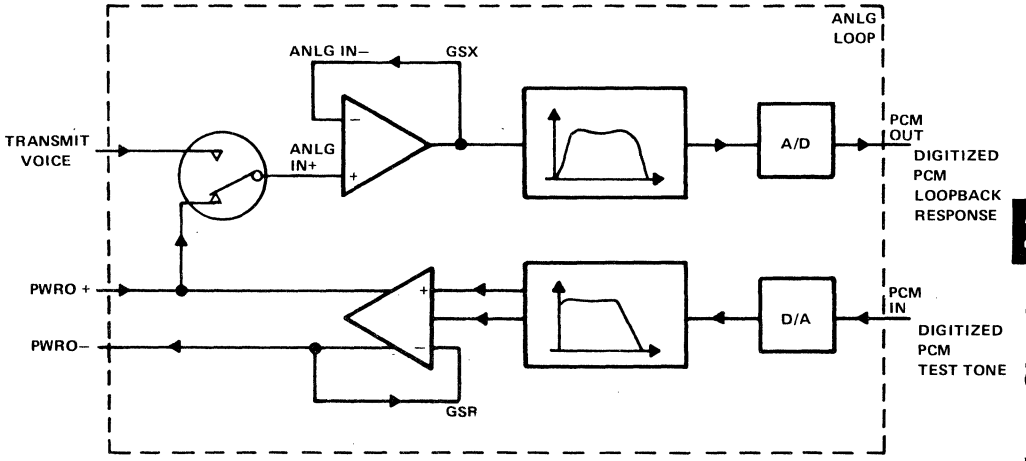

FIGURE 8. TCM29C14 ANALOG LOOPBACK CONFIGURATION

Due to the difference in the transmit and receive transmission levels, a 0 dBmO code into PCM IN will emerge from PCM OUT as a 3-dBmO code, an implicit gain of 3 dB. Because of this, the maximum signal that can be tested by analog loopback is 0 dBmO.

precision voltage references

No external components are required with the TCM29C13, TCM29C14, TCM29C16, and TCM29C17 to provide the voltage references. Voltage references that determine the gain and dynamic range characteristics of the device are generated internally. A difference in subsurface charge density between two suitably implanted MOS devices is used to derive a temperature- and bias-stable reference voltage. These references are calibrated during the manufacturing process.Separate references are supplied to the transmit and receive sections, and each is calibrated independently. Each reference value is then further trimmed in the gain setting operational amplifiers to a final precision value. Manufacturing tolerances can be achieved of typically ±0.04 dB in absolute gain for each half channel, providing the user a significant margin to compensate for error in other board components.

conversion laws

The TCM29C13 and TCM29C14 provide pin-selectable μ-law operation as specified by CCITT G.711 recommendation. A-law operation is selected when the ASEL pin is connected to V_{BB}. Signaling is not allowed during A-law operation. The TCM29C16 is μ-law only. The TCM29C17 is A-law only.

The μ-law operation is effectively selected by not selecting A-law operation. If the ASEL pin is connected to V_{CC} or GND, the device is in μ-law operation. If μ-law operation is selected, SIGX is a TTL-level input that can be used in the fixed data rate timing mode to modify the LSB of the PCM output is signaling frames.

transmit operation

transmit filter

The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. the load impedance to ground (ANLG GND) at the amplifier output (GSX) must be greater than 10 kΩ in parallel with less than 50 pF. The input signal on the ANLG IN + pin can be either ac or dc coupled. The input operational amplifier can also be used in the inverting mode or differential amplifier mode.

A low-pass antialiasing section is included on the device. This section provides 35-dB attenuation at the sampling frequency. No external components are required to provide the necessary antialiasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation that fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712. The TCM29C13, TCM29C14, TCM29C16, and TCM29C17 specifications meet or exceed digital class 5 central office switching systems requirements.

A high-pass section configuration was chosen to reject low-frequency noise from 50- and 60-Hz power lines, 17-Hz European electric railroads, ringing frequencies and their harmonics, and other low-frequency noise. Even with the high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder performs an analog-to-digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clocks bits of the next frame.

The autozero circuit corrects for dc offset on the input signal to the encoder. The autozero circuit uses the sign bit averaging technique. The sign bit from the encoder output is long-term averaged and subtracted from the input to the encoder. All dc offset is removed from the encoder input waveform.

receive operation

decoding

The serial PCM word is received at the PCM IN pin on the first ight data clock bits of the frame. Digital-to-analog conversion is performed and the corresponding analog sample is held on an internal sample-and-hold capacitor. This sample is transferred to the receive filter.

receive filter

The receive section of the filter provides passband flatness and stopband rejection that fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin x)/x response of such decoders.

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receive output power amplifiers

A balanced output amplifier is provided to allow maximum flexibility in output configuration. Either of the two outputs can be used single-ended (i.e., referenced to ANLG GND) to drive single-ended loads. Alternatively, the differential output will directly drive a bridged load. The output stage is capable of driving loads as low as 300 ohms single-ended to a level of 12 dBm or 600 ohms differentially to a level of 15 dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GSR input. GSR is internally connected to an analog gain-setting network. When GSR is connected to PWRO−, the receive level is at maximum. When GSR is connected to PWRO+, the level is minimum. The output transmission level is adjusted between 0 and −12 dB as GSR is adjusted (with an adjustable resistor) between PWRO+ and PWRO−.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions (i.e., when the digital input at PCM IN is the eight-code sequence specified in CCITT recommendation G.711).

TYPICAL APPLICATION DATA

output gain set design considerations (see Figure 9)

PWRO+ and PWRO− are low-impedance complementary outputs. The voltages at the nodes are:

V_{O+} at PWRO+
V_{O-} at PWRO−
$V_{OD} = V_{O+} - V_{O-}$ (total differential response)

R1 and R2 are a gain-setting resistor network with the center tap connected to the GSR input.

A value greater than 10 kΩ and less than 100 kΩ for R1 + R2 is recommended because of the following:

The parallel combination of R1 + R2 and R_L sets the total loading.
The total capacitance at the GSR input and the parallel combination of R1 and R2 define a time constant that has to be minimized to avoid inaccuracies.

V_A represents the maximum available digital milliwatt output response (V_A = 3.06 V rms).

$$V_{OD} = A \cdot V_A$$

$$\text{Where } A = \frac{1 + (R1/R2)}{4 + (R1/R2)}$$

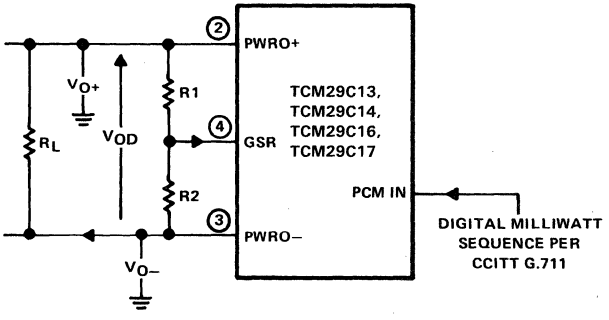

FIGURE 9. GAIN-SETTING CONFIGURATION

D2866, AUGUST 1985—REVISED FEBRUARY 1986

NOT RECOMMENDED FOR NEW DESIGN

For new design, refer to TCM3105

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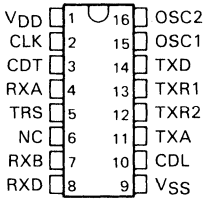
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TCM3101 is a single-chip asynchronous Frequency Shift Keying (FSK) modem that uses silicon gate CMOS technology to implement a switched capacitor architecture. It is pin selectable (TXR1, TXR2, and TRS inputs) for a wide range of transmit/receive baud rates and is compatible with the applicable Bell 202 or CCITT V23 specifications. Operation is fully reversible, thereby allowing both forward and backward channels to be used simultaneously.

The transmitter is a programmable frequency synthesizer that provides two output frequencies (on TXA), representing the 'marks' and 'spaces' of the digital signal present on the TXD input.

The receive section is responsible for the demodulation of the analog signal appearing at the RXA input and is based on the principle of frequency to voltage conversion. This section contains a group delay equalizer (to correct phase distortion), automatic gain control, carrier detect level adjustment, and bias distortion adjustment, thereby optimizing performance and giving the lowest possible bit error rate.

Carrier-detect information is given to the system by means of the carrier-detect circuits, which set a flag on the CDT output if the level of received in-band energy falls below a value set on the CDL input for a specified minimum duration.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN NO.	PIN NAME	DESCRIPTION
1	V_{DD}	Positive supply voltage
2	CLK	Output for a continuous clock signal output at 19.11 kHz (9.56 kHz for CCITT V23 600 baud)
3	CDT	Carrier Detect Output, a low-level output that indicates carrier failure
4	RXA	Receive Analog Input to which the received line signal must be ac coupled
5	TRS	Transmit/Receive Standard Select Input, which, with TXR1 and TXR2, sets the standard bit rates and mark/space frequencies
6	NC	No internal connection
7	RXB	Receive Bias Adjust for external adjustment of the decision threshold of the final comparator to minimize bias distortion
8	RXD	Receiver Digital Output for the demodulated received data in positive logic. The high logic level is a mark and the low logic level is a space.
9	V_{SS}	Supply voltage (normally ground), connected to substrate
10	CDL	Carrier Detect Level Adjust for external adjustment of carrier detect threshold
11	TXA	Transmit Analog Output for the modulated signal, which must be ac coupled
12	TXR2	Bit Rate Select 2 input, which, along with TXR1 and TRS, sets the bit rates and mark/space frequencies
13	TXR1	Bit Rate Select 1 input, which, along with TXR2 and TRS, sets the bit rates and mark/space frequencies
14	TXD	Transmit Digital Input for input data to the transmitter in positive logic. The high logic level is a mark and the low logic level is a space. The data can be accepted at any speed from zero to the selected speed and may be totally asynchronous.
15	OSC1	Oscillator connections. The crystal (typically 4.4336 MHz) is connected to these pins. If an external clock is used, OSC1 is left open and the clock is connected to OSC2.
16	OSC2	

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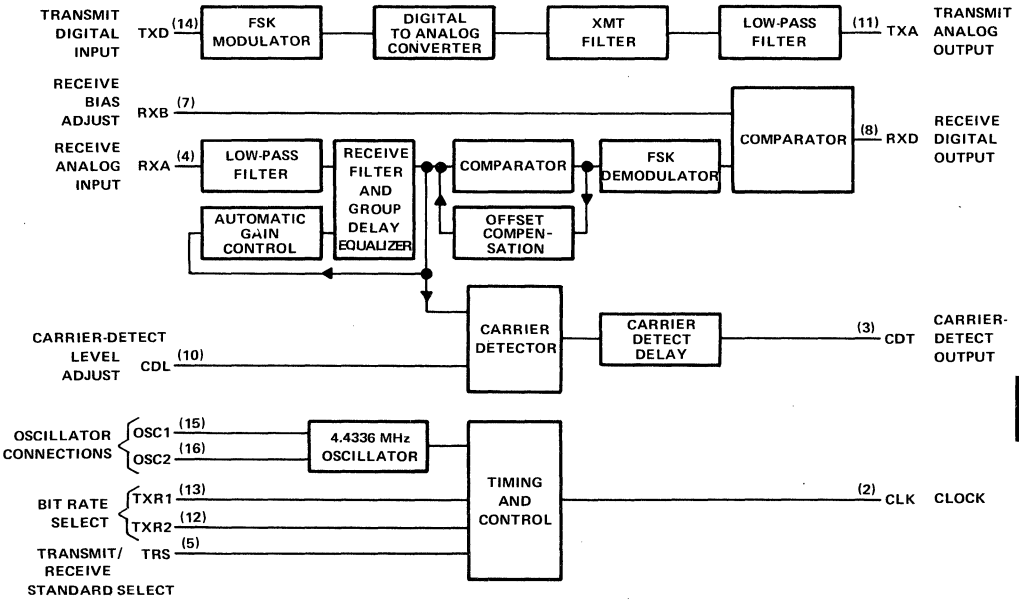
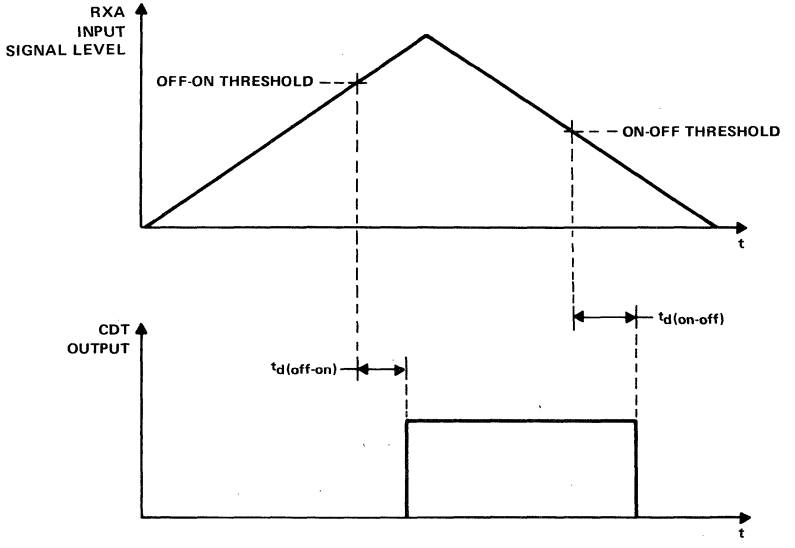
functional block diagram



timing diagram



absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 10 V
Input voltage, V_I (any input) . . . . . −0.3 to V_{DD}
Operating free-air temperature range . . . . . −10°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Clock frequency, f_{clock}	4.4334	4.4336	4.4338	MHz
Supply voltage, V_{DD}	4	5	5.5	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Analog input level, peak-to-peak (ac coupled)		0.3	0.78	V
Analog load impedance at TXA	50			kΩ
Operating free-air temperature range, T_A	−10		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-Level output voltage	RXD, CDT, CLK	I_{OH} = −100 μA,	V_{DD} = 5 V	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	RXD, CDT, CLK	I_{OL} = 1.6 mA,	V_{DD} = 5 V	V_{SS}		0.4	V
	Analog output voltage level, peak-to-peak		V_{DD} = 4 V	R_L = 50 kΩ, C_L = 100 pF		1.3		V
			V_{DD} = 5 V		1.4	1.6	2	
			V_{DD} = 5.5 V			1.75		
	Adjust voltage	RXB	V_{DD} = 5 V		2.5	2.7	3	V
		CDL			2	3.2	4	
	Analog output dc offset					$V_{DD}/2$		V
	Digital input current		V_I = 0 to V_{DD}				±1	μA
	Analog input current						±15	μA
	Bias input current	RXB, CDL				100	150	μA
I_{DD}	Supply current		V_{DD} = 4 V			2	4	mA
			V_{DD} = 5 V			4	6	
			V_{DD} = 5.5 V			6	8	
C_i	Input capacitance, all inputs		f = 1 MHz			10		pF
C_o	Output capacitance, all outputs		f = 1 MHz			10		pF
	Phase jitter						200	μs
	Bias distortion†						15%	
	Carrier detect threshold, off-on‡				−45.5		−43	dBm
	Carrier detect threshold, on-off‡				−48		−45.5	dBm
	Carrier detect hysteresis				2.5	2.8		dBm
$t_{d(off-on)}$	Carrier detect delay time		RX = 600 or 1200 bps		12		25	ms
$t_{d(on-off)}$	Carrier detect delay time				12		20	ms

†Bias distortion is the departure from a 50% duty cycle when a series of alternating mark and space tones are received.
‡This is the threshold with the CDL input properly adjusted.

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PRINCIPLES OF OPERATION

The TCM3101 FSK modem is made up of four functional circuits. The circuits are the transmitter, the receiver, a carrier detector, and control and timing (See Figure 1).

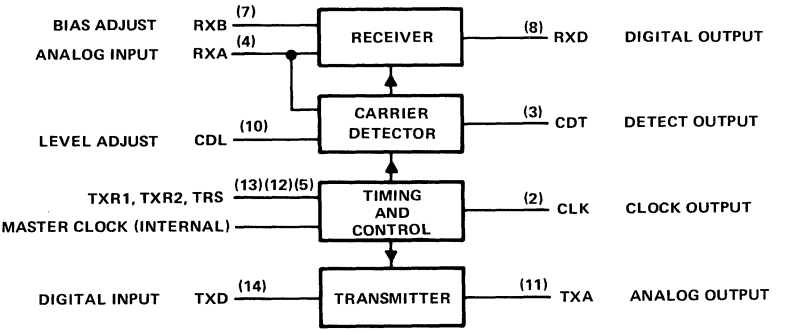

FIGURE 1. TCM3101 SYSTEM PARTITIONING

transmitter

The transmitter comprises a phase coherent FSK modulator, a transmit filter, and a transmit amplifier. The modulator is a programmable frequency synthesizer that derives the output frequencies by variable division of the oscillator frequency (4.4336 MHz). The division ratio is set by the states of the Transmit/Receive Standard input (TRS), the Bit Rate Select inputs (TXR1 and TXR2), and the Digital Data input (TXD).

The transmit frequency assignments are given in Table 1. The data convention is that a high logic level equals a mark and a low logic level equals a space.

TABLE 1. TRANSMIT FREQUENCY ASSIGNMENTS

TRS	STANDARD	TXR1	TXR2	TRANSMITTER BIT RATE	TXD	TX FREQUENCY (Hz)
L or H	CCITT V23	H	L	75	H	M 390
					L	S 450
		L	H	600	H	M 1300
					L	S 1700
		L	L	1200	H	M 1300
					L	S 2100
CLK	BELL 202	H	L	150	H	M 387
					L	S 487
		L	X	1200	H	M 1200
					L	S 2200
X		H	H	0	X	TRANSMITTER DISABLED

A switched-capacitor low-pass filter limits the harmonics and noise outside the transmit band and the characteristics of this filter are set by the frequency select inputs as previously described. The harmonics introduced by the transmit filter clock are removed by a continuous low-pass filter.

The transmitter output level varies with power supply voltage and so must be compensated in the 2-wire to 4-wire converter to give a constant output level to the line.

receiver

A continuous low-pass anti-aliasing filter is followed by the receive amplifier, which automatically controls the gain to give a constant output level from the receive filter. The receive filter limits the bandwidth of the signal presented to the demodulator, reducing out-of-band interference, and has very high rejection of 75- and 150-baud backward channel frequencies. These are typically present at much higher levels than the received signal. The receiver bit rate assignments are given in Table 2.

TABLE 2. RECEIVER BIT RATE ASSIGNMENTS

TRS	STANDARD	RECEIVE BIT RATE	CLK FREQUENCY (kHz)
H	CCITT V23	600	9.56
L	CCITT V23	1200	19.11
CLK	BELL 202		

The group delay equalizer is a switched-capacitor network that compensates the delay introduced by the receive filter and the network. The output from the equalizer is then limited to give an FSK modulated squarewave that is presented to the demodulator.

The demodulator is an edge-triggered multivibrator that triggers off positive- and negative-going edges. The output of the demodulator is, therefore, a stream of constant-length pulses at a frequency that is double the frequency of the limited input signal. The dc component of this signal is proportional to the received frequency and is extracted by a switched-capacitor, low-pass, post-demodulator filter.

The variation of dc level with received frequency is presented to a comparator that slices at a level externally fixed by the RXB bias adjustment pin. This voltage depends on received bit rate and internal offsets. The comparator output is then the received data at the RXD output.

carrier detect

The carrier detect circuits comprise an energy detector and digital delay. The energy detector compares the total signal level at the output of the receive filter to an externally set threshold level on the CDL input. The comparator has a 2.5-dB hysteresis and a delay to allow for momentary signal loss and to prevent oscillation. The output of the detector is available on the CDT pin where a high level indicates that a carrier is present.

control and timing

An on-chip oscillator runs from an external 4.4336-MHz crystal connected between the OSC1 and OSC2 pins or an external signal driving OSC1. A clock signal equal to 16 times the selected receive bit rate is available on the CLK output.

The single-supply rail means that all analog functions are referenced to an internally generated reference. All analog inputs and output must be ac coupled.

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TYPICAL APPLICATION INFORMATION

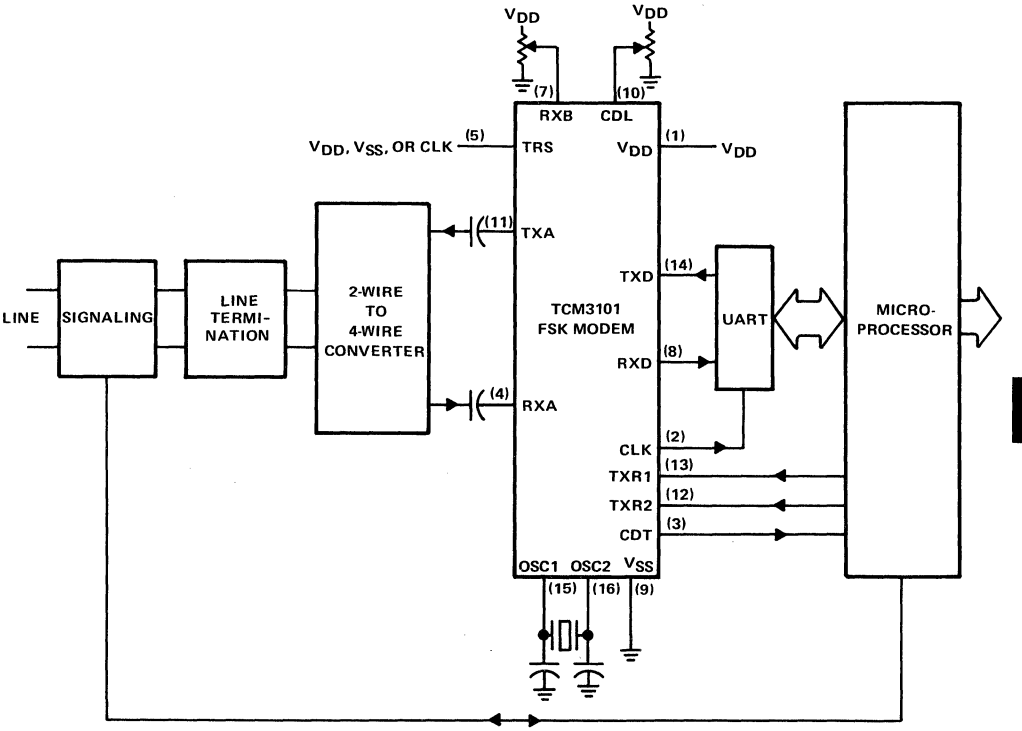

FIGURE 2. TYPICAL SYSTEM CONFIGURATION

TYPICAL APPLICATION INFORMATION

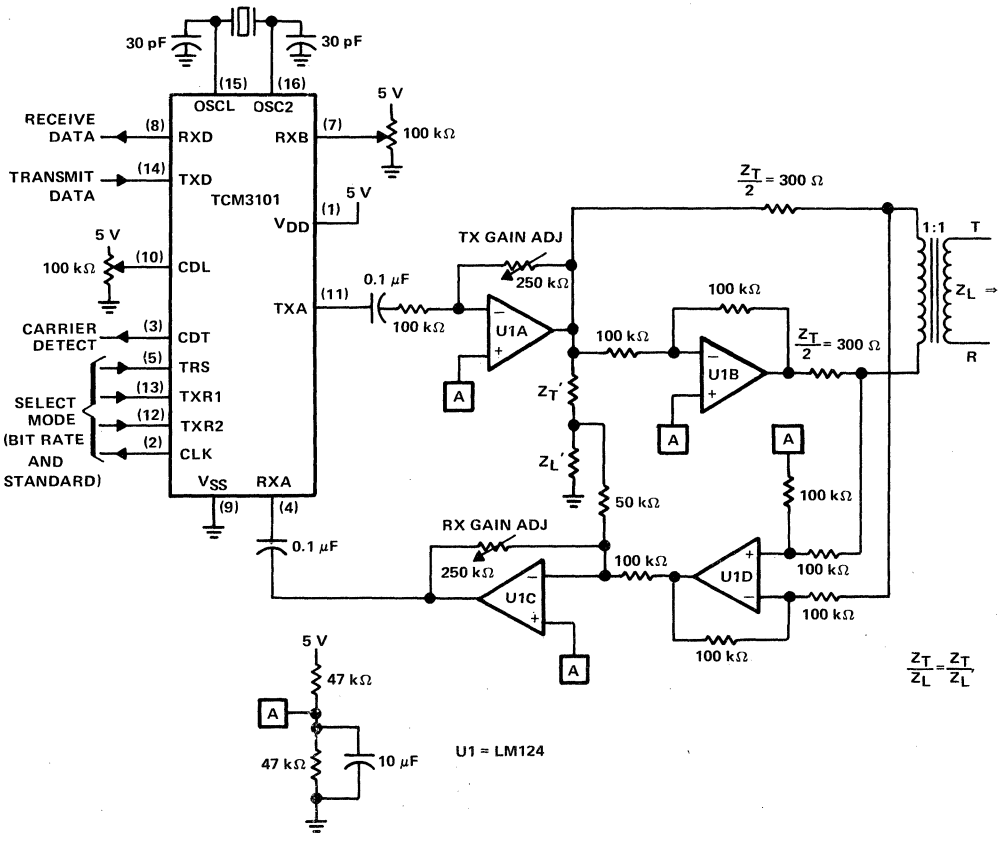

FIGURE 3. TELEPHONE LINE INTERFACE CIRCUIT

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TYPICAL APPLICATION INFORMATION

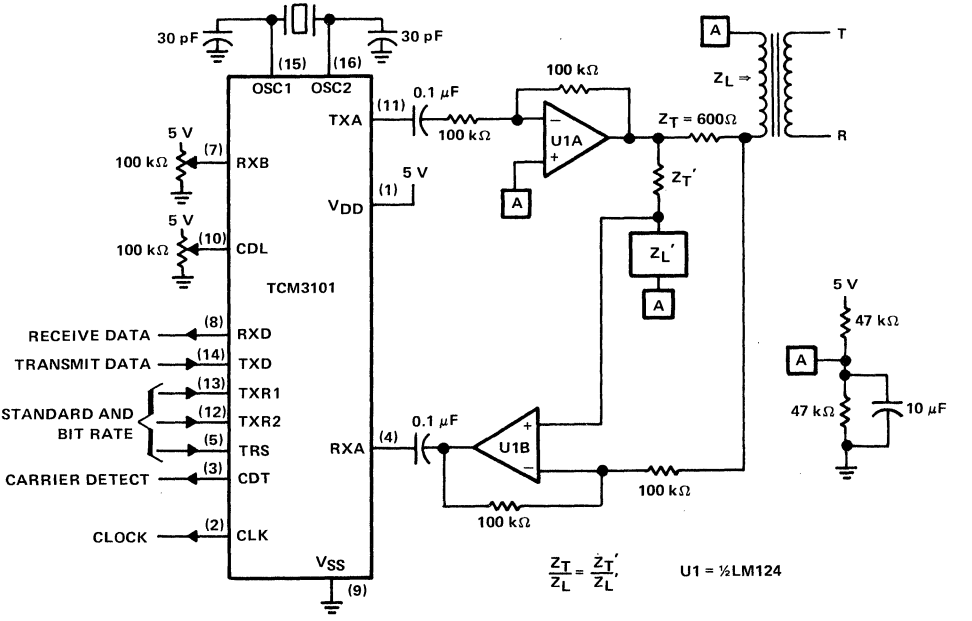
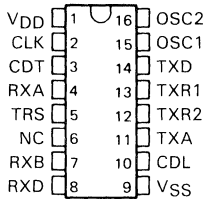


FIGURE 4. SIMPLIFIED TELEPHONE LINE INTERFACE CIRCUIT

D2662, NOVEMBER 1985—REVISED APRIL 1986

- **Single-Chip Frequency-Shift-Keying (FSK) Modem**
- **Meets Both Bell 202 and CCITT V23 Specifications**
- **Transmit Modulation at 75, 150, 600, and 1200 Baud**
- **Receive Demodulation at 5, 75, 150, 600, and 1200 Baud**
- **Half-Duplex Operation Up to 1200 Baud Transmit and Receive**
- **Full-Duplex Operation Up to 1200 Baud Transmit and 150 Baud Receive**
- **On-Chip Group Delay Equalization and Transmit/Receive Filtering**
- **Carrier-Detect-Level Adjustment and Carrier-Fail Output**
- **Single 5-V Power Supply**
- **Low Power Consumption**
- **Reliable CMOS Silicon Gate Technology**

J DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM3105 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem that uses silicon gate CMOS technology to implement a switched capacitor architecture. It is pin selectable (TXR1, TXR2, and TRS inputs) for a wide range of transmit/receive baud rates and is compatible with the applicable BELL 202 or CCITT V23 standards. Operation is fully reversible, thereby allowing both forward and backward channels to be used simultaneously.

The transmitter is a programmable frequency synthesizer that provides two output frequencies (on TXA), representing the 'marks' and 'spaces' of the digital signal present on the TXD input.

The receive section is responsible for the demodulation of the analog signal appearing at the RXA input and is based on the principle of frequency-to-voltage conversion. This section contains a group delay equalizer (to correct phase distortion), automatic gain control, carrier detect level adjustment, and bias distortion adjustment, thereby optimizing performance and giving the lowest possible bit error rate.

Carrier-detect information is given to the system by means of the carrier-detect circuits, which set a flag on the CDT output if the level of received in-band energy falls below a value set on the CDL input for a specified minimum duration.

The TCM3105JE is characterized for operation from −40°C to 85°C. The TCM3105JL is characterized for operation from 0°C to 70°C.

PIN FUNCTIONAL DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{DD}	Positive supply voltage
2	CLK	Output for a continuous clock signal at 16 times the highest selected (transmit or receive) bit rate
3	CDT	Carrier-Detect Output. A low-level output indicates carrier failure
4	RXA	Receive Analog Input to which the received line signal must be ac coupled
5	TRS	Transmit/Receive Standard Select Input, which, with TXR1 and TXR2, sets the standard bit rates and mark/space frequencies
6	NC	No internal connection
7	RXB	Receive Bias Adjust for external adjustment of the decision threshold of the final comparator to minimize bias distortion
8	RXD	Receiver Digital Output for the demodulated received data in positive logic. The high logic level is a mark and the low logic level is a space.
9	V_{SS}	Most negative supply voltage (normally ground); connected to substrate
10	CDL	Carrier Detect Level Adjust for external adjustment of carrier detect threshold
11	TXA	Transmit Analog Output for the modulated signal, which must be ac coupled
12	TXR2	Bit Rate Select 2 input, which, along with TXR1 and TRS, sets the bit rates and mark/space frequencies
13	TXR1	Bit Rate Select 1 input, which, along with TXR2 and TRS, sets the bit rates and mark/space frequencies
14	TXD	Transmit Digital Input for input data to the transmitter in positive logic. The high logic level is a mark and the low logic level is a space. The data can be accepted at any speed from zero to the selected speed and may be totally asynchronous.
15 16	OSC1 OSC2	Oscillator connections. The crystal (typically 4.4336 MHz) is connected to these pins. If an external clock is used, OSC1 is left open and the clock is connected to OSC2.

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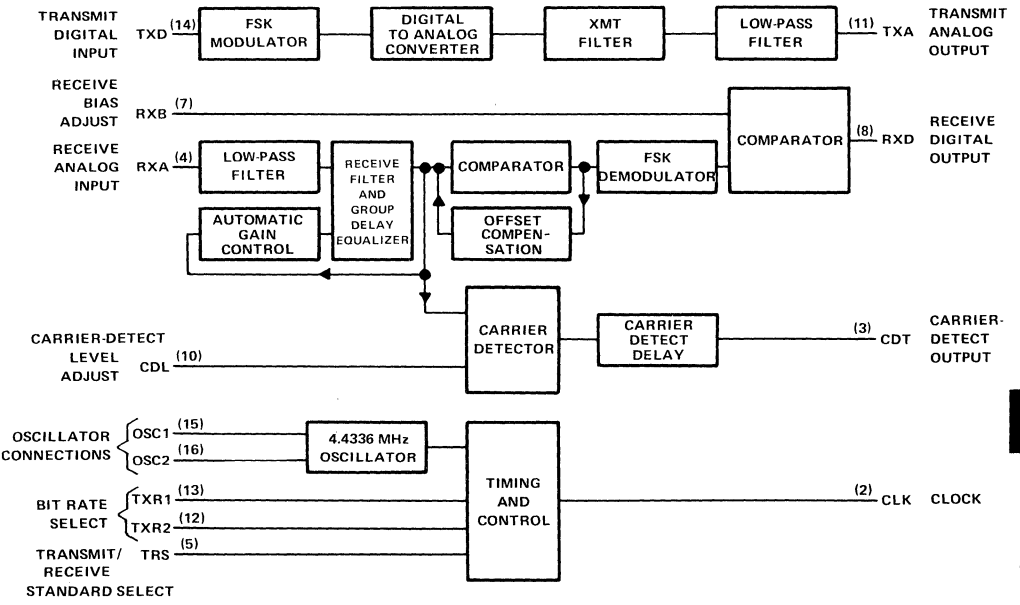
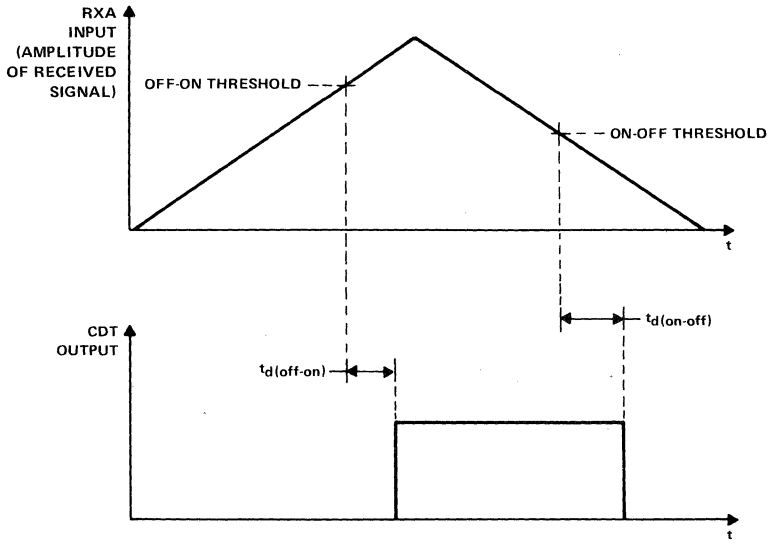
functional block diagram



timing diagram



absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 10 V
Input voltage, V_I (any input) . . . . . −0.3 to V_{DD}
Operating free-air temperature range: TCM3105JE . . . . . −55°C to 85°C
TCM3105JL . . . . . −10°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	TCM3105JE			TCM3105JL			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	5.5	4	5	5.5	V
High-level input voltage, V_{IH}	2		V_{DD}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	0		0.8	V
Analog input level, peak-to-peak (ac coupled)		0.30	0.78		0.30	0.78	V
Clock frequency, f_{clock}	4.4334	4.4336	4.4338	4.4334	4.4336	4.4338	MHz
Analog load impedance at TXA	50			50			kΩ
Operating free-air temperature range, T_A	−40		85	0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TCM3105JE			TCM3105JL			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	RXD, CDT, CLK	I_{OH} = −100 μA	2.4		V_{DD}	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	RXD, CDT, CLK	I_{OL} = 1.6 mA	V_{SS}		0.4	V_{SS}		0.4	V
	Analog output voltage level, peak-to-peak	TXA	V_{DD} = 4 V, R_L = 50 kΩ, C_L = 100 pF		1.55			1.55		V
			V_{DD} = 5 V, R_L = 50 kΩ, C_L = 100 pF	1.4	1.9	2.3	1.4	1.9	2.3	
			V_{DD} = 5.5 V, R_L = 50 kΩ, C_L = 100 pF		2.1			2.1		
	Adjust voltage	RXB	V_{DD} = 5 V	2.3	2.7	3.1	2.3	2.7	3.1	V
		CDL		2.8	3.3	3.9	2.8	3.3	3.9	
	Analog output dc offset	TXA			$V_{DD}/2$			$V_{DD}/2$		V
	Digital input current	TXD, TRS, TXR1, TXR2	V_I = 0 to V_{DD}			±1			±1	μA
	Analog input current	RXA				±15			±15	μA
	Bias input current	RXB, CDL	V_I = 3 V			±150			±150	μA
I_{DD}	Supply current		V_{DD} = 4 V		3	6		3	5	mA
			V_{DD} = 5 V		5	10		5	8	
			V_{DD} = 5.5 V		8	16		8	12	
C_i	Input capacitance, all inputs		f = 1 MHz		10			10		pF
C_o	Output capacitance, all inputs		f = 1 MHz		10			10		pF
	Phase jitter					200			200	μs
	Bias distortion‡					±15%			±15%	
	Carrier detect threshold, off-on§			−45.5		−43	−45.5		−43	dBm
	Carrier detect threshold, on-off§			−48		−45.5	−48		−45.5	dBm
	Carrier detect hysteresis			2.5	2.8		2.5	2.8		dBm

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Bias distortion is the departure from a 50% duty cycle when a series of alternating mark and space tones is received.
§This is the threshold with the CDL input properly adjusted.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TCM3105JE			TCM3105JL			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{d(off\text{-}on)}$	Carrier detect off-to-on delay time	RX = 600 or 1200 b/s	12		25	12		25	ms
		RX = 5, 75, or 150 b/s	48		80	48		80	
$t_{d(on\text{-}off)}$	Carrier detect on-to-off delay time	RX = 600 or 1200 b/s	12		20	12		20	ms
		RX = 5, 75, or 150 b/s	48		75	48		75	
	Transmit frequency deviation from assignment (see Table 1)	f_{clock} = 4.4336 MHz		±1			±1		Hz

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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PRINCIPLES OF OPERATION

The TCM3105 FSK modem is made up of four functional circuits. The circuits are the transmitter, the receiver, a carrier detector, and control and timing (See Figure 1).

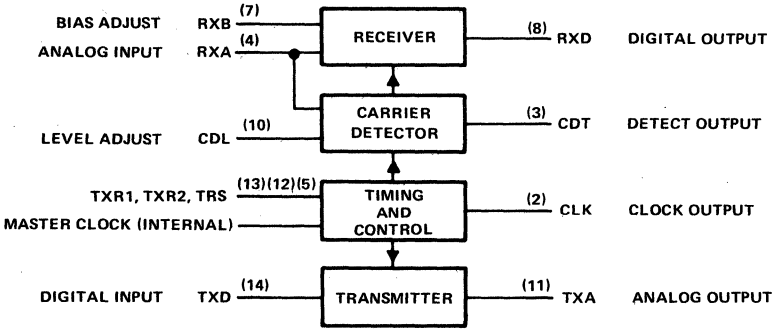

FIGURE 1. TCM3105 SYSTEM PARTITIONING

transmitter

The transmitter comprises a phase coherent FSK modulator, a transmit filter, and a transmit amplifier. The modulator is a programmable frequency synthesizer that drives the output frequencies by variable division of the oscillator frequency (4.4336 MHz). The division ratio is set by the states of the Transmit/Receive Standard input (TRS), the Bit Rate Select inputs (TXR1 and TXR2), and the Digital Data input (TXD).

A switched-capacitor low-pass filter limits the harmonics and noise outside the transmit band and the characteristics of this filter are set by the frequency select inputs as previously described. The harmonics introduced by the transmit filter clock are removed by a continuous low-pass filter.

The transmitter output level varies with power supply voltage and so must be compensated in the 2-wire to 4-wire converter to give a constant output level to the line.

receiver

A continuous low-pass anti-aliasing filter is followed by the receive amplifier, which automatically controls the gain to give a constant output level from the receive filter. The receive filter limits the bandwidth of the signal presented to the demodulator, reducing out-of-band interference, and has very high rejection of the transmit channel frequencies. These are typically present at much higher levels than the received signal.

The group delay equalizer is a switched-capacitor network that compensates the delay introduced by the receive filter and the network. The output from the equalizer is then limited to give an FSK modulated squarewave that is presented to the demodulator.

The demodulator is an edge-triggered multivibrator that triggers off positive and negative going edges. The output of the demodulator is, therefore, a stream of constant-length pulses at a frequency that is double the frequency of the limited input signal. The dc component of this signal is proportional to the received frequency and is extracted by a switched-capacitor, low-pass, post-demodulator filter.

The variation of dc level with received frequency is presented to a comparator that slices at a level externally fixed by the RXB bias adjustment pin. This voltage depends on received bit rate and internal offsets. The comparator output is then the received data at the RXD output.

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carrier detect

The carrier detect circuits comprise an energy detector and digital delay. The energy detector compares the total signal level at the output of the receive filter to an externally set threshold level on the CDL input. The comparator has a 2.5-dB hysteresis and a delay to allow for momentary signal loss and to prevent oscillation. The output of the detector is available on the CDT pin where a high level indicates that a carrier is present.

control and timing

An on-chip oscillator runs from an external 4.4336-MHz crystal connected between the OSC1 and OSC2 pins or an external signal driving OSC1. A clock signal equal to 16 times the highest selected bit rate (transmit or receive) is available on the CLK output.

The single-supply rail means that all analog functions are referenced to an internally generated reference. All analog inputs and output must be ac coupled.

transmit and receive modes

The various modes of operation of the TCM3105 are given in Table 1. The data convention is that a logic high is a mark and a logic low is a space.

TABLE 1. MODES OF OPERATION

STANDARD	TRS	TXR1	TXR2	TRANSMITTED BAUD RATE	RECEIVED BAUD RATE	TRANSMIT FREQUENCY ASSIGNMENTS (Hz)	RECEIVE FREQUENCY ASSIGNMENTS (Hz)	CLK FREQUENCY (kHz)
CCITT V.23	L	L	L	1200	1200	M 1300 S 2100	M 1300 S 2100	19.11
	H	L	L	1200	75	M 1300 S 2100	M 390 S 450	19.11
	L	L	H	600	75	M 1300 S 1700	M 390 S 450	9.56
	H	L	H	600	600	M 1300 S 1700	M 1300 S 1700	9.56
	L	H	L	75	1200	M 390 S 450	M 1300 S 2100	19.11
	H	H	L	75	600	M 390 S 450	M 1300 S 1700	9.56
	L	H	H	75	75	M 390 S 450	M 390 S 450	1.19
BELL 202	$\overline{CLK}$	L	L	1200	1200	M 1200 S 2200	M 1200 S 2200	19.11
	$\overline{CLK}$/8	L	H	1200	150	M 1200 S 2200	M 387 S 487	19.11
	$\overline{CLK}$/8	L	H	1200	5	M 1200 S 2200	M 387 S 0	19.11
	CLK	H	L	150	1200	M 387 S 487	M 1200 S 2200	19.11
	CLK	H	H	150	150	M 367 S 487	M 387 S 487	2.39
	CLK†	H†	L†	5	1200	M 387 S 0	M 1200 S 2200	19.11
	H†	H†	H†					
	H	H	H	Transmit Disabled	1200	Transmit Disabled	M 1200 S 2200	19.11

H = high level, L = low level
†In these modes, the modulation is controlled by the TRS and TXR2 pins. TXD is tied high.

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APPLICATION INFORMATION

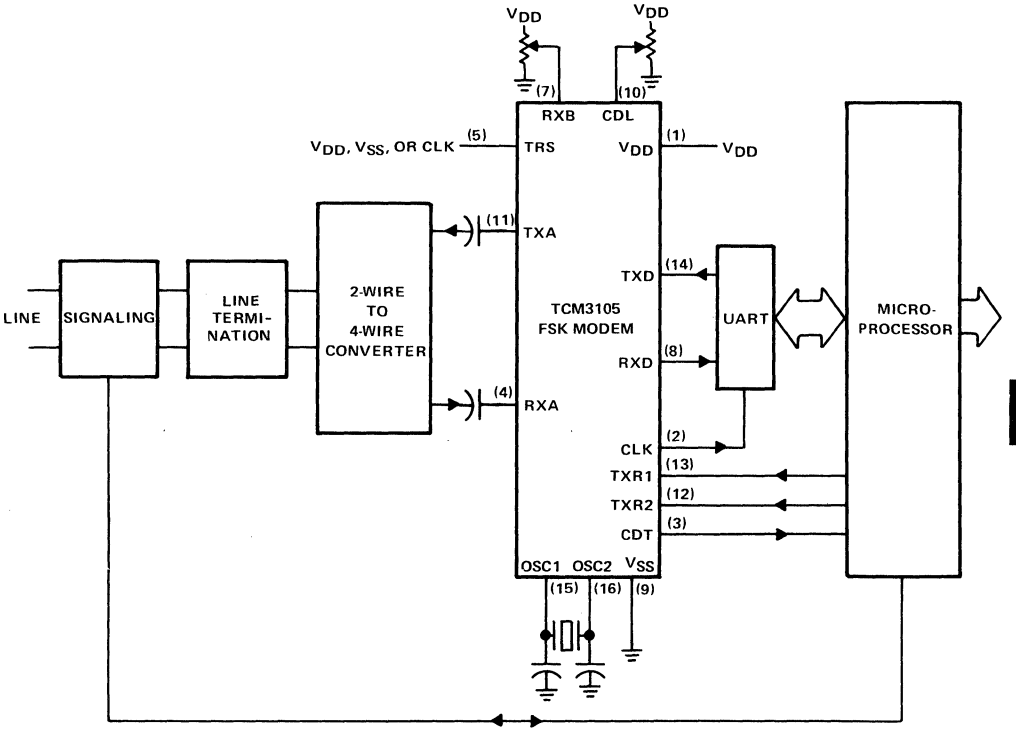

FIGURE 2. TYPICAL SYSTEM CONFIGURATION

APPLICATION INFORMATION

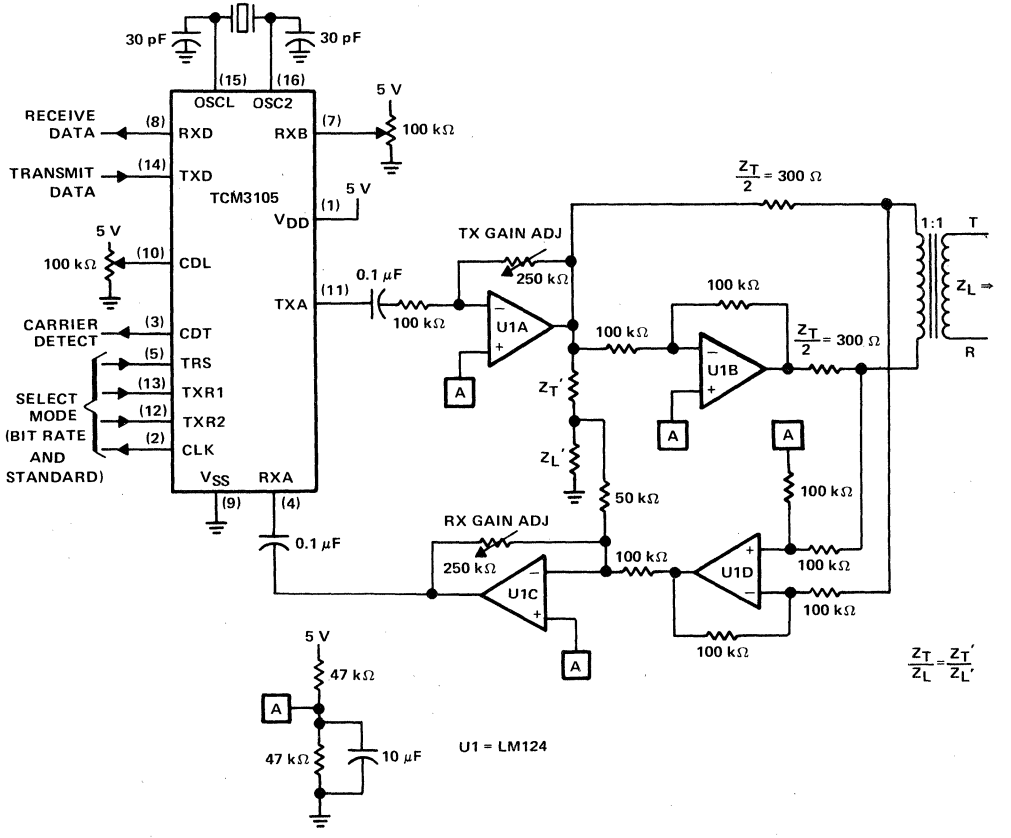

FIGURE 3. TELEPHONE LINE INTERFACE CIRCUIT

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APPLICATION INFORMATION

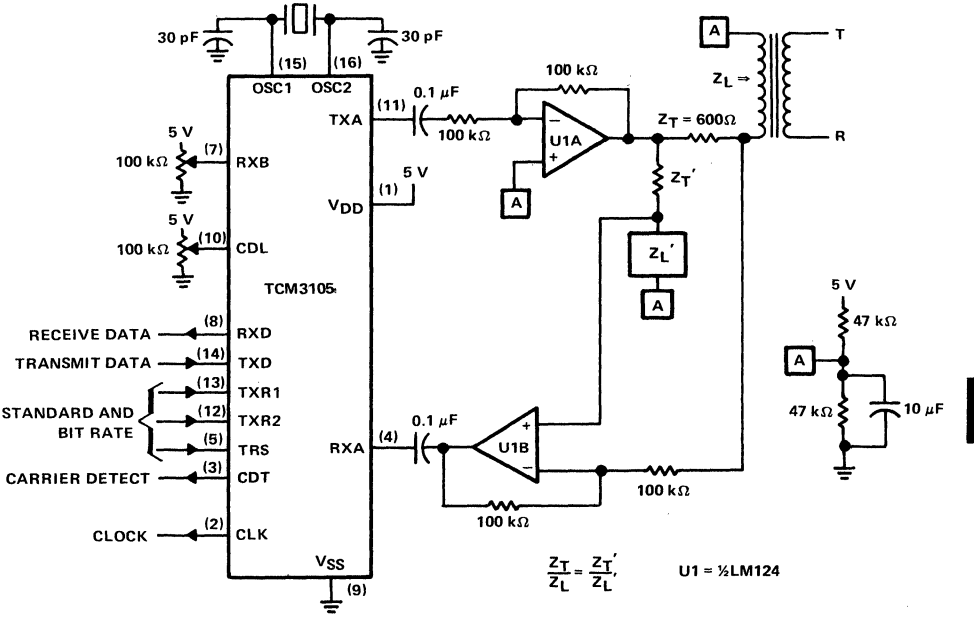


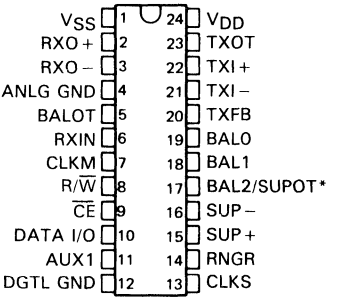
FIGURE 4. SIMPLIFIED TELEPHONE LINE INTERFACE CIRCUIT

TCM4204A, TCM4205A, TCM4207A SUBSCRIBER-LINE-CONTROL CIRCUITS

D2729, NOVEMBER 1983—REVISED APRIL 1986

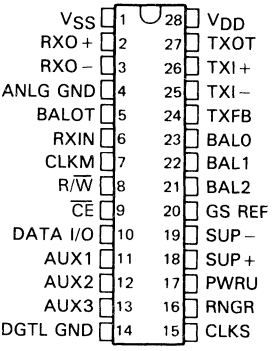
- **Per-Channel-Programmable Single-Chip Subscriber-Line-Control Circuit (SLCC)**
- **Programmable TX and RX Gain**
- **Digital Inputs and Outputs are Compatible with TTL Levels**
- **±5 V Power Supplies**
- **Software-Selectable External Balance Networks**
- **On-Off Hook Detection, Ring Trip**
- **TCM4205A Provides Control of the Three Auxiliary Relays and Ground Start Supervision**
- **Serial Interface to Microprocessor**
- **High-Reliability Silicon-Gate CMOS Technology**
- **TCM4207A Uses a Flux Canceling Technique that Allows Use of a Smaller Transformer**

TCM4204A, TCM4207A . . . J PACKAGE
(TOP VIEW)



*BAL2 for TCM4204A, SUPOT for TCM4207A

TCM4205A . . . J PACKAGE
(TOP VIEW)



description

The TCM4204A, TCM4205A, and TCM4207A are subscriber-line-control circuits (SLCC) designed to provide all the functions of a complete voice-band PCM channel when used in conjunction with appropriate codec and filter circuits. The TCM4205A enhancement of the TCM4204A brings out two additional relay control pins (AUX2) and (AUX3), an external reference for ground-start applications (GS REF), and a pin for control of an external power supply (PWRU). The TCM4207A replaces BAL2 with a filtered analog output (SUPOT) that can be used in flux canceling applications.

The primary applications for these devices include:

Transmission Systems and Switching Systems
2-Wire Interface 4-Wire Interface
Subscriber Line Concentrators

These devices are characterized for operation from 0°C to 70°C.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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analog section

Separate Programmable Attenuators: 63 steps covering a 12.6-dB range in 0.2-dB steps
6-dB Differential RX amplification for driving a 900-ohm load to a peak of 3.2 V
Software-selectable external balance networks. Electronic 2-wire to 4-wire conversion.
Software-controlled analog loopback
Separate RX and TX paths allow true 4-wire operation.

supervision

Normal loop-start and/or ground-start supervision
Ring trip supervision
Supervision function provided with minimal, low cost external components.

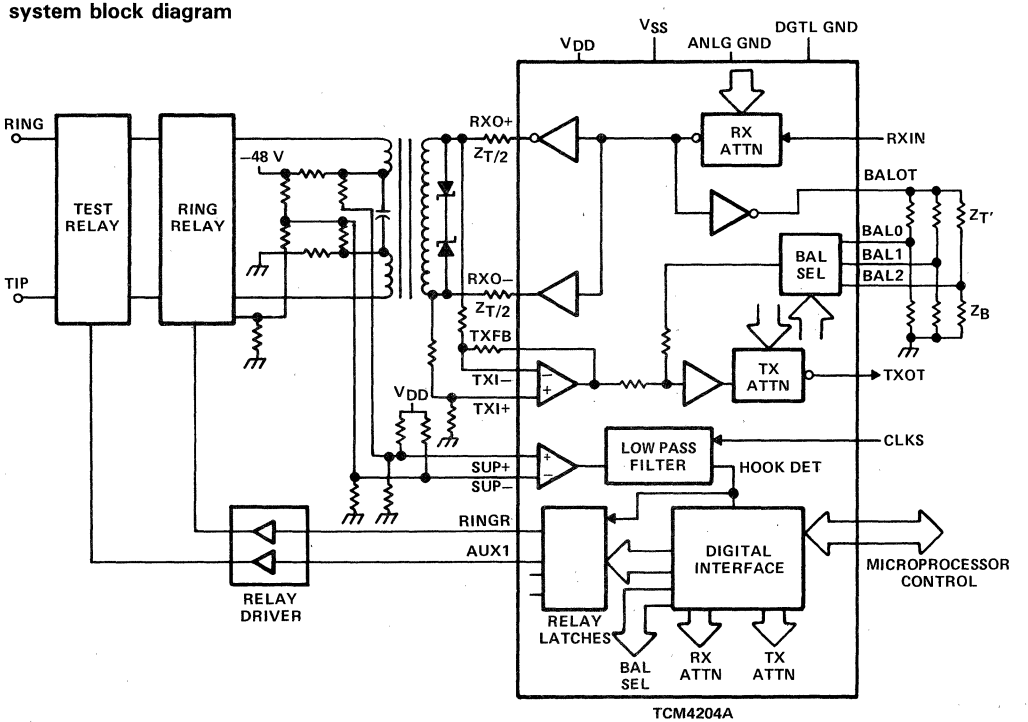
digital interface

Simple four-pin serial interface provides easy-to-use microprocessor interface.
Clocks can be any of the standard PCM clock frequencies.
Power fault detection lets user know when RAM has been affected by a supply fault.

software control

Up to three external balance networks
Transmit and receive attenuators
Power down, standby, voice, or loopback modes of operation
Ring relay and up to three auxiliary relays.

system block diagram



TCM4204A

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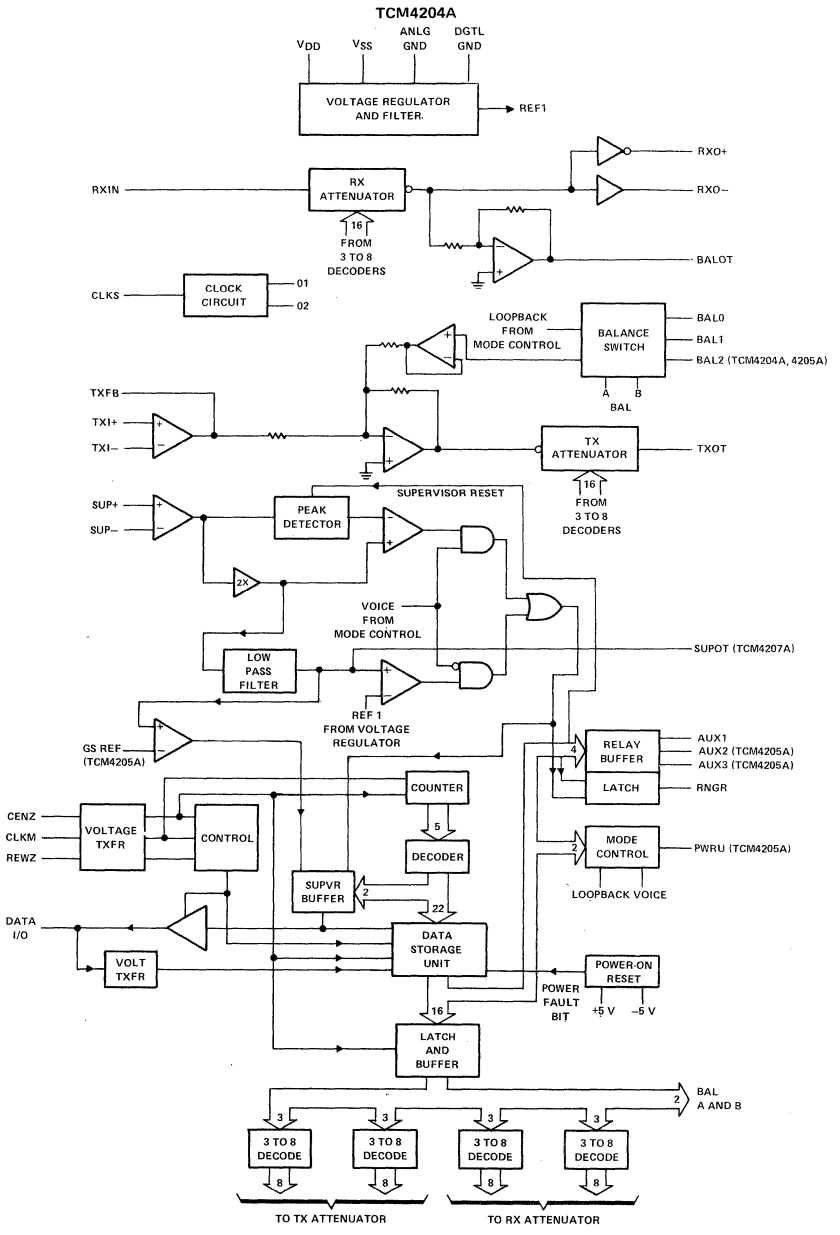
functional block diagram (positive logic)



NAME	PIN			DESCRIPTION
	TCM4204A	TCM4205A	TCM4207A	
ANLG GND	4	4	4	Analog ground
AUX1	11	11	11	Latched digital outputs for relay control
AUX2		12		
AUX3		13		
BAL0	19	23	19	Analog input to balance network selection
BAL1	18	22	18	
BAL2	17	21		
BALOT	5	5	5	A buffered form of the RX signal for application to the external balance network
$\overline{CE}$	9	9	9	Chip enable. Activated by a logic low input.
CLKM	7	7	7	Digital clock input that advances the pointer counter of the digital storage unit (DSU) allowing the information in the DSU to be accessed. When R/$\overline{W}$ and $\overline{CE}$ are low, information on the DATA I/O pin is latched into the DSU by the falling edge of CLKM.
CLKS	13	15	13	A continuous clock input (from 1.536 to 2.048 MHz) used for internal logic. This signal is not synchronous with any other signal.
DATA I/O	10	10	10	Digital data input/output. When $\overline{CE}$ is low and R/$\overline{W}$ is high, the DATA I/O pin is in the output mode. When $\overline{CE}$ is low and R/$\overline{W}$ is low, the DATA I/O pin is in the input mode. When $\overline{CE}$ is high, the DATA I/O pin is in the high-impedance state.
DGTL GND	12	14	12	Digital ground
GS REF		20		Analog reference voltage input used for ground start supervision.
PWRU		17		Decoded digital output of Mode Control used to control an external power supply.
RNGR	14	16	14	Latched digital output to control the ring relay. The output turns off (low) when off-hook is detected, but the controller must program the ring bit low to ensure that the output remains low.
RXIN	6	6	6	Analog input to the receive section
RXO+	2	2	2	Complementary analog output of the receive amplifier
RXO−	3	3	3	
R/$\overline{W}$	8	8	8	Digital input control for the direction of response of the digital storage unit. A logic high on R/$\overline{W}$ sets the DSU to transmit information. A logic low on R/$\overline{W}$ enables the DSU to receive information.
SUP+	15	18	15	Differential analog supervision inputs. Inputs to SUP+ and SUP− are used to detect off-hook status during normal and ringing supervision.
SUP−	16	19	16	
SUPOT			17	Filtered supervisory analog output
TXFB	20	24	20	Feedback out of TX input amplifier
TXI+	21	25	21	Analog differential inputs to TX input amplifier
TXI−	22	26	22	
TXOT	23	27	23	Analog output of TX output amplifier
V_{DD}	24	28	24	Supply voltage (5 V ±5%)
V_{SS}	1	1	1	Supply voltage (−5 V ±5%) referenced to ANLG GND

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} . . . . . 6 V
Supply voltage, V_{SS} . . . . . −6 V
Input/output voltage: digital . . . . . V_{DD} + 0.3 V to GND − 0.3 V
analog . . . . . V_{DD} + 0.3 V to V_{SS} − 0.3 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 125°C

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)		4.75	5.25	V
Supply voltage, V_{SS} (see Note 2)		−4.75	−5.25	V
High-level input voltage, V_{IH}		2.4		V
Low-level input voltage, V_{IL}			0.8	V
DC voltage at either supervision input (SUP+ or SUP−)			±2.5	V
SUPOT voltage			±3	V
DC offset voltage at analog input to RX section (RXIN)			±25	mV
DC offset voltage at transmit inputs (TXI+ and TXI−)			±25	mV
Load capacitance, C_L	BALOT, TXOT, SUPOT, TXFB		25	nF
	RXO+, RXO−		100	
Load resistance, R_L	BALOT, TXOT, SUPOT, TXFB	5	100	kΩ
	RXO+, RXO−	300		Ω
Rise time (any logic input), t_r			100	ns
Fall time (any logic input), t_f			100	ns
Clock frequency f_{CLKS}		1.536	2.048	MHz
Operating free-air temperature, T_A		0	70	°C

NOTES: 1. Reference is to DGTL GND and ANLG GND.
2. Reference is to ANLG GND.

static electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V, V_{SS} = −5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −0.4 mA	4.6			V
V_{OL}	Low-level output voltage		I_{OL} = 1.6 mA			0.4	V
	Differential voltage between V_{DD} and V_{SS} required to initiate POR (power-on-reset)		dV_{DD}/dt > 1 V/ms	6		8	V
	Differential voltage between SUP+ and SUP− required to initiate off-hook condition		Voice mode, SUP− at DGTL GND, DSU bit 23 high	−20	0	25	mV
			Standby and power-down mode, SUP− at DGTL GND	25	50	75	mV
I_I	Input current, analog	SUP+, SUP−	V_I = 3 V			1	μA
			V_I = −3 V			−1	μA
		RXIN, TXI+, TXI−, BAL0, BAL1, BAL2	V_I = 5 V			1	μA
			V_I = −5 V			−1	μA
I_{IH}	High-level input current		V_I = 5 V			1	μA
I_{IL}	Low-level input current		V_I = 0			−1	μA
I_{OH}	High-level output current	digital	V_{OH} = 2.5	−1.6			mA
		data	V_{OH} = 0 (continuous)	−10			mA
I_{OL}	Low-level output current	digital	V_{OL} = 2.5 V	1.6			mA
		data	V_{OL} = 5 V (continuous)	55			mA
	Analog output offset voltage	TXOT	Loopback mode, TXI+/TXI− at ANLG GND			±50	mV
		TXFB	TXI+ at ANLG GND, TXI− tied to TXFB, Loopback mode			±25	mV
		RXO+	Voice mode, RXIN at ANLG GND			±75	mV
		RXO−	Voice mode, RXIN at ANLG GND			±75	mV
		SUPOT	SUP+ and SUP− at ANLG GND		220		mV
	Receive output dc leakage current (See Note 3)		Standby or power-down mode, RXO+ connected to RXO− through a 600 Ω resistor			±20	μA
I_{DD}	Supply current		On hook, power-down mode			3	mA
			On hook, voice mode			9	mA
			Off hook, power-down mode			6	mA
			Off hook, voice mode			13	mA
I_{SS}	Supply current		On hook, power-down mode			−3	mA
			On hook, voice mode			−9	mA
			Off hook, power-down mode			−6	mA
			Off hook, voice mode			−13	mA

†All typical values are at V_{DD} = 5 V, V_{SS} = −5 V, T_A = 25°C.

NOTE 3: If used with a center-tapped transformer (with center tap connected to GND), the output leakage current will increase.

dynamic characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Receive output dynamic range (RXO+, RXO−)		Input to RXIN = −75 dBm to 3 dBm, R_L = 900 Ω to ANLG GND, Receive channel attenuator set to code 100111 (0 dB), f = 1.02 kHz	−74 to 3	−75 to 3.1		dBm
	Receive output dynamic range (BALOT)		Input to RXIN = −75 dBm to 3 dBm, R_L = 5 kΩ to ANLG GND, Receive channel attenuator set to code 100111 (0 dB), f = 1.02 kHz	−74 to 3	−75 to 3.1		dBm
	Transmit output dynamic range (TXOT)		Loopback mode, Input = −75 dBm to 3 dBm. R_L = 5 kΩ to ANLG GND, Transmit channel attenuator set to code 111111 (0 dB), f = 1.02 kHz	−74 to 3	−75 to 3.1		dBm
	Transmit output dynamic range (TXFB)		Input = −75 dBm to 3 dBm, R_L = 5 kΩ to ANLG GND, Transmit input amplifier set for unity gain, Transmit attenuator set to 0 dB, f = 1.02 kHz	−74 to 3	−75 to 3.1		dBm
	Supervision output dynamic range (SUPOT)		Input to SUP+ = 75 mV to 750 mV (rms), SUP− at ANLG GND, R_L = 100 kΩ to ANLG GND, f = 5 Hz	−14 to 6	−13.8 to 6.2		dBm
	Frequency response of supervision circuits	0 to 10 Hz	SUP− at ANLG GND, Input to SUP+ = −10 dBmO‡, f_{clock} = 2.048 MHz			8	dB
		16.6 Hz				−45	
		15 Hz to 65				−30	
		66 Hz or greater				−40	
C_i	Input capacitance	Data	$\overline{CE}$ high			14	pF
		All others				7.5	
$t_{d(POR)}$	Delay time to power-on reset		V_{DD} − V_{SS} switched from 10 V to 6 V	100		200	ns
Z_i	Input impedance, (any input or I/O)			1			MΩ
Z_o	Output impedance	Digital outputs	I_O = −200 μA			100	Ω
		TXOT, BALOT, TXFB				50	
		SUPOT				1	kΩ
		RXO+, RXO−	Voice mode, I_O = −10 μA		1	3	Ω

†All typical values are at V_{DD} = 5 V, V_{SS} = −5 V, T_A = 25°C.
‡0 dBmO is the zero-reference point of the channel under test. This corresponds to a voltage of 1520 mV (rms) on inputs and outputs, with attenuators set for 0 dB.

ac characteristics — half channel† over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
Frequency response	50 Hz to 200 Hz	R_L = 900 Ω to ANLG GND, V_I = 0 dBm0, Ref = 1.020 kHz	−0.2	0.2	dB
	200 Hz to 300 Hz		−0.1	0.1	
	300 Hz to 4 kHz		−0.05	0.05	
Level (gain) tracking	V_i = 0, −10, −20, −30 dBm0	R_L = 900 Ω to ANLG GND, f = 1.020 kHz	−0.05	0.05	dB
	V_i = −40, −50 dBm0		−0.1	0.1	
Idle channel noise		R_L = 900 Ω to ANLG GND		8	dBrnc0
Total distortion	V_i = 0 dBm0 to −30 dBm0	R_L = 900 Ω to ANLG GND, f = 1.020 kHz		−50	dB
	V_i = −30 dBm0 to −40 dBm0			−45	
	V_i = −40 dBm0 to −50 dBm0			−40	
Total harmonic distortion	V_i = 3 dBm0, f = 1.020 kHz			−55	dB
Phase Delay time (carrier)	1 kHz			20	μs
	1.8 kHz			20	
Absolute delay time	500 Hz to 600 Hz			30	μs
	600 Hz to 1 kHz			20	
	1 kHz to 2.6 kHz			10	
	2.6 kHz to 2.8 kHz			30	
Departure from linear phase	600 Hz to 1 kHz			±0.1	rad
	1 kHz to 1.3 kHz			±0.05	
	1.3 kHz to 2.3 kHz			±0.05	
	2.3 kHz to 2.7 kHz			+0.04 −0.05	
	2.7 kHz to 3.1 kHz			±0.1	
Supply-voltage sensitivity (see Note 4)	50 Hz to 4 kHz	V_{DD} changing 200 mV p-p		−40	dB
		V_{SS} changing 200 mV p-p		−40	
	4 kHz to 50 kHz	V_{DD} changing 200 mV p-p		−25	
		V_{SS} changing 200 mV p-p		−25	

†Transmit channel is tested with input amplifier set for unity gain. Receive and transmit attenuators are set to 0 dB.

NOTE 4: The receiver supply-voltage sensitivity is the differential RXO+-to-RXO− noise referenced to supply noise. It is assumed that the feed transformer will reject common-mode RXO+/RXO− noise and, therefore, the common-mode supply-voltage sensitivity is not specified.

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system characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 9 and 10)

PARAMETER	FREQUENCY RANGE	TEST CONDITIONS	MIN	MAX	UNIT
Return loss (see Note 5)	200 Hz to 500 Hz	Z_L = 900 Ω + 2.2 μF		−25	dB
	500 Hz to 1 kHz			−35	
	1 kHz to 2.5 kHz			−40	
	2.5 kHz to 3.4 kHz			−35	
Transhybrid loss (see Note 5)	200 Hz to 500 Hz	Z_L = 900 Ω + 2.2 μF		−25	dB
	500 Hz to 1 kHz			−35	
	1 kHz to 2.5 kHz			−40	
	2.5 kHz to 3.4 kH			−35	
Longitudinal balance (see Note 5)	60 Hz to 500 Hz	2-wire to 4-wire		−66	dB
	500 Hz to 1 kHz			−50	
	1 kHz to 4 kHz			−58	
	200 Hz to 4 kHz	4-wire to 2-wire		−60	

NOTE 5: The return loss, the transhybrid loss, and the longitudinal balance are functions of external components, primarily the battery feed transformer or its functional replacement. The SLCC will not materially change the return loss or the longitudinal balance. The imbalance in transhybrid loss caused by phase or gain errors in the SLCC will be less than those listed.

SLCC — microprocessor timing requirements over recommended ranges of supply voltage and operating free-air temperature

	PARAMETER	MIN	MAX	UNIT
t_a	Access time from $\overline{CE}$↓		140	ns
$t_{c(CLK)}$	Clock period for CLKM	2000		ns
t_r, t_f	Rise and fall times for CLKM	5		ns
t_v	Output data valid after CLKM	80		ns
$t_{w(CLKH)}$	Pulse duration CLKM high	550		ns
$t_{w(CLKL)}$	Pulse duration CLKM low	300		ns
$t_{en(CLK)}$	Internal read/write enable after CLKM		250	ns
$t_{en(R/\overline{W})}$	Enable time, Input after R/$\overline{W}$↓	0	250	ns
$t_{dis(\overline{CE})}$	Disable time, output after $\overline{CE}$↑		180	ns
t_{su1}	Setup time, CLKM↓ before R/$\overline{W}$↑	50		ns
t_{su2}	Setup time, data before CLKM↓ (see Note 6)	180		ns
t_{su3}	Setup time, CE↓ before CLKM↑ (see Notes 7 and 8)	180		ns
	Duty cycle, CLKM (see Note 9)	10	90	%

NOTES: 6. The R/$\overline{W}$ input must be a logic low.
7. If the user is not interested in reading bit 0, t_{su3} can be a minimum of 30 ns.
8. The R/$\overline{W}$ input must be a logic high.
9. As long as the minimum high and low pulse durations are observed, the CLKM duty cycle is $t_{w(CLKH)}/[t_{w(CLKL)} + t_w\ (CLKH)]$.

supervision timing characteristics over recommended ranges of operating conditions (see Figure 4)

normal loop supervision timing characteristics, f_{CLKS} = 2.048 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation time high-to-low, hook status bit	Standby mode, SUP− = GND,		75	100	ms
t_{PLH}	Propagation time low-to-high, hook status bit	SUP+ changing from		60	100	ms
$t_{PHL} - t_{PLH}$	Differential propagation time	0 V to 200 mV or from			±20	ms
t_{nr}	Maximum noise rejection duration time	200 mV to 0 V	10			ms

ground key/ground start supervision timing characteristics (TCM4205A only)

PARAMETER		MIN	MAX	UNIT
t_{PHL}	Propagation time high-to-low, ground start bit		150	ms
t_{PLH}	Propagation time low-to-high, ground start bit		150	ms
$t_{PHL} - t_{PLH}$	Differential propagation time		±20	ms
t_{nr}	Maximum noise rejection duration time	10		ms

ring trip detection timing characteristic

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{rt}	Ring trip detect time	Standby mode, SUP− = GND, SUP+ changing from 0 V to 200 mV		55	100	ms

microprocessor internal polling timing requirement

PARAMETER	MIN	MAX	UNIT
Microprocessor polling interval		100	ms

†All typical values are at V_{DD} = 5 V, V_{SS} = −5 V, T_A = 25°C.

PRINCIPLES OF OPERATION

mode control

The SLCC can be forced into one of four modes by the microprocessor (see Figure 1 for mode states and Table 1 for the recommended mode control sequence). The mode control functions are as follows:

Voice operation — All circuits powered up. PWRU output pin is set high.

Power down — Audio circuits are powered down, supervisory circuits are powered up, and the PWRU output pin is set low.

Loopback — Normal balance circuit is interrupted allowing the transmit output to follow the receive input. All other circuits are powered up.

Standby — Audio circuits are powered down, supervisory circuits are powered up, and the PWRU output pin is set high. The internal power-on reset (POR) circuit sets the SLCC to this mode at power up.

TABLE 1. RECOMMENDED MODE CONTROL SEQUENCE

BITS A	BITS B	FUNCTION
L	H	Power Down
L	L	Standby
H	L	Voice
H	H	Loopback

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PRINCIPLES OF OPERATION

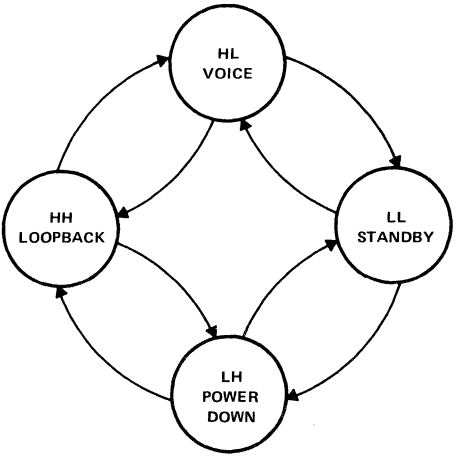

FIGURE 1. MODE CONTROL STATE DIAGRAM

internal power-down states

The internal power down states are the standby mode and the power-down mode. The only difference between the two states is the level of the PWRU output. In the standby mode, PWRU is set high and in the power-down mode, PWRU is set low. The PWRU output can be used to control an external dc-to-dc converter for floating constant-current-feed applications or to drive a status indicator.

standby mode

1. All analog functions except supervision and all logic functions except microprocessor interface and registers are powered down.
2. PWRU output is set high.

power-down mode

1. All analog functions except supervision and all logic functions except microprocessor interface and registers are powered down.
2. PWRU output is set low.

PRINCIPLES OF OPERATION

digital control and microprocessor interface

The data storage unit contains 24 bits of R/$\overline{W}$ (Read/Write) and RO (Read Only) data. The R/$\overline{W}$ data is used to control attenuation, balance, relay selection, and mode of operation. The RO data provides supervisory status information.

The microprocessor uses the DATA I/O, R/$\overline{W}$, $\overline{CE}$, and CLKM input lines to control and time access to the data. When $\overline{CE}$ is toggled from high to low, the serial data sequence is started at bit 0 and the pointer is sequenced through the 24 data bits. The pointer is advanced by the CLKM input. In addition, $\overline{CE}$ enables the read and write functions. When $\overline{CE}$ is high, the DATA I/O pin is in a high impedance state, and the CLKM and R/$\overline{W}$ inputs are ignored.

balance network

The SLCC allows up to three external balance networks to be selected by the microprocessor. The balance networks are scaled versions of Z_T and Z_L. The scale factor is user dependent. To properly balance the two- to four-wire converter, the ratio Z_T'/Z_B must equal Z_T/Z_L where Z_L is the line impedance and Z_T, Z_T', and Z_B are as labeled in the Typical Application Data. The impedance of the Z_T' and Z_B must be greater than 5 kΩ for all three balance networks in parallel.

TABLE 2. BALANCE NETWORK SELECTION

BAL A	SELECT B	TCM4204A or TCM4205A	TCM4207A
L	L	BAL0	BAL0
L	H	BAL1	BAL1
H	L	BAL2	disallowed
H	H	disallowed	disallowed

power on reset

When the SLCC is powered up, it is forced into a known state (see Table 3). The pointer counter is set to zero. After a power-on-reset has occurred, the following conditions exist:

1. The pointer counter addresses bit 0 (on/off hook).
2. The power fault bit goes high to let the user know that a power-on-reset has occurred. For example, a large V_{DD} or V_{SS} glitch will cause a power-on-reset. The power-fault bit flags this condition. The power-fault bit must be reset by the user.
3. All relays are tuned off (control bits are low).
4. The standby mode-control condition is set.
5. All attenuator bits are set to zero causing maximum attenuation of the receiver and transmitter amplifiers.
6. Balance select conditions are set to the 0,0 condition.

supervisor reset

Supervisor reset (bit 23) resets the peak detector reference voltage in the SLCC supervisor circuit. The peak detector circuit is used during dial pulse collection and on-hook detection when the SLCC is in the voice mode. The reference voltage is also reset by the ring relay control (bit 3). When off-hook is detected and the ring relay is off, the supervisor reset (bit 23) should be set high and then returned to low prior to setting the SLCC to the voice mode.

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PRINCIPLES OF OPERATION

TABLE 3. REGISTER MAP

BIT NUMBER	FUNCTION	DATA TYPE	POWER ON RESET
0	On/Off Hook	RO	X
1	Ground Start	RO	X
2	Power Fault	R/$\overline{W}$	H
3	Ring Relay	R/$\overline{W}$	L
4	AUX1 Relay	R/$\overline{W}$	L
5	AUX2 Relay	R/$\overline{W}$	L
6	AUX3 Relay	R/$\overline{W}$	L
7	Mode Control A	R/$\overline{W}$	L
8	Mode Control B	R/$\overline{W}$	L
9	Rx Atten Bit 5 (MSB)	R/$\overline{W}$	L
10	Rx Atten Bit 4	R/$\overline{W}$	L
11	Rx Atten Bit 3	R/$\overline{W}$	L
12	Rx Atten Bit 2	R/$\overline{W}$	L
13	Rx Atten Bit 1	R/$\overline{W}$	L
14	Rx Atten Bit 0 (LSB)	R/$\overline{W}$	L
15	Tx Atten Bit 5 (MSB)	R/$\overline{W}$	L
16	Tx Atten Bit 4	R/$\overline{W}$	L
17	Tx Atten Bit 3	R/$\overline{W}$	L
18	Tx Atten Bit 2	R/$\overline{W}$	L
19	Tx Atten Bit 1	R/$\overline{W}$	L
20	Tx Atten Bit 0 (LSB)	R/$\overline{W}$	L
21	Balance Select A	R/$\overline{W}$	L
22	Balance Select B	R/$\overline{W}$	L
23	Supervisor Reset	R/$\overline{W}$	L

attenuator characteristics

Both attenuators have identical characteristics but are separately controlled. The characteristics of the attenuators are as follows:

1. 63 steps (reference Table 4)
2. Receiver range of 4.8 dB gain to −7.8 dB loss (differential)
3. Transmitter range of 0 dB to −12.6 dB loss
4. Step size of 0.2 dB
5. The accuracy of any attenuator setting is ±1 step size.

lead options

The TCM4204A (24-pin constant-voltage option) is designed to provide the minimum set of features required by the largest proportion of world-wide needs. The TCM4204A has the following:

1. Three separate external balance networks
2. Two relay outputs (TTL); one output dedicated to ring and one auxiliary output.

The TCM4205A (28-pin ground-start option) has the following:

1. Three separate external balance networks
2. Four relay outputs (TTL); one dedicated to ring and three auxiliary outputs
3. An input to set the ground-start trip level.

The TCM4207A (24-pin flux-canceling option) has the following:

1. Two separate external balance networks
2. Two relay outputs (TTL); one output dedicated to ring and one auxiliary output
3. One filtered analog output (16.6 Hz at CLKS = 2.048 MHz) that is an analog representation of the dc voltage (< 10 Hz) between the supervisory inputs.

TABLE 4. ATTENUATOR CODES

ATTENUATOR CODE		TRANSMIT†	RECEIVE
DECIMAL	BINARY	CHANNEL	CHANNEL‡
0	000000	−12.6 dB	−7.8 dB
1	000001	−12.4 dB	−7.6 dB
2	000010	−12.2 dB	−7.4 dB
3	000011	−12.0 dB	−7.2 dB
4	000100	−11.8 dB	−7.0 dB
5	000101	−11.6 dB	−6.8 dB
6	000110	−11.4 dB	−6.6 dB
7	000111	−11.2 dB	−6.4 dB
8	001000	−11.0 dB	−6.2 dB
9	001001	−10.8 dB	−6.0 dB
10	001010	−10.6 dB	−5.8 dB
11	001011	−10.4 dB	−5.6 dB
12	001100	−10.2 dB	−5.4 dB
13	001101	−10.0 dB	−5.2 dB
14	001110	−9.8 dB	−5.0 dB
15	001111	−9.6 dB	−4.8 dB
16	010000	−9.4 dB	−4.6 dB
17	010001	−9.2 dB	−4.4 dB
18	010010	−9.0 dB	−4.2 dB
19	010011	−8.8 dB	−4.0 dB
20	010100	−8.6 dB	−3.8 dB
21	010101	−8.4 dB	−3.6 dB
22	010110	−8.2 dB	−3.4 dB
23	010111	−8.0 dB	−3.2 dB
24	011000	−7.8 dB	−3.0 dB
25	011001	−7.6 dB	−2.8 dB
26	011010	−7.4 dB	−2.6 dB
27	011011	−7.2 dB	−2.4 dB
28	011100	−7.0 dB	−2.2 dB
29	011101	−6.8 dB	−2.0 dB
30	011110	−6.6 dB	−1.8 dB
31	011111	−6.4 dB	−1.6 dB
32	100000	−6.2 dB	−1.4 dB
33	100001	−6.0 dB	−1.2 dB
34	100010	−5.8 dB	−1.0 dB
35	100011	−5.6 dB	−0.8 dB
36	100100	−5.4 dB	−0.6 dB
37	100101	−5.2 dB	−0.4 dB
38	100110	−5.0 dB	−0.2 dB
39	100111	−4.8 dB	0.0 dB
40	101000	−4.6 dB	+0.2 dB
41	101001	−4.4 dB	+0.4 dB
42	101010	−4.2 dB	+0.6 dB
43	101011	−4.0 dB	+0.8 dB
44	101100	−3.8 dB	+1.0 dB
45	101101	−3.6 dB	+1.2 dB
46	101110	−3.4 dB	+1.4 dB
47	101111	−3.2 dB	+1.6 dB
48	110000	−3.0 dB	+1.8 dB
49	110001	−2.8 dB	+2.0 dB
50	110010	−2.6 dB	+2.2 dB
51	110011	−2.4 dB	+2.4 dB
52	110100	−2.2 dB	+2.6 dB
53	110101	−2.0 dB	+2.8 dB
54	110110	−1.8 dB	+3.0 dB
55	110111	−1.6 dB	+3.2 dB
56	111000	−1.4 dB	+3.4 dB
57	111001	−1.2 dB	+3.6 dB
58	111010	−1.0 dB	+3.8 dB
59	111011	−0.8 dB	+4.0 dB
60	111100	−0.6 dB	+4.2 dB
61	111101	−0.4 dB	+4.4 dB
62	111110	−0.2 dB	+4.6 dB
63	111111	0.0 dB	+4.8 dB

†Transmit input amplifier set for unity gain.

‡Output measured differentially across RXO+ and RXO−.

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PARAMETER MEASUREMENT INFORMATION

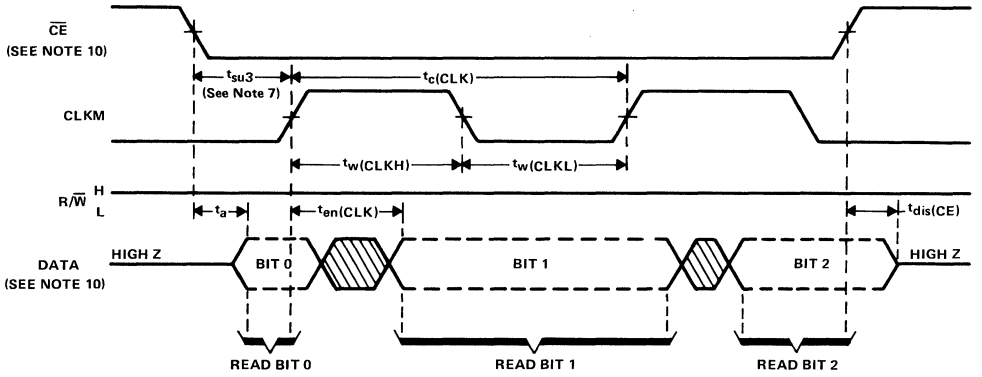


FIGURE 2. SLCC — MICROPROCESSOR TIMING REQUIREMENTS FOR READ OPERATION

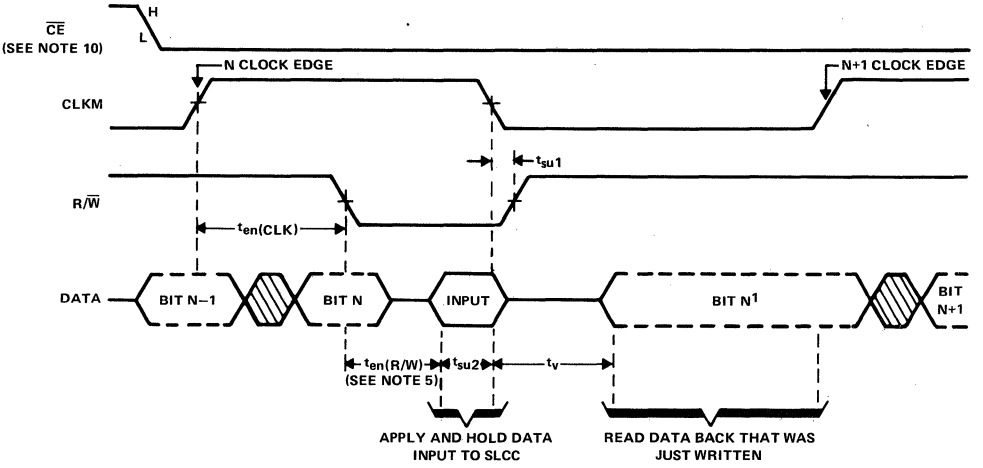


FIGURE 3. SLCC — MICROPROCESSOR TIMING REQUIREMENTS FOR WRITE OPERATION

NOTES: 7. If the user is not interested in reading bit 0, t_{su3} can be a minimum of 30 ns.

10. The DATA pin is an input, an output, or in a high-impedance state. When $\overline{CE}$ is low, the DATA pin will be either an input or an output depending upon the condition of R/$\overline{W}$. When R/$\overline{W}$ is high and $\overline{CE}$ is low, the DATA pin is an output that a microprocessor can poll. When R/$\overline{W}$ is low and $\overline{CE}$ is low, the DATA pin is an input. Dashed lines on the DATA signal indicate that the data on the DATA pin is coming from the SLCC. Solid lines on the DATA signal indicate that the data on the DATA pin is coming from the system. Each time the $\overline{CE}$ input goes low, the bit pointer is reset to bit zero. All rise and fall times are assumed to be 20 ns or less; therefore, timing requirements are shown referenced to 50% of the rising or falling slope of the waveform. A write operation can only be performed when CLKM is high. When CLKM is low, only a read operation can be performed.

PARAMETER MEASUREMENT INFORMATION

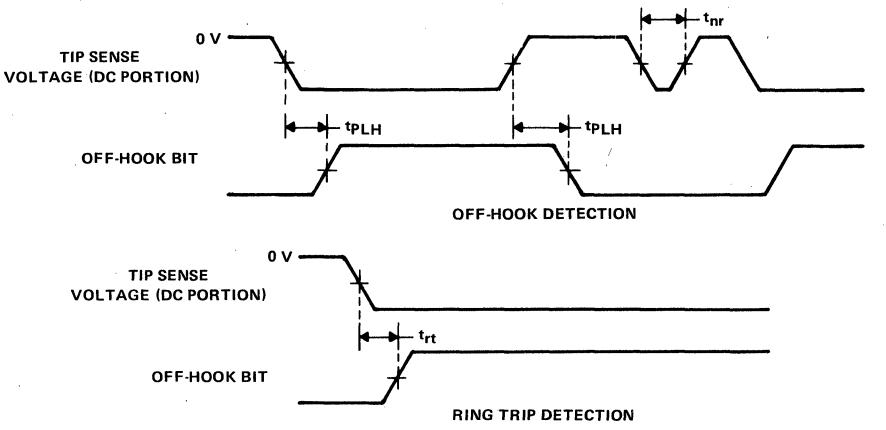
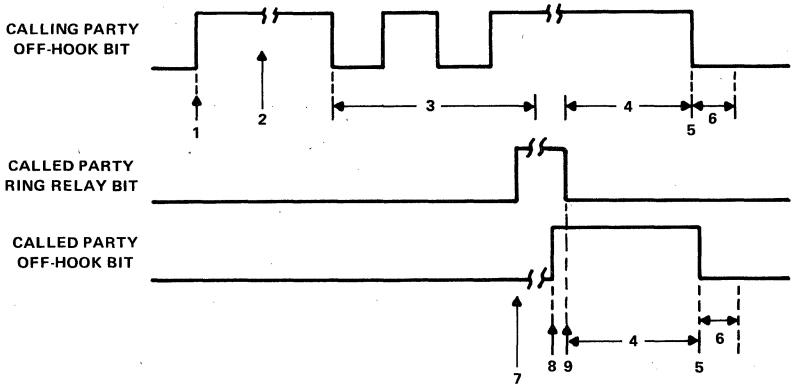


FIGURE 4. SUPERVISION TIMING WAVEFORMS

TYPICAL APPLICATION DATA



1 OFF-HOOK
2 VOICE MODE SET UP BY MICROPROCESSOR
3 DIAL PULSE COLLECTION
4 VOICE (CONVERSATION)
5 ON-HOOK
6 MICROPROCESSOR DETECTS ON-HOOK BY READING BIT "0" AND SET SYSTEM TO STANDBY MODE
7 MICROPROCESSOR ENABLES BIT "3" RING RELAY ON
8 MICROPROCESSOR DETECTS OFF-HOOK BY READING BIT "0"
9 MICROPROCESSOR DISABLES BIT "3" AND SETS THE SLCC TO VOICE MODE

FIGURE 5. MICROPROCESSOR INTERNAL POLLING (TYPICAL SEQUENCE)

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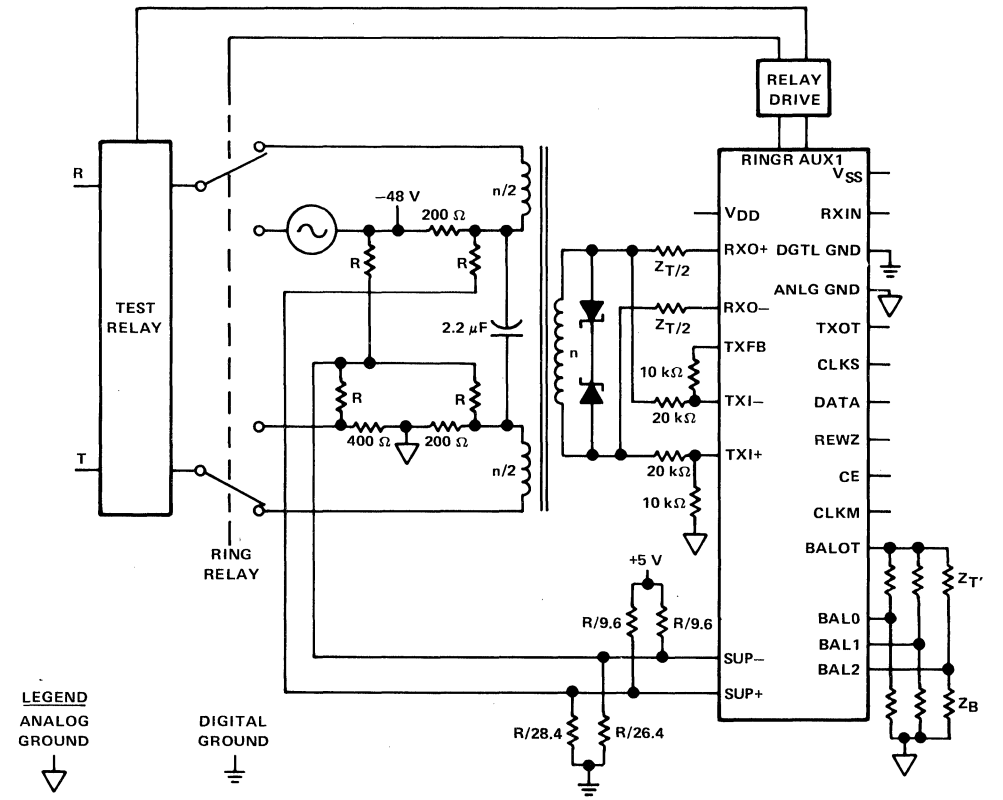
TYPICAL APPLICATION DATA (see Notes 11 and 12)

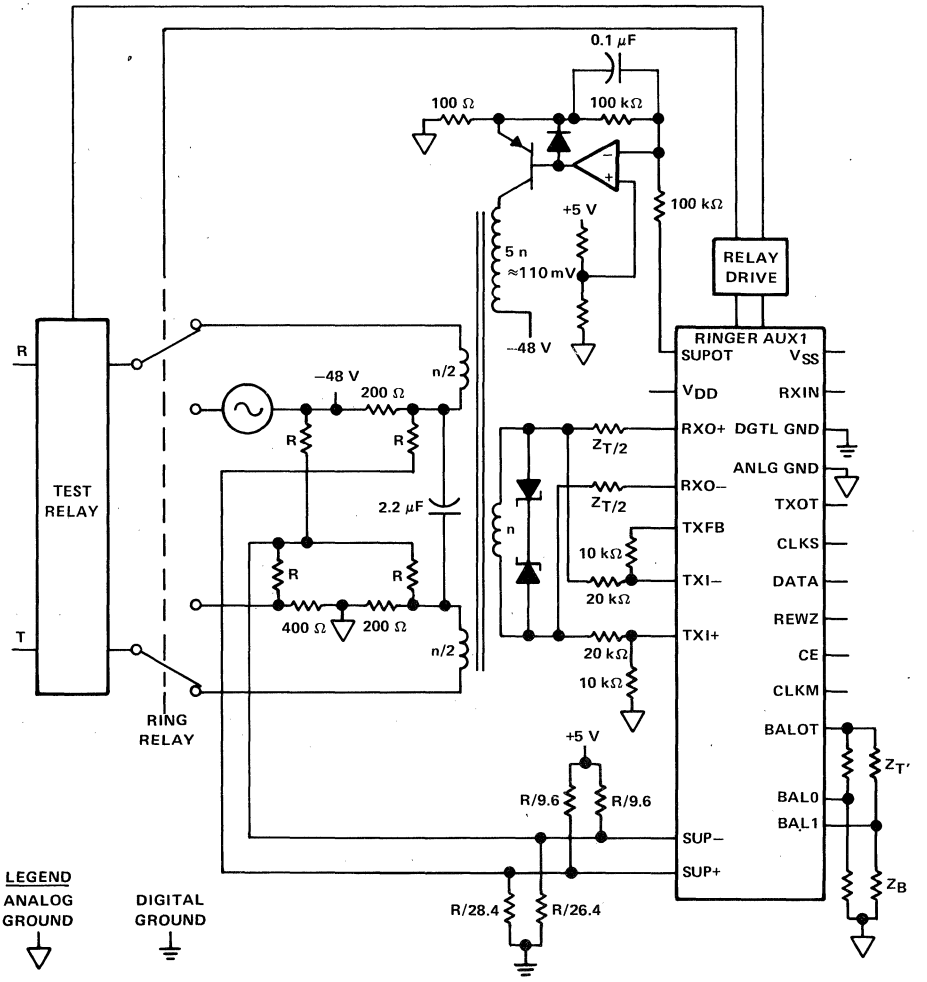


Typically, R = 600 kΩ

FIGURE 6. TCM4204A, TCM4205A SLCC STANDARD SUBSCRIBER LINE

NOTES: 11. All resistors should have tolerances of ±1% or better.
12. If the battery-feed transformer is center tapped on the SLCC side, it is recommended that the center tap be left disconnected.

TYPICAL APPLICATION DATA (see Notes 11 and 12)



Typically, R = 600 kΩ

FIGURE 7. TCM4207A SLCC STANDARD SUBSCRIBER LINE

NOTES: 11. All resistors should have tolerances of ±1% or better.
12. If the battery-feed transformer is center tapped on the SLCC side, it is recommended that the center tap be left disconnected.

TYPICAL APPLICATION DATA (see Notes 11 and 12)

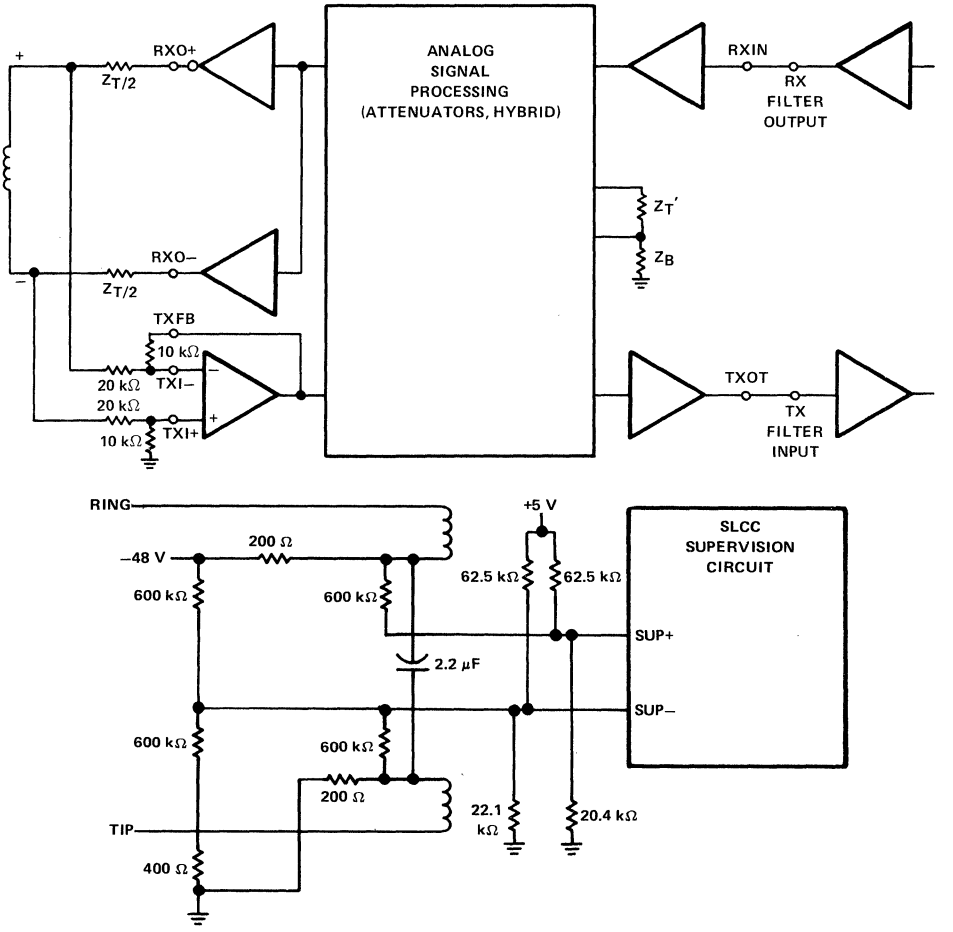


FIGURE 8. INPUT/OUTPUT OFFSETS

NOTES: 11. All resistors should have tolerances of ±1% or better.
12. If the battery-feed transformer is center tapped on the SLCC side, it is recommended that the center tap be left disconnected.

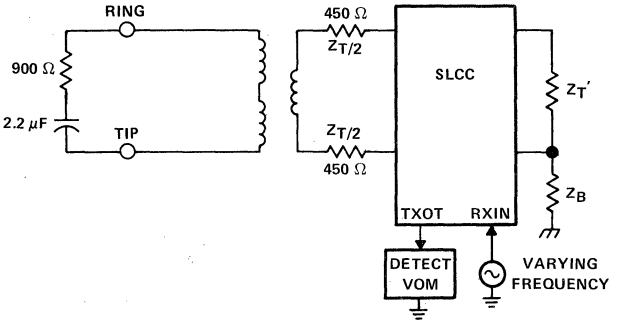


FIGURE 9. STRUCTURAL THL TEST CIRCUIT

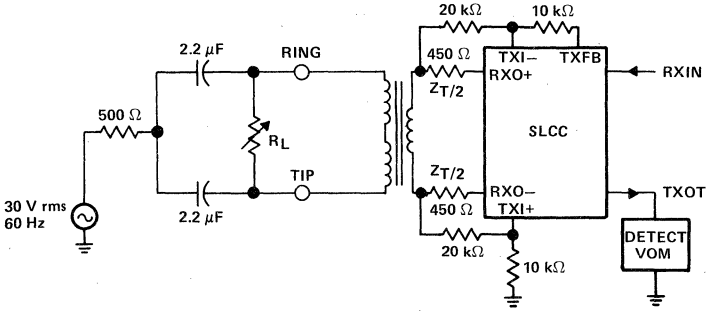
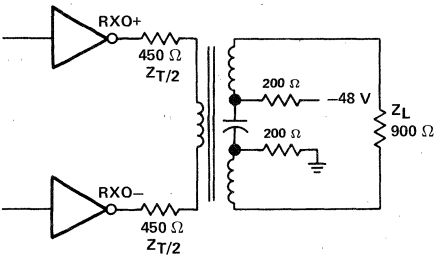


FIGURE 10. LONGITUDINAL REJECTION TEST CIRCUIT



SIGNAL LEVEL AT 900 Ω	ACROSS 900 Ω	DIFFERENTIAL RMS RXO+, RXO−	SINGLE ENDED RXO+, RXO−
6 dBmo	1.8 Vrms	5.34 Vrms	+3.78 Vpp
0 dBmo	0.95 Vrms	2.68 Vrms	+1.89 Vpp
−10 dBmo	0.30 Vrms	0.85 Vrms	+0.60 Vpp
−20 dBmo	95 mVrms	0.27 Vrms	+189 mVpp
−30 dBmo	30 mVrms	85 mVrms	+60 mVpp
−40 dBmo	9.5 mVrms	27 mVrms	+18.9 mVpp
−60 dBmo	950 μVrms	2.7 mVrms	+1.89 mVpp
−80 dBmo	95 μVrms	270 μVrms	+189 μVpp

FIGURE 11. SIGNAL LEVELS, 2W SIDE

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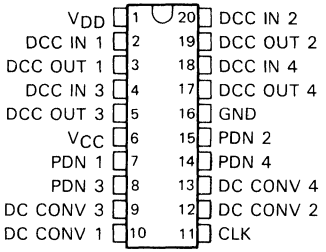
PRODUCT PREVIEW

TCM4208
SUBSCRIBER-LINE-INTERFACE CIRCUIT
QUAD DC-TO-DC CONVERTER

D2867, MARCH 1985

- Quad High-Efficiency DC-to-DC Down Converter for Line Card Applications
- Power-Up, Power-Down, and Power-Denial Modes
- High Switching Frequency, Typ 256 kHz
- 5-V and −5-V Power Supplies
- CMOS Silicon-Gate Technology for Low Active and Negligible Standby Power Dissipation
- Fast Turn On

TCM4208 . . . J
DUAL-IN-LINE PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM4208 is a quad dc-to-dc down-converter designed to provide an optional solution to minimize power dissipation when feeding analog subscriber lines. When used in conjunction with the TCM4204, TCM4205, or TCM4207 Subscriber Line Control Circuit (SLCC), the incoming dc supply voltage from the battery (or extended battery) is down-converted to feed the line without substantial line-card power dissipation. The switching frequency is synchronized to the pulse-code-modulation (PCM) clock. The use of high-frequency switching and small smoothing components allows the size of the printed circuit board (PCB) to be reduced.

The TCM4208 is characterized for operation from 0°C to 70°C.

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PIN	NAME	DESCRIPTION
1	V_{DD}	−5 V supply voltage
2	DCC IN 1	DC-control input, channel 1, is input for an on-chip amplifier and forms the control point for adjustment of supply voltage
3	DCC OUT 1	DC-control amplifier output, channel 1
4	DCC IN 3	DC-control input, channel 3, is input for an on-chip amplifier and forms the control point for adjustment of supply voltage
5	DCC OUT 3	DC-control amplifier output, channel 3
6	V_{CC}	5-V supply voltage
7	PDN 1	Power-down input, channel 1. This input has three input states†.
8	PDN 3	Power-down input, channel 3. This input has three input states†.
9	DC CONV 3	DC-to-DC converter output, channel 3. Output drives the gate of the MOS switch
10	DC CONV 1	DC-to-DC converter output, channel 1. Output drives the gate of the MOS switch
11	CLK	Input from PCM clock
12	DC CONV 2	DC-to-DC converter output, channel 2. Output drives the gate of the MOS switch
13	DC CONV 4	DC-to-DC converter output, channel 4. Output drives the gate of the MOS switch
14	PDN 4	Power-down input, channel 4. This input has three input states†.
15	PDN 2	Power-down input, channel 2. This input has three input states†.
16	GND	Ground
17	DCC OUT 4	DC-control amplifier output, channel 4
18	DCC IN 4	DC-control input, channel 4, is input for an on-chip amplifier and forms the control point for adjustment of supply voltage
19	DCC OUT 2	DC-control amplifier output, channel 2
20	DCC IN 2	DC-control input, channel 2, is input for an on-chip amplifier and forms the control point for adjustment of supply voltage

†See "Principles of Operation".

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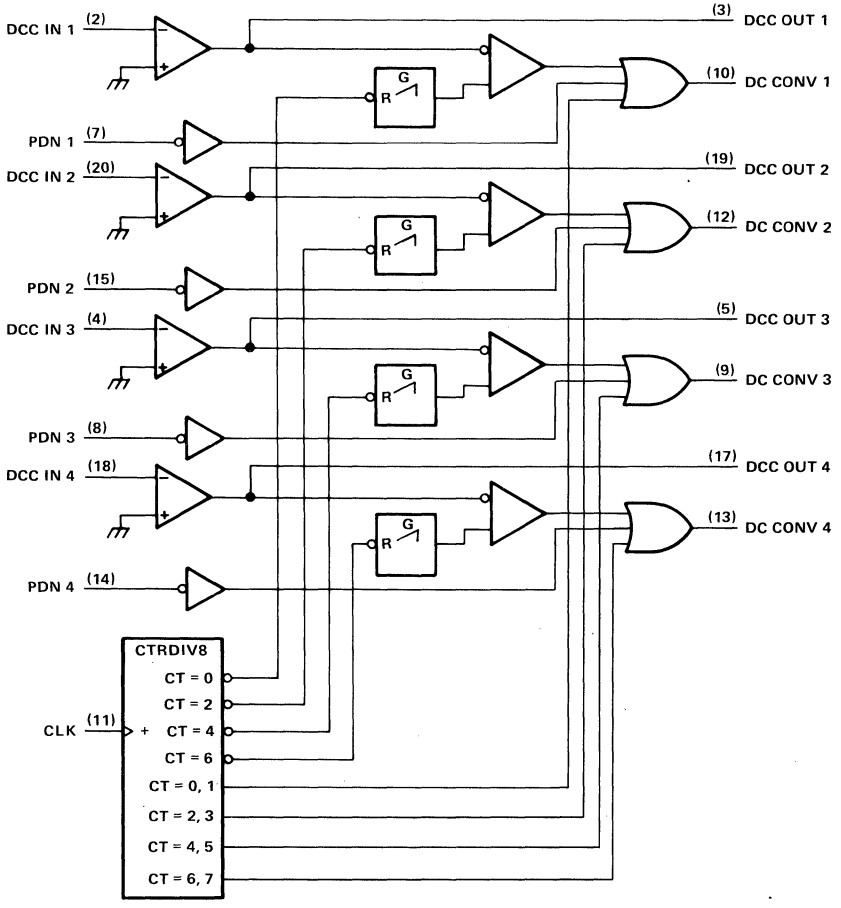
logic diagram (positive logic)



PRINCIPLES OF OPERATION

The TCM4208 is a quad dc-to-dc conversion device that is principly used in line card applications for down converting the feed voltage on short telephone lines. It can also be used in other switched power supply applications.

Each of the four channels on the TCM4208 is under the control of the PDN (power-down control) input and three states can be obtained (see functional block diagram).

operational states

1. Power down (PDN input at 0 V). The corresponding output pin (DC CONV) goes high and remains so while PDN is at 0 V. This gives 100% of the input supplied (V_{batt}) to the V_{reg} rail.
2. Power up (PDN input at 5 V). The corresponding output pin (DC CONV) goes into a switching mode, the output duty cycle being controlled by an on-chip ramp generator, amplifier, and comparator such that a precision dc output (V_{reg}) can be obtained and scaled from an input (V_{cont}).
3. Power denial (PDN input at -5 V). The corresponding output pin (DC CONV) goes into a 25% "on" switching mode causing 25% of input V_{batt} to be supplied to the V_{reg} rail.

circuit configuration

The normal configuration is as shown in the typical application data. Resistors R1 and R2 adjust the gain of the control loop in the power-up mode. The DC CONV output can be modulated from 100% on to 25% on. This occurs only when a very short line is being fed.

The switch (a small-signal N-channel VMOS transistor) is switched at 256 kHz and a 3.3-mH ferite choke and a 0.1-μF capacitor are sufficient for smoothing. The diode (a 1N914 or equivalent) should have a fast recovery to maximize the total efficiency of the system. The diode from the gate of the VMOS goes to V_i (a low-current bias voltage that is 6 to 8 volts more positive than V_{batt}), which is used to turn on the switch in the power-down mode.

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TYPICAL APPLICATION DATA

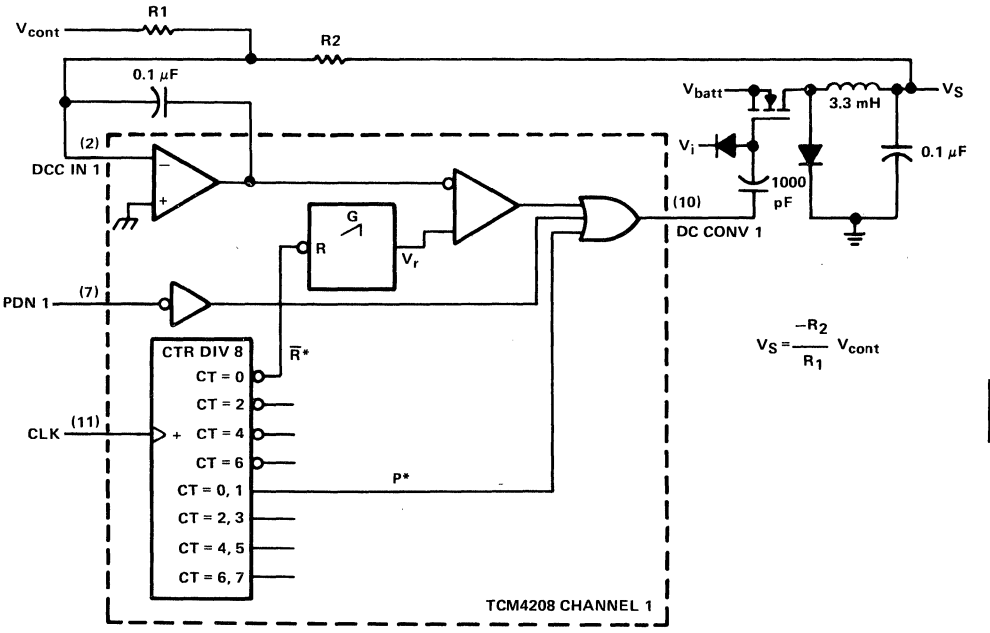


FIGURE 1. TCM4208 TYPICAL APPLICATION CIRCUIT (ONE CHANNEL ONLY)

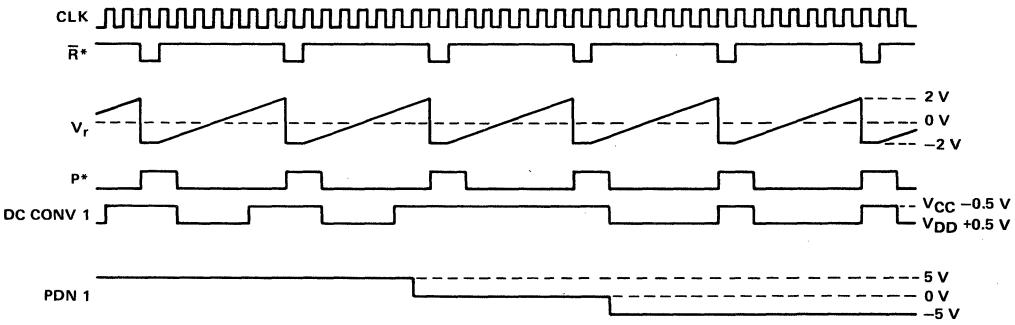


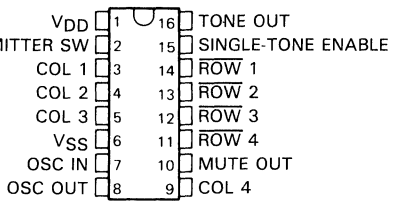
FIGURE 2. TIMING AND WAVEFORMS

*$\overline{R}$ is the ramp reset pulse occurring at one-eighth the CLK input rate. Each converter has its own ramp reset pulse and the four reset pulses are spaced at quarter bit intervals. Similarly each converter has its own P pulse lasting for two clock cycles.

D2650, NOVEMBER 1982—REVISED OCTOBER 1984

- **Low-Cost TV Color-Burst Crystal Sine-Wave Input Produces Highly Accurate and Stable Tones**
- **Device Powered Directly by Telephone or Small Batteries**
- **Keyboard or Electronic Input Capability**
- **Dual-Tone and Single-Tone Capability**
- **Minimal Standby Power Requirement**
- **Total Harmonic Distortion Meets EIA Standard RS-470**
- **PEP3 Processing Available**
- **Wide Supply-Voltage Range**
- **Minimal Parts Required**
- **Single-Tone Production Can be Inhibited**
- **Auxiliary Switching Outputs: One Bipolar Transistor and One CMOS Gate**
- **Designed to be Interchangeable with Mostek MK5087**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM5087 tone encoder is a CMOS integrated circuit designed specifically to generate the dial tones used in dual-tone telephone dialing systems. It requires a sine-wave input normally supplied by a low-cost TV color-burst crystal at 3.579545 MHz to generate eight different audio sinusoidal frequencies. With this input the encoder generates dial tones that are very low in total harmonic distortion and comply with standard Dual-Tone Multi-Frequency (DTMF) specifications without any need for frequency adjustment.

When generating a dual-tone signal, the encoder generates one column tone and one row tone and adds them for its output. The table below presents the frequencies produced by the tone encoder with the 3.579545-MHz TV-crystal signal input. Any deviation in this frequency will be reflected in the frequency output. The tolerance of the crystal is normally 0.02%.

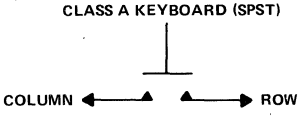
TONE	DTMF STANDARD (Hz)	ENCODER OUTPUT* (Hz)	ERROR FROM STANDARD* (%)
Row 1	697	701.3	+0.62
Row 2	770	771.4	+0.19
Row 3	852	857.2	+0.61
Row 4	941	935.1	−0.63
Column 1	1209	1215.9	+0.57
Column 2	1336	1331.7	−0.32
Column 3	1477	1471.9	−0.35
Column 4	1633	1645	+0.73

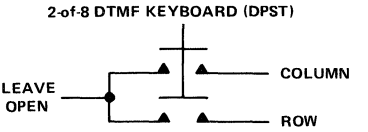
*Using an input signal from a 3.579545-MHz crystal.

operation

keyboard and electronic inputs

The specific tone or tones generated are determined by inputs designated $\overline{\text{ROW}}$ 1 through $\overline{\text{ROW}}$ 4 and COLUMN 1 through COLUMN 4. The inputs are normally received from a 2-of-8 DTMF (DPST) keyboard, a Class A (SPST) keyboard, or an electronic circuit. Unlike dynamic or scanned inputs, the static inputs of the TCM5087 do not generate noise. See function table for input and output description.





single-tone enable input

This input inhibits the generation of single tones when taken low. All other chip functions remain unchanged. If the input is high or left open, single-tone operation is enabled.

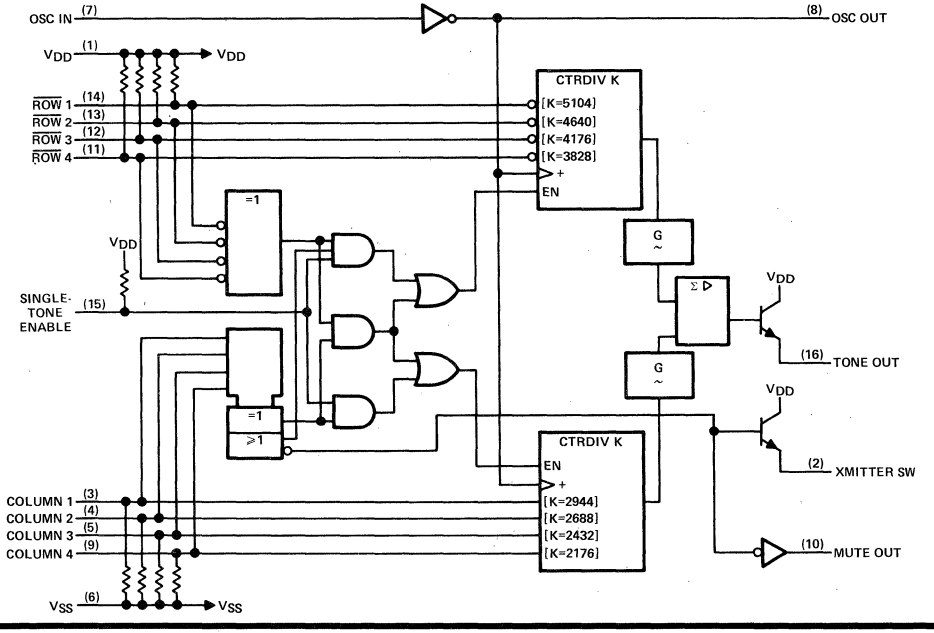
transmitter switch output

This output is at high impedance when one or more of the column inputs are active and is high when all column inputs are inactive. The output is the emitter of a bipolar transistor whose collector is at V_{DD}.

mute output

The mute output is high when one or more column inputs are active and is low when all column inputs are inactive.

functional block diagram



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TONE ENCODER FUNCTION TABLE

INPUT COMBINATIONS†	TONE OUTPUT		MUTE OUTPUT	TRANSMITTER SWITCH OUTPUT
	PIN 15‡ OPEN	PIN 15‡ AT V_{SS}		
0 rows 0 columns	0	0	L	H
1 row 1 column	Row and column	Row and column	H	Hi-Z
2 or more rows 1 column	column	0	H	Hi-Z
1 row 2 or more columns	Row	0	H	Hi-Z
2 or more rows 2 or more columns	0	0	H	Hi-Z
0 rows 1 column	Column	0	H	Hi-Z
0 rows 2 or more columns	0	0	H	Hi-Z
1 or more rows 0 columns	0	0	L	H

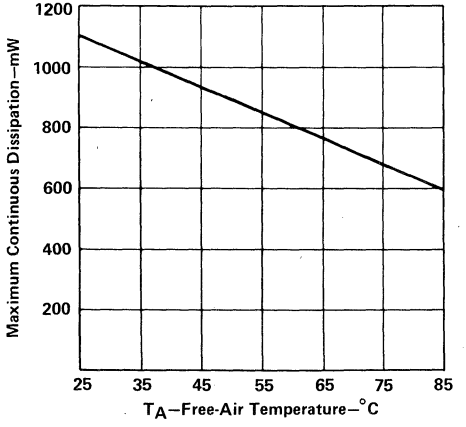
†Row inputs will be active (on) when the input voltage is at a low level ($V_I \leq V_{IL}$), and column inputs are active at a high input level. Under keyboard control, connecting a row input to a column input activates both.
‡Pin 15 is the single-tone disable input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} (see Note 1) . . . . . 13.5 V
Input voltage range . . . . . −0.3 V to V_{DD} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{DD} + 0.3 V
Continuous power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . −30°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTES: 1. All voltage values are with respect to the V_{SS} terminal.
2. For operation above 25°C free-air temperature see the Dissipation Derating Curve.

DISSIPATION DERATING CURVE



recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		3.5		10	V
High-level input voltage, V_{IH}	Row inputs (off)	0.9 V_{DD}		V_{DD}	V
	All other inputs	0.7 V_{DD}		V_{DD}	
Low-level input voltage, V_{IL}	Column inputs (off)	V_{SS}		0.1 V_{DD}	V
	All other inputs	V_{SS}		0.3 V_{DD}	
Contact resistance between row and column inputs				100	Ω
Tone-output load resistance, R_L	$V_{DD} \leq 5$ V		620		Ω
	$V_{DD} > 5$ V		330		Ω
Operating free-air temperature, T_A		−30		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Column or row input resistance			10			kΩ
	Single-tone-enable input resistance to V_{DD}		T_A = 25°C	20		100	kΩ
V_{OH}	High-level output voltage	Mute output	V_{DD} = 3 V, I_{OH} = 0.2 mA,	2			V
			V_{DD} = 10 V, I_{OH} = 0.5 mA	9			
		Transmitter switch output	V_{DD} = 3.5 V, I_{OH} = −15 mA	1.5	2.5		
			V_{DD} = 10 V, I_{OH} = −40 mA	8			
V_{OL}	Low-level output voltage, mute output		V_{DD} = 3 V, I_{OL} = −0.2 mA			0.5	V
			V_{DD} = 10 V, I_{OL} = −0.5 mA			0.5	
I_{OL}	Off-state current transmitter switch output		V_{DD} = 10 V, V_O = 0 V			10	μA
I_{DDstby}	Standby supply current with outputs unloaded		V_{DD} = 3.5 V		0.25	100	μA
			V_{DD} = 10 V		0.5	200	
I_{DDop}	Operating current		V_{DD} = 3.5 V, See Note 3		1	2	mA
			V_{DD} = 10 V, See Note 3		5	10	

operating characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
Output rms voltage	Row tone	R_L = 330 Ω to 1 kΩ,	317	400	500	mV
	Column tone	T_A = 25°C	396	500	630	
Preemphasis (column tone to row tone)			1	2	3	dB
Dual-tone output distortion (see Note 4)		$V_{DD} \geq 4$ V			−20	dB
Quiescent tone-output power					−80	dBm
Tone-output rise time (see Note 5)				3	5	ms

†Unless otherwise noted, test conditions are: R_L = 620 Ω for $V_{DD} \leq 5$ V or R_L = 330 Ω for $V_{DD} > 5$ V. Crystal parameters are the following: f = 3.579545 MHz ±0.02%, R_S < 100 Ω, C_L = 18 pF, C_M = 0.02 pF, C_H = 5 pF, L_M = 96 mH.

NOTES: 3. Operating current is measured with all outputs unloaded, one row input connected to one column input, and normal oscillator input.

4. Distortion is expressed as the ratio of total out-of-band power relative to the total fundamental power for the dual tone.

5. This is the time required for output to change from its quiescent value to 90% of its final rms value.

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output waveforms

Typical row and column stairstep approximations of sinusoidal outputs are shown in Figures 1 and 2. The row and column outputs are added together resulting in a typical dual-tone waveform as shown in Figure 3. Spectral analysis of this dual-tone waveform shows that all harmonic and intermodulation distortions are typically 30 dB below the strongest column-tone fundamental.

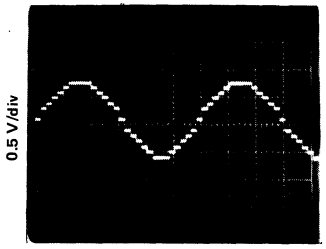


FIGURE 1

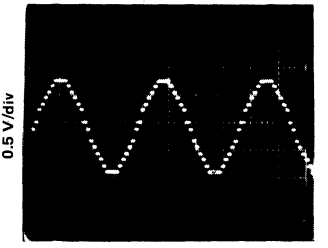


FIGURE 2

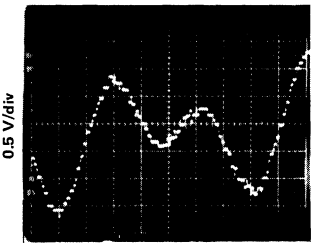


FIGURE 3

distortion considerations

The following formula is used to calculate the total harmonic distortion of a single row or a single column:

$$\text{THD} = \left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + V_{5f}^2 + \ldots + V_{nf}^2}}{V_{1f}}\right) \times 100\%$$

where V_{2f} is the second harmonic of the fundamental frequency V_{1f} waveform and so on. The dual-tone total harmonic distortion is:

$$\text{THD} = \left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 + \ldots + V_{nR}^2 + V_{2C}^2 + \ldots V_{nC}^2 \pm V_{IMD}^2}}{\sqrt{V_{FR}^2 + V_{FC}^2}}\right) \times 100\%$$

where V_{FR} and V_{FC} are the row and column fundamental frequency waveforms, and V_{2R} and V_{2C}, etc., are the corresponding harmonics.

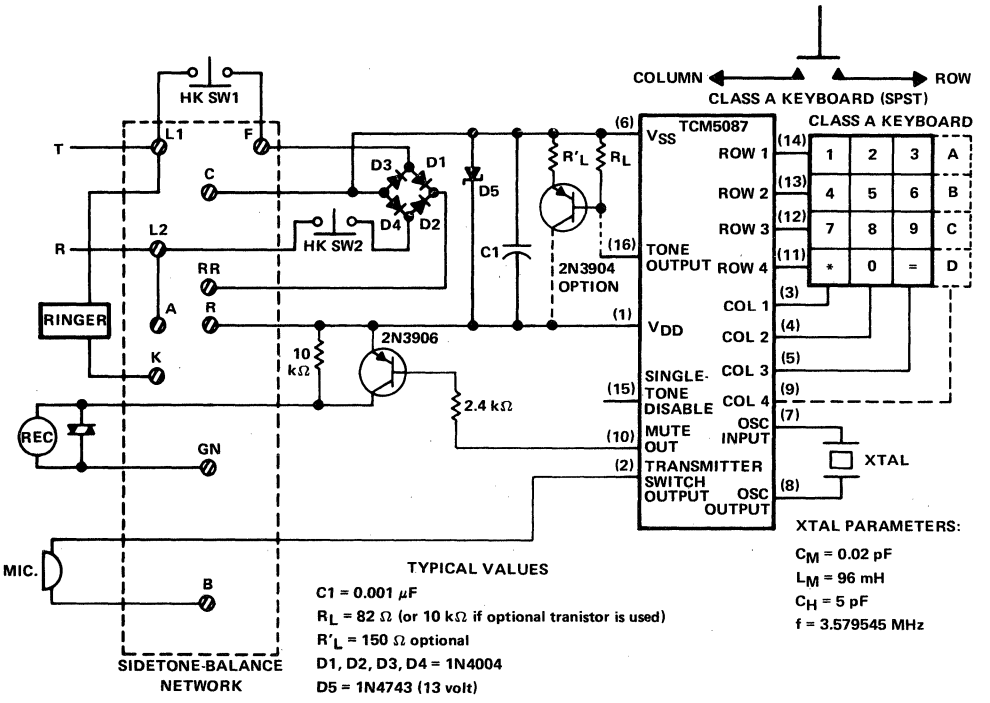
The total intermodulation distortion is:

$$V_{IMD}^2 = (V_{1R} + V_{1C})^2 + (V_{1R} - V_{1C})^2 + \ldots + (V_{nr} + V_{nC})^2 + (V_{nR} - V_{nC})^2$$

A relatively simple method of distortion measurement uses a spectrum analyzer to relate the harmonics to the fundamental frequency waveform. The tone encoder spectrum indicates the harmonics and intermodulation distortion at least 30 dB down relative to the column tone.

Another method for distortion measurement of the dual-tone waveform is to compare the total power in the fundamental frequencies with the total power in the various harmonics plus intermodulation on a signal analyzer. The encoders provide an output distortion of -20 dB maximum when operated between 3.5 volts and 10 volts. If operated between 3 volts and 3.5 volts, some clipping occurs at the output causing the distortion to exceed the -20 dB level.

TYPICAL APPLICATIONS DATA



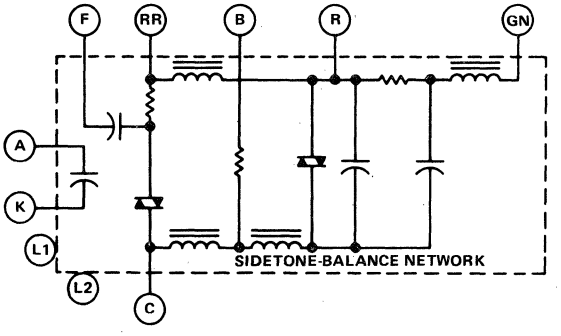


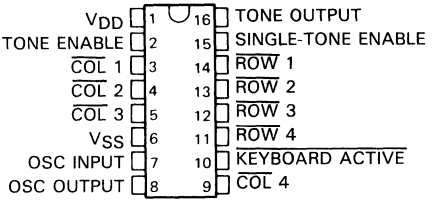
FIGURE 4. TYPICAL APPLICATION USING HYBRID COIL SIDETONE-BALANCE NETWORK, ELECTRONIC SWITCHING, AND LOW-COST (CLASS A) KEYBOARD

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

D2651, NOVEMBER 1982—REVISED OCTOBER 1984

- **Low-Cost TV Color-Burst Crystal Sine-Wave Input Produces Highly Accurate and Stable Tones**
- **Device Powered Directly by Telephone or Small Batteries**
- **Keyboard or Electronic Input Capability**
- **Dual-Tone and Single-Tone Capability**
- **Minimal Standby Power Requirement**
- **Total Harmonic Distortion Meets EIA Standard RS-470**
- **PEP3 Processing Available**
- **Wide Supply-Voltage Range**
- **Minimal External Parts Required**
- **Single-Tone Production Can be Inhibited**
- **Separate Tone Enable Provided**
- **Auxiliary Switching Bipolar Transistor Available**
- **Designed to be Interchangeable with Mostek MK5089**

N PACKAGE
(TOP VIEW)



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM5089 tone encoder is a CMOS integrated circuit designed specifically to generate the dial tones used in dual-tone telephone dialing systems. It requires a sine-wave input normally supplied by a low-cost TV color-burst crystal at 3.579545 MHz to generate eight different audio sinusoidal frequencies. With this input the encoder generates dial tones that are very low in total harmonic distortion and comply with standard Dual-Tone Multi-Frequency (DTMF) specifications without any need for frequency adjustment.

When generating a dual-tone signal, the encoder generates one column tone and one row tone and adds them for its output. The table below presents the frequencies produced by the tone encoder with the 3.579545-MHz TV-crystal signal input. Any deviation in this frequency will be reflected in the frequency output. The tolerance of the crystal is normally 0.02%.

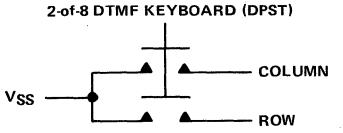
TONE	DTMF STANDARD (Hz)	ENCODER OUTPUT* (Hz)	ERROR FROM STANDARD* (%)
Row 1	697	701.3	+0.62
Row 2	770	771.4	+0.19
Row 3	852	857.2	+0.61
Row 4	941	935.1	−0.63
Column 1	1209	1215.9	+0.57
Column 2	1336	1331.7	−0.32
Column 3	1477	1471.9	−0.35
Column 4	1633	1645	+0.73

*Using an input signal from a 3.579545-MHz crystal.

operation

keyboard and electronic inputs

The specific tone or tones generated are determined by inputs designated $\overline{\text{ROW}}$ 1 through $\overline{\text{ROW}}$ 4 and $\overline{\text{COLUMN}}$ 1 through $\overline{\text{COLUMN}}$ 4. These input levels are normally received from a 2-of-8 DTMF (DPST) keyboard or from an electronic circuit. Unlike dynamic or scanned inputs, the static inputs of the TCM5089 do not generate any noise. See function table for input and output description.



single-tone enable input

This inhibits the generation of single tones when taken low or left open. However, all other chip functions remain unchanged. If the input is high, single-tone operation is enabled.

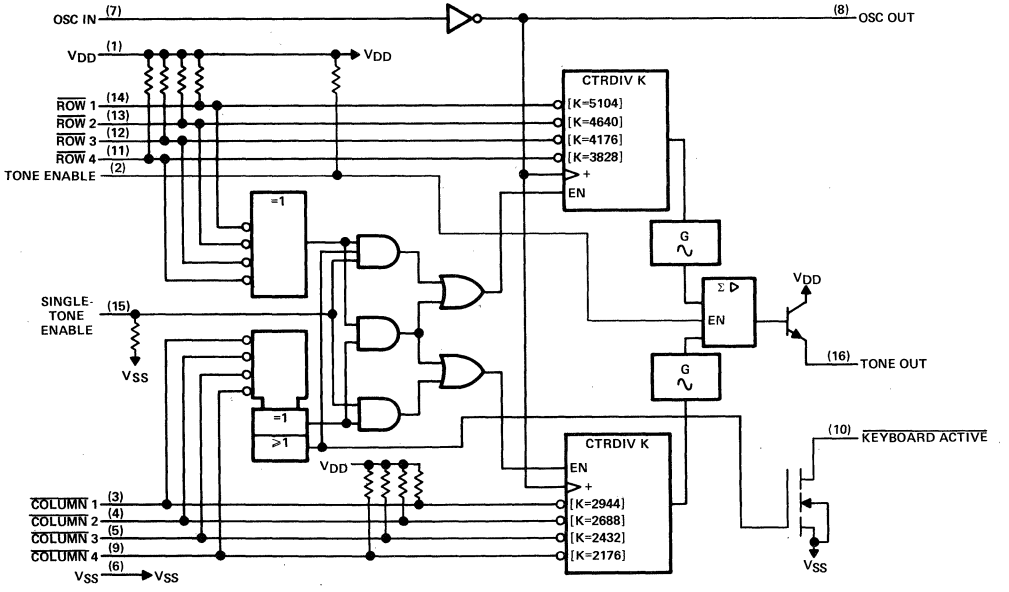
tone enable input

The tone enable input, when low, disables the tone output of the encoder. Other chip functions remain unchanged.

keyboard active output

This output provides for switching of an external receiver, transmitter, or other functions. The output is low whenever one or more column inputs are active and at a high impedance when all column inputs are inactive.

functional block diagram



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TONE ENCODER FUNCTION TABLE

INPUT COMBINATIONS†	TONE OUTPUT			KEYBOARD ACTIVE OUTPUT
	PIN 2 OPEN‡ PIN 15 at V_{DD}‡	PIN 2 OPEN‡ PIN 15 at V_{SS}‡	PIN 2 AT V_{SS}‡	
0 rows 0 Columns	0	0	0	Hi-Z
1 row 1 column	Row and column	Row and column	0	L
2 or more rows 1 column	column	0	0	L
1 row 2 or more columns	Row	0	0	L
2 or more rows 2 or more columns	0	0	0	L
0 rows 1 column	Column	0	0	L
0 rows 2 or more columns	0	0	0	L
1 or more rows 0 columns	0	0	0	Hi-Z

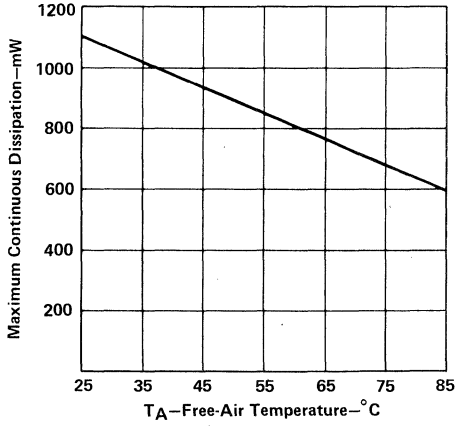
†An inactive level can be produced by an open circuit. Under voltage-level control, row and column inputs will be active when low as defined by V_{IL} in recommended operating conditions.
‡Pin 15 is the single-tone enable input; Pin 2 is the tone-enable input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} (see Note 1) . . . . . 13.5 V
Input voltage range . . . . . -0.3 V to V_{DD} + 0.3 V
Output voltage range . . . . . -0.3 V to V_{DD} + 0.3 V
Continuous power dissipation at 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . -30°C to 70°C
Storage temperature range . . . . . -55°C to 150°C

NOTES: 1. All voltage values are with respect to the V_{SS} terminal.
2. For operation above 25°C see the Dissipation Derating Curve.

DISSIPATION DERATING CURVE



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3		10	V
High-level input voltage, any input, V_{IH}	0.7 V_{DD}		V_{DD}	V
Low-level input voltage, any input, V_{IL}	V_{SS}		0.3 V_{DD}	V
Operating free-air temperature, T_A	−30		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input resistance, single-tone input to V_{SS}		20		100	kΩ
I_{OH}	High-level output current, keyboard active output	V_O = 5 V†			2	μA
I_{OL}	Low-level output current, keyboard active output	V_O = 0.5 V†	−500			μA
I_{DDstby}	Standby power supply current	V_{DD} = 10 V, See Note 3			200	μA
I_{DDop}	Operating power supply current	V_{DD} = 3.5 V, See Note 4			2	mA

operating characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output rms voltage	Row tone	V_{DD} = 3.5 V, R_L = 10 kΩ	235		365	mV
	Column tone		275		516	
Preemphasis (column-tone to row-tone)		R_L = 10 kΩ	2.4		3	dB
Dual-tone output distortion (see Note 5)		V_{DD} ≥ 3.5 V, R_L = 10 kΩ			−20	dB
Quiescent tone-output power		R_L = 10 kΩ			−80	dBm
Tone-output rise time (see Note 6)				2.8	5	ms

†V_O is the dc bias on the keyboard-active output.
‡Crystal parameters are as follows: f = 3.579545 MHz ±0.02%, R_S ≤ 100 Ω, C_L = 18 pF, C_M = 0.02 pF, and L_M = 96 mH.
NOTES: 3. Standby power supply current is measured with no inputs activated.
4. Operating current is measured with all outputs unloaded, one row inut and one column input active, and normal oscillator input.
5. Distortion is expressed as the ratio of total out-of-band power relative to the total fundamental power for the dual tone.
6. This is the time required for the output to change from its quiescent value to 90% of its final rms value.

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output waveforms

Typical row and column stairstep approximations of sinusoidal outputs are shown in Figures 1 and 2. The row and column outputs are added together resulting in a typical dual-tone waveform as shown in Figure 3. Spectral analysis of this dual-tone waveform shows that all harmonic and intermodulation distortions are typically 30 dB below the strongest column-tone fundamental.

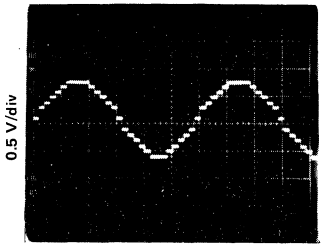


FIGURE 1

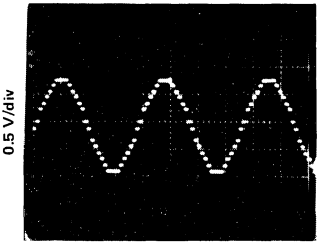


FIGURE 2

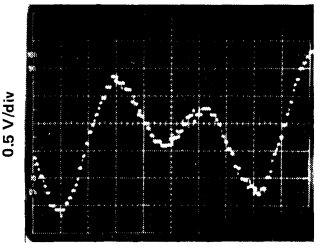


FIGURE 3

distortion considerations

The following formula is used to calculate the total harmonic distortion of a single row or a single column:

$$THD = \left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + V_{5f}^2 + \ldots + V_{nf}^2}}{V_{1f}} \right) \times 100\%$$

where V_{2f} is the second harmonic of the fundamental frequency V_{1f} waveform and so on. The dual-tone total harmonic distortion is:

$$THD = \left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 + \ldots + V_{nR}^2 + V_{2C}^2 + \ldots V_{nC}^2 \pm V_{IMD}^2}}{\sqrt{V_{FR}^2 + V_{FC}^2}} \right) \times 100\%$$

where V_{FR} and V_{FC} are the row and column fundamental frequency waveforms, and V_{2R} and V_{2C}, etc. are the corresponding harmonics.

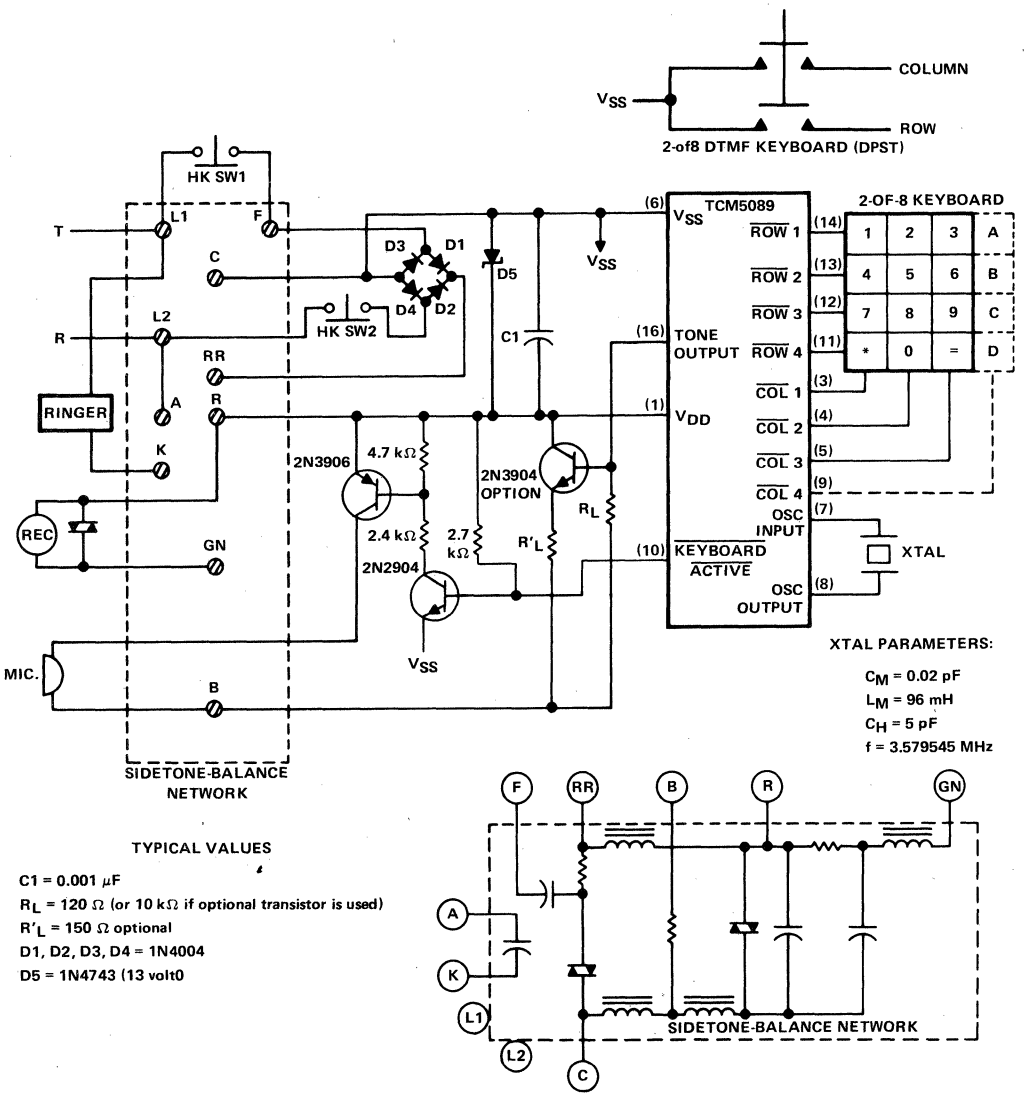
The total intermodulation distortion is:

$$V_{IMD}^2 = (V_{1R} + V_{1C})^2 + (V_{1R} - V_{1C})^2 + \ldots + (V_{nr} + V_{nC})^2 + (V_{nR} - V_{nC})^2$$

A relatively simple method of distortion measurement uses a spectrum analyzer to relate the harmonics to the fundamental frequency waveform. The tone encoder spectrum indicates the harmonics and intermodulation distortion at least 30 dB down relative to the column tone.

Another method for distortion measurement of the dual-tone waveform is to compare the total power in the fundamental frequencies with the total power in the various harmonics plus intermodulation on a signal analyzer. The encoders provide an output distortion of −20 dB maximum when operated between 3.5 volts and 10 volts. If operated between 3 volts and 3.5 volts, some clipping occurs at the output causing the distortion to exceed the −20 dB level.

APPLICATIONS INFORMATION



TYPICAL VALUES

C1 = 0.001 μF
R_L = 120 Ω (or 10 kΩ if optional transistor is used)
R'_L = 150 Ω optional
D1, D2, D3, D4 = 1N4004
D5 = 1N4743 (13 volt0

FIGURE 4. TYPICAL APPLICATION USING HYBRID COIL SIDETONE-BALANCE NETWORK, ELECTRONIC SWITCHING, AND LOW-COST (CLASS A) KEYBOARD

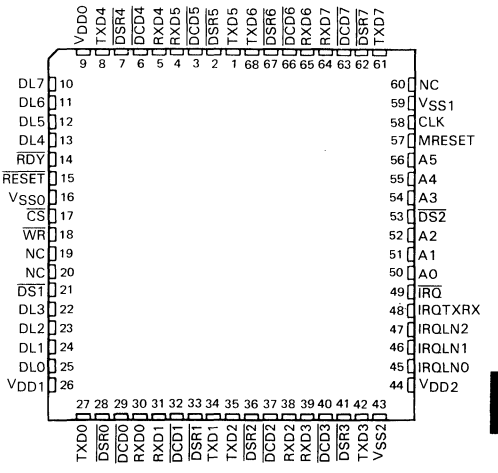
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TCM78808
OCTAL ASYNCHRONOUS RECEIVER/TRANSMITTER

D2941, APRIL 1986

- Eight Independent Full-Duplex Serial Data Lines
- Programmable Baud Rates Individually Selectable for the Transmitter/Receiver of Each Line (50 to 19,200 Baud)
- Summary Registers Allow a Single Read to Detect a Data Set Change or to Determine the Cause of an Interrupt on Any Line
- Triple Buffers for Each Receiver
- Device Scanner Mechanism Reports Interrupt Requests Due to Transmitter/Receiver Interrupts
- Independently Programmable Lines for Interrupt-Driven Operation
- Modem Status Change Detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) Signals
- Programmable Interrupts for Modem Status Changes
- Synchronizes Critical Read-Only Registers
- Replaces Eight Signetics 2661 UARTs

FN, HA, OR HB PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TCM78808 octal asynchronous receiver/transmitter is designed for the new generations of asynchronous serial communications and for microcomputer systems. The device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on eight independent lines.

On-chip baud rate generation allows the designer to select and program any one of 16 rates between 50 and 19,200 baud. Baud rates are selectable for each receiver and transmitter. A built-in scanning mechanism provides an alternative to the customary polling of status registers.

The TCM78808 functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its eight serial data lines (stop bits, parity, character length, baud rates, etc.). Each individual serial line functions as a one-line UART-type device.

An integral interrupt scanner checks for device interrupt conditions on the eight lines of the TCM78808. Its scanning algorithm is designed to give priority to receivers over transmitters. The scanner can also be programmed to check for interrupts due to changes in modem control signals (DSR and DCD).

The TCM78808 contains two types of programmable registers: line specific and summary. The six line-specific registers provide independent control of each of the eight serial lines. Two summary registers consolidate information about the current state of all eight lines and allows programs to service device interrupts quickly and efficiently.

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Each of the eight serial data lines in the TCM78808 has a set of line-specific registers for buffering data into and out of the line and for external control of line characteristics. The receiver buffer register comprises a character assembly register plus a two-entry first-in first-out (FIFO) buffer. The transmitter holding register provides similar functions on the output side. Information about the current state of the given line is contained in the (read-only) status register. Two mode registers control communications parameters. One mode register handles stop bits, parity, character length, and modem control interrupt enable (MCIE). The second mode register sets the incoming and outgoing baud rates. The command register controls various other functions of the given line.

The TCM78808 has a pair of summary registers that provide the current status of all eight serial data lines. This makes it possible to determine that line status has changed with a single read operation. The (read-only) interrupt summary register indicates that an interrupt has occurred, and contains both the line number that generated the interrupt and the corresponding direction of flow (transmitter or receiver). With both MCIE set and receiver interrupt enable, the interrupt summary register will respond to changes in $\overline{DSR}$ or $\overline{DCD}$. The data-set-change summary register monitors changes in $\overline{DSR}$ or $\overline{DCD}$ on a line-by-line basis and indicates whether a modem status change has occurred on each data line subsequent to the last time the corresponding bit was cleared.

The TCM78808 is characterized for operation from 0°C to 70°C.

SIGNAL	DESCRIPTION
A0 THRU A5	Address bits 0 through 5 select the internal registers in the TCM78808.
CLK	Clock input for timing
$\overline{CS}$	Chip Select. When low, activates the TCM78808 to receive and transmit data over data lines DL0 through DL7.
$\overline{DCD0}$ THRU $\overline{DCD7}$	Data-Set Carrier Detect inputs monitor data-set carrier detect signals from modems.
DL0 THRU DL7	Data Lines 0 through 7 receive and transmit the parallel data.
$\overline{DS1}$, $\overline{DS2}$	Data Strobes 1 and 2 receive timing information for data transfers. The DS1 and DS2 inputs must be connected together.
$\overline{DSR0}$ THRU $\overline{DSR7}$	Data Set Ready inputs monitor data-set-ready signals from modems.
$\overline{IRQ}$	Interrupt Request output requests a processor interrupt.
IRQLN0 THRU IRQLN2	Interrupt Request Line number outputs indicate the line number of the originating interrupt request.
IRQTXRX	Interrupt Request Transmit/Receive output indicates whether an interrupt request is for transmitting or receiving data.
MRESET	Manufacturing Reset. For manufacturing use
$\overline{RDY}$	Ready output indicates when the TCM78808 is ready to participate in data-transfer cycles.
$\overline{RESET}$	Reset input initializes the internal logic.
RXD0 THRU RXD7	Receive Data inputs accept asynchronous bit-serial data input streams.
TXD0 THRU TXD7	Transmit Data output provides asynchronous bit-serial data output streams.
V_{DD0} THRU V_{DD2}	5-volt nominal power supply
V_{SS0} THRU V_{SS2}	Ground reference
$\overline{WR}$	Write input specifies direction of data transfer on the DL0 through DL7 lines.

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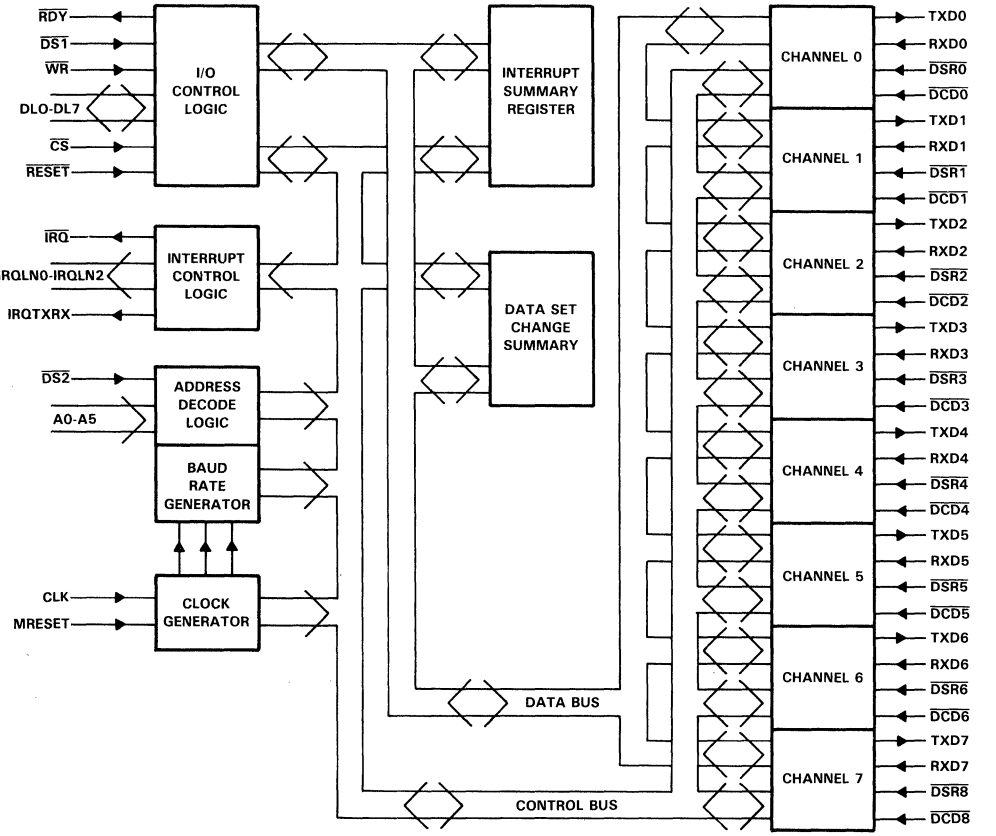
functional block diagram



absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{DD} . . . . . 7 V
Input voltage, V_I . . . . . −5 V to 7 V
Input current, I_I . . . . . −30 mA to 5 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5.25 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} for DL0 thru DL7 = −1 mA, I_{OH} for all other (except $\overline{IRQ}$ and $\overline{RDY}$) = −2 mA	2.4		V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} for DL0 thru DL7 = 5.5 mA, I_{OL} for all other = 3.5 mA		0.4	V
I_{IH}	High-level input current		V_I = 5.25 V		10	μA
I_{IL}	Low-level input current		V_I = 0		−10	μA
I_{OS}†	Short-circuit output current	DL0-DL7	V_{DD} = 5.25 V	−50	−180	mA
		All other outputs except $\overline{IRQ}$ and $\overline{RDY}$		−30	−110	
I_{OZH}‡	Off-state output current, high-level voltage applied		V_O = 2.4 V		−10	μA
I_{OZL}‡	Off-state output current, low-level voltage applied		V_O = 0.4 V		10	μA
I_{DD}	Supply current		V_{DD} = 5 V, T_A = 25°C		240	mA
C_i	Input capacitance				4	pF
C_{io}§	Input/output capacitance				5	pF

† Not more than one output should be short circuited at a time, and the duration of the short should not exceed one second.
‡ All three-state output drivers are wired in an I/O configuration. The parameters include the driver and receiver input currents.
§ This parameter includes the capacitive loads of the output driver and the receiver input.

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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

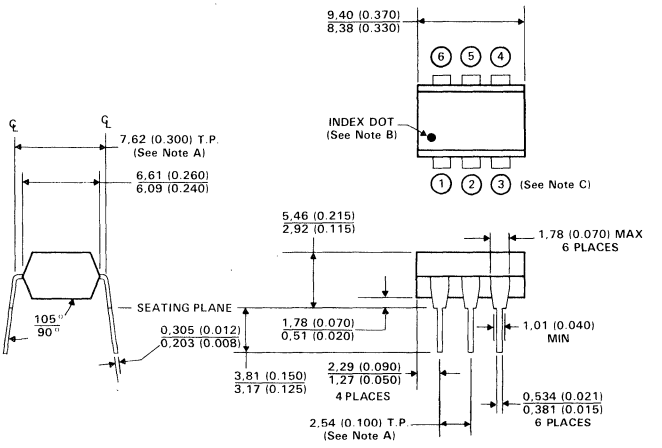
D2906, OCTOBER 1985

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation . . . 2.5 kV rms (3.535 kV peak)**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching: t_r = 2 μs Typ, t_f = 2 μs Typ**
- **UL Recognized — File #E65085**
- **Primarily Used with Telephone Ring Detector TCM1520A and Tone Drivers TCM1501A, TCM1506A, and TCM1512A**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-pin lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES: A. Leads are within 0,13 mm (0.005 inch) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. Terminal connections:
1. Anode
2. Cathode
} Infrared-emitting diode
3. No internal connection
4. Emitter
5. Collector
6. Base
} Phototransistor

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

CP-7

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Input-to-output voltage . . . . . ±2.5 kV rms (±3.535 kV peak)
Collector-base voltage . . . . . 70 V
Collector-emitter voltage (see Note 1) . . . . . 30 V
Emitter-collector voltage . . . . . 7 V
Emitter-base voltage . . . . . 7 V
Input-diode reverse voltage . . . . . 3 V
Input-diode continuous forward current at (or below) 25°C free-air temperature (see Note 2) . . . . . 100 mA
Continuous power dissipation at (or below) 25°C free-air temperature
Infrared-emitting diode (see Note 3) . . . . . 150 mW
Phototransistor (see Note 4) . . . . . 150 mW
Total, infrared-emitting diode plus phototransistor (see Note 5) . . . . . 250 mW
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
5. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)CBO}$	Collector-base breakdown voltage		I_C = 10 μA,	I_E = 0,	I_F = 0	70			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage		I_C = 1 mA,	I_B = 0,	I_F = 0	30			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage		I_E = 10 μA,	I_C = 0,	I_F = 0	7			V
I_R	Input diode static reverse current		V_R = 3 V					10	μA
$I_{C(on)}$	On-state collector current	Phototransistor operation	V_{CE} = 0.4 V,	I_F = 0.8 mA,	I_B = 0	100			μA
			V_{CE} = 0.4 V,	I_F = 10 mA,	I_B = 0	5			mA
		Photodiode operation	V_{CB} = 0.4 V,	I_F = 16 mA,	I_E = 0	7	20		μA
$I_{C(off)}$	Off-state collector current	Phototransistor operation	V_{CE} = 10 V,	I_F = 0,	I_B = 0		1	50	nA
		Photodiode operation	V_{CB} = 10 V,	I_F = 0,	I_E = 0		0.1	20	
h_{FE}	Transistor static forward current transfer ratio		V_{CE} = 5 V,	I_C = 10 mA,	I_F = 0	200	550		
V_F	Input diode static forward voltage		I_F = 16 mA				1.2	1.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage		I_C = 5 mA,	I_F = 10 mA,	I_B = 0		0.25	0.4	V
r_{IO}	Input-to-output internal resistance		V_{in-out} = ±500 V,	See Note 6		10^{11}			Ω
C_{io}	Input-to-output capacitance		V_{in-out} = 0,	f = 1 MHz,	See Note 6		1	1.3	pF

NOTE 6: These parameters are measured between both input-diode leads shorted together and all the phototransistor leads shorted together.

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	Phototransistor operation	V_{CC} = 10 V, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1		2	10	μs
t_f	Fall time				2	10	
t_r	Rise time	Photodiode operation	V_{CC} = 10 V, $I_{C(on)}$ = 20 μA, R_L = 1 kΩ, See Test Circuit B of Figure 1		1		μs
t_f	Fall time				1		

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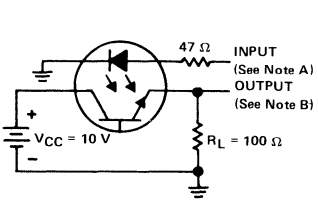
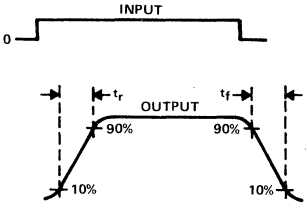
PARAMETER MEASUREMENT INFORMATION

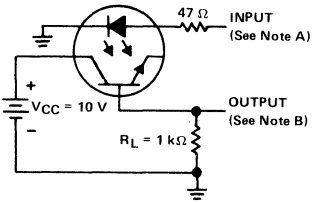
Adjust amplitude of input pulse for:
$I_{C(on)}$ = 2 mA (Test Circuit A) or
$I_{C(on)}$ = 20 μA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION



VOLTAGE WAVEFORMS



TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, $t_r \leq$ 15 ns, duty cycle ≈ 1%, t_w = 100 μs.
B. The output waveform is monitored on an oscilloscope with the following characteristics: $t_r \leq$ 12 ns, $R_{in} \geq$ 1 MΩ, $C_{in} \leq$ 20 pF.

FIGURE 1. SWITCHING TIMES

TYPICAL CHARACTERISTICS

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

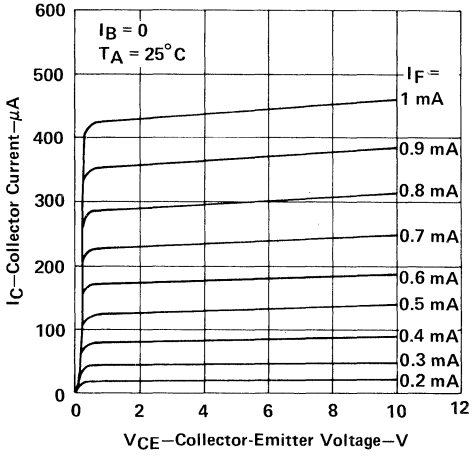


FIGURE 2

COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

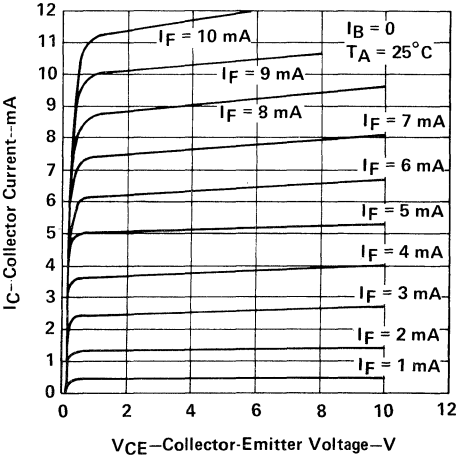


FIGURE 3

TYPICAL CHARACTERISTICS

PHOTOTRANSISTOR COLLECTOR CURRENT
vs
INPUT DIODE FORWARD CURRENT

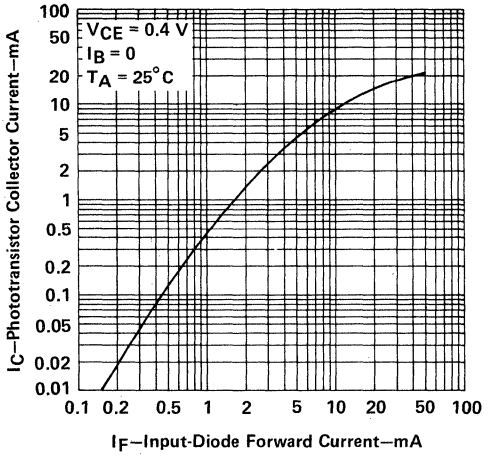


FIGURE 4

RELATIVE ON-STATE COLLECTOR CURRENT
vs
FREE-AIR TEMPERATURE

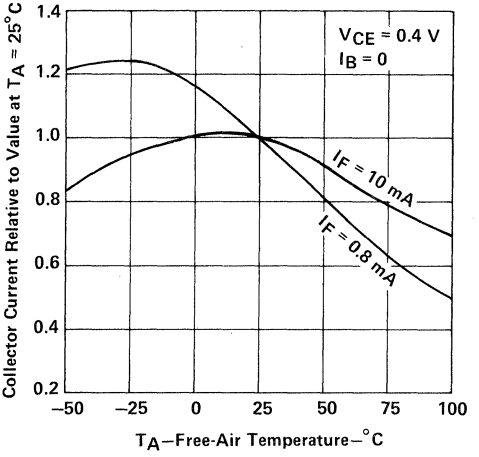


FIGURE 5

NORMALIZED TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

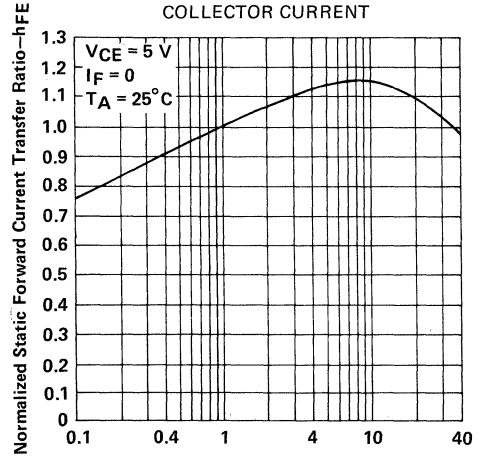


FIGURE 6

NORMALIZED TRANSISTOR STATIC FORWARD
CURRENT TRANSFER RATIO
vs
FREE-AIR TEMPERATURE

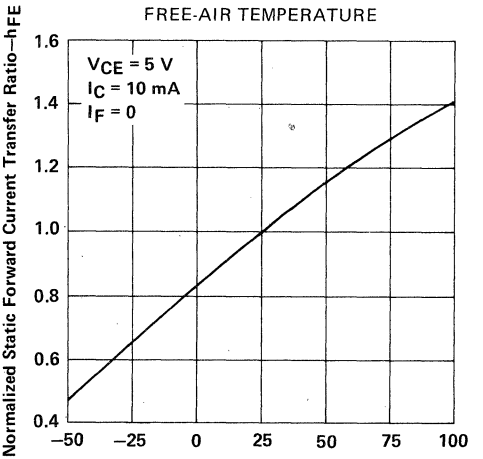


FIGURE 7

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PRODUCT PREVIEW

TISP108A
DUAL ASYMMETRICAL TRANSIENT VOLTAGE SUPPRESSOR

D2929, APRIL 1986

FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common . . . 82 V Max**
- **Surge Current 8/20 μs . . . 150 A**
- **Holding Current . . . 150 mA Min**

description

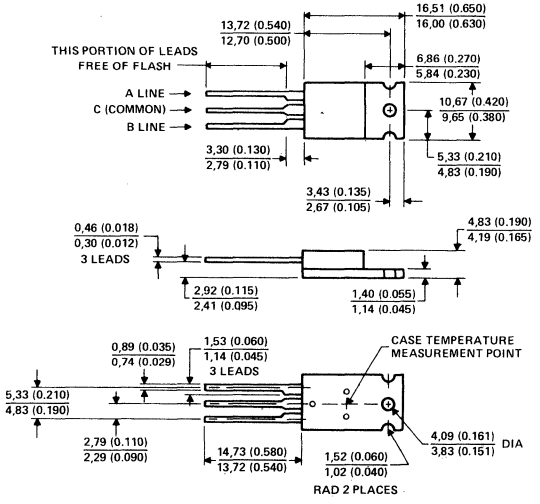
The TISP108A is designed specifically for telephone line card protection against lightning and transients induced by ac lines when A and B are connected to the TIP and RING circuits. These devices consist of three bidirectional suppressor sections that will suppress voltage transients between terminals A and C, B and C, and A and B.

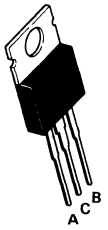
Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover level.

mechanical data

THE COMMON PIN IS IN ELECTRICAL CONTACT WITH THE MOUNTING PAD





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

2 Telecommunications Circuits

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current, 8/20 μs (see Notes 1, 2, and 3)	150 A
Nonrepetitive peak on-state current, t_W = 10 μs, half sine-wave (see Notes 2 and 3)	15 A
Rate of rise of on-state current	100 A/μs
Operating junction temperature	110°C
Operating case temperature range	−10°C to 85°C
Storage temperature range	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 85°C, derate linearly to zero at 110°C case temperature.
3. This value applies when the case temperature is at (or below) 85°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = ±1 mA	±58			V
I_D	Off-state current	V_D = ±50 V			±500	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		100	200	pF

† Polarity may be determined arbitrarily.

electrical characteristics for the A and C or the B and C terminals‡, T_J = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = −1 mA	−58			V
α_{VZ}	Temperature coefficient of reference voltage				0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Note 5			−82	V
$I_{(BO)}$	Breakover current	See Note 5	−0.15		−1.3	A
V_F	Forward voltage	I_F = 5 A, See Note 5			3	V
V_T	On-state voltage	I_T = −5 A, See Note 5		−2.2	−3	V
I_H	Holding current	See Note 5	−150			mA
dv/dt	Critical rate of rise of off-state voltage				−5	kV/μs
I_D	Off-state current	V_D = −50 V			−500	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		250	350	pF

‡ Polarity is determined at terminal A or B with respect to C.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤2%.

thermal characteristics

	PARAMETER	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance	62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

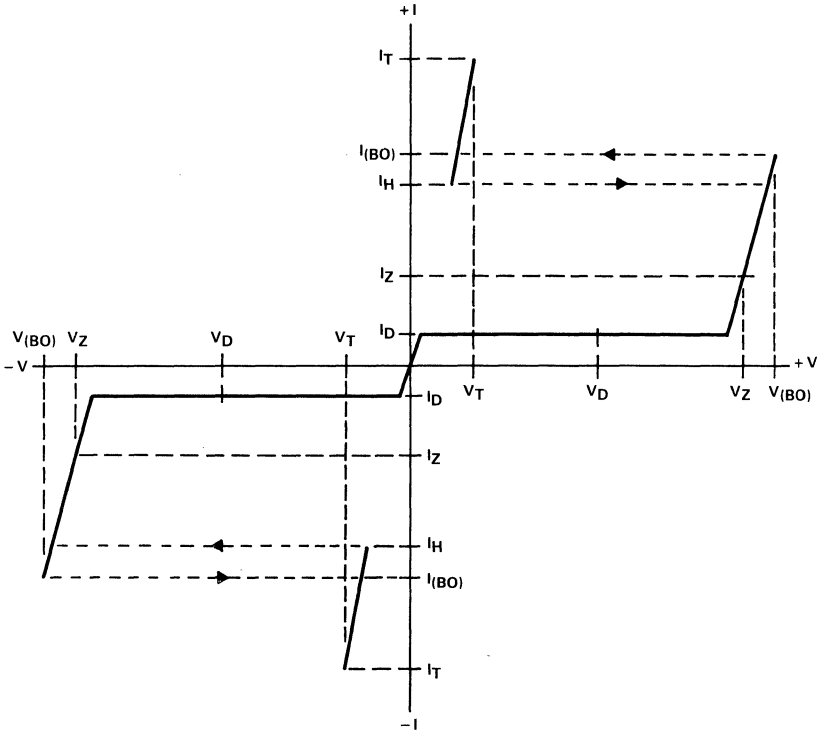

FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR TERMINALS A AND B†

† Polarity may be determined arbitrarily

PARAMETER MEASUREMENT INFORMATION

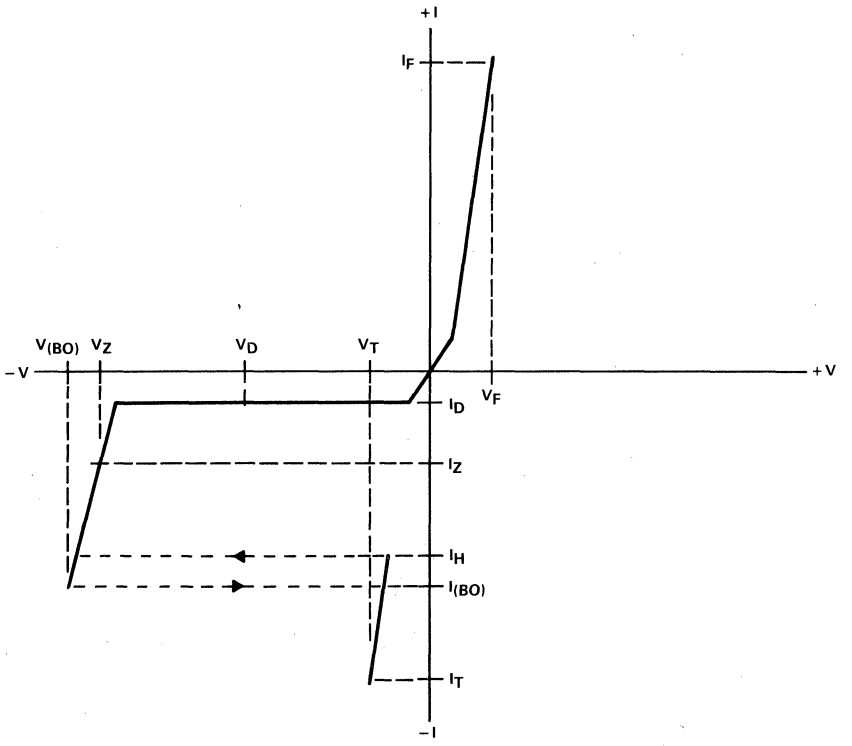

FIGURE 2. VOLTAGE-CURRENT CHARACTERISTICS FOR TERMINALS A AND C OR B AND C‡

‡ Polarity is determined at terminal A or B with respect to C.

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TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

TISP218A
DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSOR

D2929, MARCH 1986

FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common . . . 180 V Max**
- **Surge Current 8/20 μs . . . 150 A**
- **Holding Current . . . 150 mA Min**

description

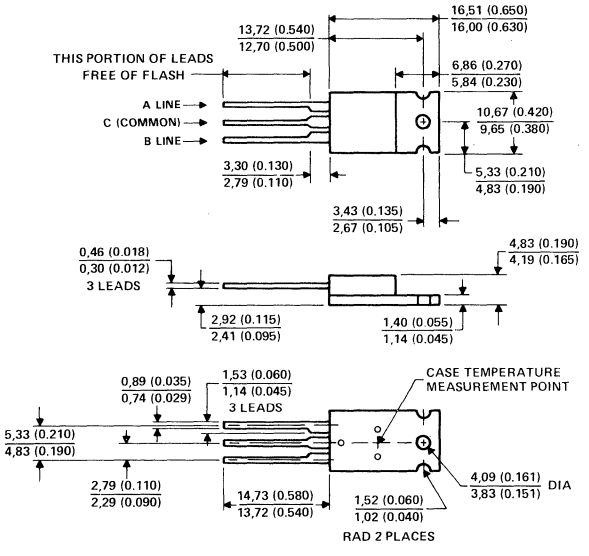
The TISP218A is designed specifically for telephone line card protection against lightning and transients induced by ac lines when A and B are connected to the TIP and RING circuits. These devices consist of two bidirectional suppressor sections connected to a common C terminal. They will suppress voltage transients between terminals A and C, B and C, and A and B.

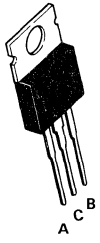
Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

mechanical data

THE COMMON PIN IS IN ELECTRICAL CONTACT WITH THE MOUNTING PAD





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3) . . . . . 150 A
Nonrepetitive peak on-state current, t_W = 10 μs, half sine-wave (see Notes 2 and 3) . . . . . 15 A
Rate of rise of on-state current . . . . . 100 A/μs
Operating junction temperature . . . . . 110°C
Operating case temperature range . . . . . −10°C to 85°C
Storage temperature range . . . . . −40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 85°C, derate linearly to zero at 110°C case temperature.
3. This value applies when the case temperature is at (or below) 85°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = ±1 mA	±120			V
I_D	Off-state current	V_D = ±50 V			±500	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		40	100	pF

electrical characteristics for the A and C or the B and C terminals†, T_J = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = ±1 mA	±120			V
α_{VZ}	Temperature coefficient of reference voltage				0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Note 5			±180	V
$I_{(BO)}$	Breakover current	See Note 5	±0.15		±1.3	A
V_T	On-state voltage	I_T = ±5 A, See Note 5		±2.2	±3	V
I_H	Holding current	See Note 5	±150			mA
dv/dt	Critical rate of rise of off-state voltage				5	kV/μs
I_D	Off-state current	V_D = ±50 V			±500	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		110	200	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.

thermal characteristics

	PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

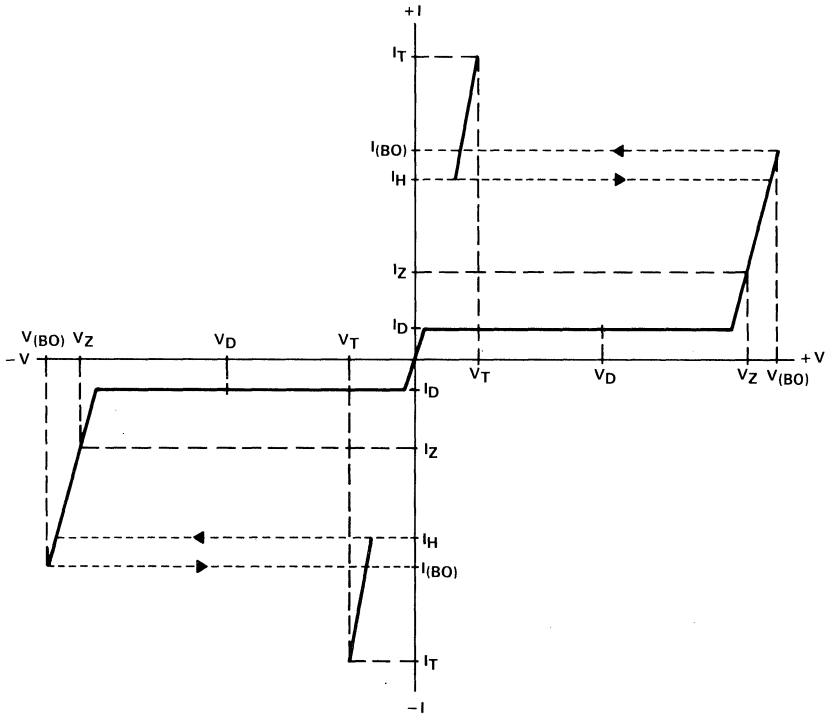

FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR ANY PAIR OF TERMINALS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained.:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

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TISP229A
DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSOR

D2929, MARCH 1986

FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common . . . 290 V Max**
- **Surge Current 8/20 μs . . . 150 A**
- **Holding Current . . . 150 mA Min**

description

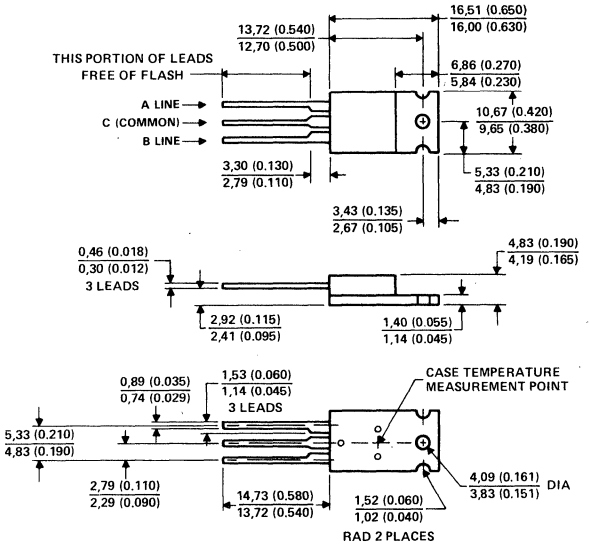
The TISP229A is designed specifically for telephone line card protection against lightning and transients, induced by ac lines when A and B are connected to the TIP and RING circuits. These devices consist of three bidirectional suppressor sections that will suppress voltage transients between terminals A and C, B and C, and A and B.

Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

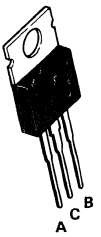
These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

mechanical data

THE COMMON PIN IS IN ELECTRICAL CONTACT WITH THE MOUNTING PAD



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



absolute maximum ratings at 25°C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3)	150 A
Nonrepetitive peak on-state current, t_W = 10 μs, half sine-wave (see Notes 2 and 3)	15 A
Rate of rise of on-state current	100 A/μs
Operating junction temperature	110°C
Operating case temperature range	−10°C to 85°C
Storage temperature range	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	230°C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 85°C, derate linearly to zero at 110°C case temperature.
3. This value applies when the case temperature is at (or below) 85°C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = ±1 mA	±200			V
I_D	Off-state current	V_D = ±50 V			±500	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		40	100	pF

electrical characteristics for the A and C or the B and C terminals†, T_J = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = ±1 mA	±200			V
αV_Z	Temperature coefficient of reference voltage				0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Note 5			±290	V
$I_{(BO)}$	Breakover current	See Note 5	±0.15		±1.3	A
V_T	On-state voltage	I_T = ±5 A, See Note 5		±2.2	±3	V
I_H	Holding current	See Note 5	±150			mA
dv/dt	Critical rate of rise of off-state voltage				5	kV/μs
I_D	Off-state current	V_D = ±50 V			±500	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		110	200	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.

thermal characteristics

	PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

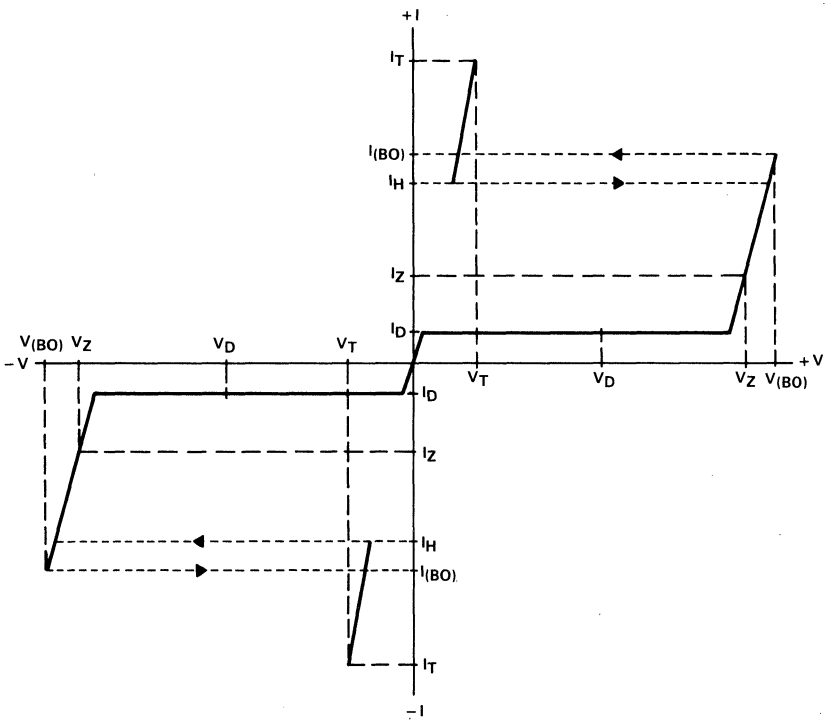

FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR ANY PAIR OF TERMINALS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

The breakover voltage represents the highest level of stress applied to the system being protected by the suppressor. With an increase in ambient temperature, the reference voltage (the level at which transient voltage clipping just begins) increases at typically 0.09%/°C. Breakover current, however, decreases at typically −0.06%/°C, but operating along the reference resistance line reduces its effect. The net result is that the breakover voltage level is only slightly dependent on ambient temperature.

D-C lockup: The suppressor will remain in a crowbar condition as long as the line can supply a short-circuit current greater than the holding current, I_H. To prevent this from happening, the following conditions must be obtained.:

$$\frac{V_{battery}}{R_{line}} < I_H$$

Continuous operation: Line short-circuits to external power supplies can result in overdissipation of the suppressor. Conventional protection techniques such as the use of fuses or PTC thermistors should be used to eliminate or reduce the fault current.

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TISP318A
DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSOR

D2929, MARCH 1986

FOR APPLICATIONS IN TELECOMMUNICATIONS EQUIPMENT

- **Breakover Voltage to Common . . . 180 V Max**
- **Surge Current 8/20 μs . . . 150 A**
- **Holding Current . . . 150 mA Min**

description

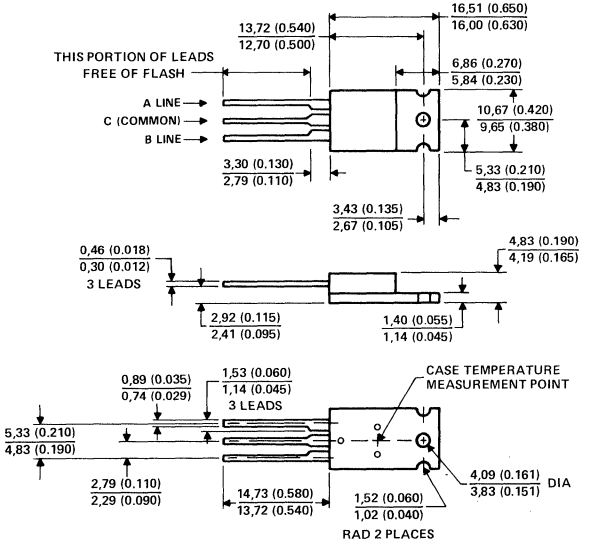
The TISP318A is designed specifically for telephone line card protection against lightning and transients induced by ac lines when A and B are connected to the TIP and RING circuits. These devices consist of two bidirectional suppressor sections connected to a common C terminal. They will suppress voltage transients between terminals A and C, B and C, and A and B.

Transients are initially clipped by zener action until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents dc latchup as the transient subsides.

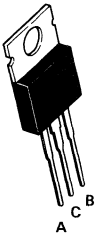
These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and symmetrical breakover control.

mechanical data

THE COMMON PIN IS IN ELECTRICAL CONTACT WITH THE MOUNTING PAD



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



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absolute maximum ratings at 25 °C case temperature (unless otherwise noted)

Nonrepetitive peak on-state pulse current 8/20 μs (see Notes 1, 2, and 3) . . . . . 150 A
Nonrepetitive peak on-state current, t_W = 10 μs, half sine-wave (see Notes 2 and 3) . . . . . 15 A
Rate of rise of on-state current . . . . . 100 A/μs
Operating junction temperature . . . . . 110 °C
Operating case temperature range . . . . . −10 °C to 85 °C
Storage temperature range . . . . . −40 °C to 125 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 230 °C

NOTES: 1. The notation "8/20 μs" refers to a waveshape having a rise time of 8 μs and a duration of 20 μs ending at 50% of the peak value (see ANSI Standard C62.1).
2. Above 85 °C, derate linearly to zero at 110 °C case temperature.
3. This value applies when the case temperature is at (or below) 85 °C. The surge may be repeated after the device has returned to thermal equilibrium.

electrical characteristics for the A and B terminals†, T_J = 25 °C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = ±1 mA	±240			V
I_D	Off-state current	V_D = ±100 V			±500	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		40	100	pF

electrical characteristics for the A and C or the B and C terminals†, T_J = 25 °C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_Z	Reference voltage	I_Z = ±1 mA	±120			V
αV_Z	Temperature coefficient of reference voltage				0.1	%/°C
$V_{(BO)}$	Breakover voltage	See Note 5			±180	V
$I_{(BO)}$	Breakover current	See Note 5	±0.15		±1.3	A
V_T	On-state voltage	I_T = ±5 A, See Note 5		±2.2	±3	V
I_H	Holding current	See Note 5	±150			mA
dv/dt	Critical rate of rise of off-state voltage				5	kV/μs
I_D	Off-state current	V_D = ±50 V			±500	μA
C_{off}	Off-state capacitance	V_D = 0, f = 1 kHz, See Note 4		110	200	pF

†Polarity may be determined arbitrarily.

NOTES: 4. These capacitance measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The third terminal and the mounting tab are connected to the guard terminal of the bridge.
5. These parameters must be measured using pulse techniques, t_W = 100 μs, duty cycle ≤ 2%.

thermal characteristics

	PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			3.5	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance			62.5	°C/W

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PARAMETER MEASUREMENT INFORMATION

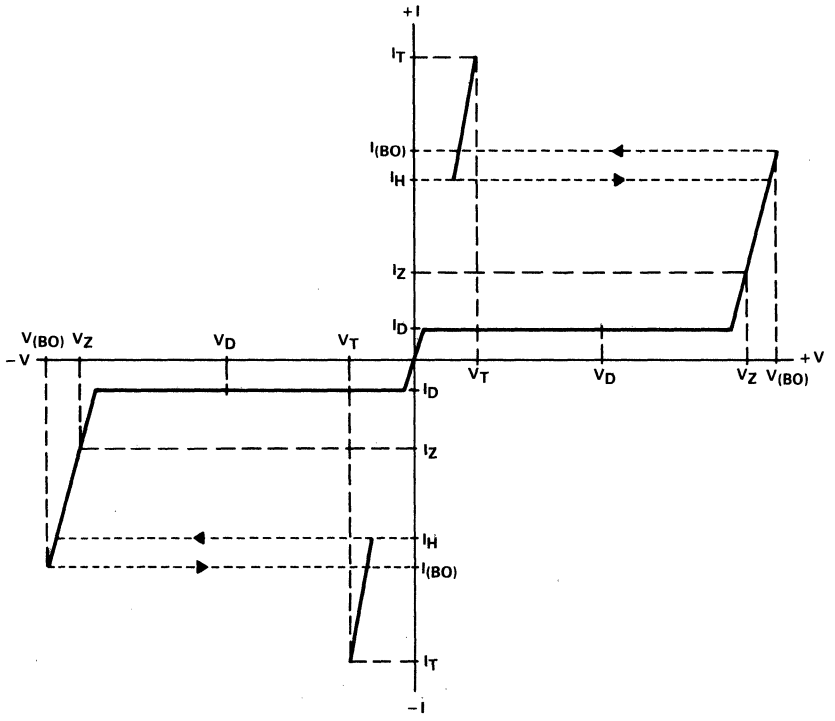

FIGURE 1. VOLTAGE-CURRENT CHARACTERISTICS FOR ANY PAIR OF TERMINALS†

†Polarity may be determined arbitrarily.

TYPICAL APPLICATION DATA

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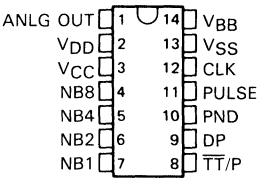
MARCH 1986

PRODUCT SUMMARY

This data is excerpted from the *TMS99531 Modem Products Data Manual*,
 Literature Code MP049

- **Standard N-Channel Silicon Gate Processing Using Switched Capacitor Technology**
- **Identical 4-Bit Addressing for Both Pulse and DTMF Dialing**
- **Interdigit Timing for Both Pulse and DTMF Dialing**
- **No Limit to the Number of Digits That Can Be Sent**
- **Accelerated Pulse Rate for Minimum Checkout or Test Time**
- **Standard 12 Frequency-Pair Combinations, Plus Single Tone Capability**
- **Stable Frequencies and Amplitudes**
- **Less Than 5 Percent Total Harmonic Distortion in Voice Band**
- **High Group Tone Pre-emphasis**
- **TTL-Compatible Input-Output Interface**
- **Subsystem Complement to the TMS99532A FSK Modem**
- **Accepts BCD Inputs for Easy Interface to Microcomputers**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS99531 Pulse and Tone Telephone Dialer is a telecommunications device compatible with the U.S. public switched telephone network. In addition to the usual common telephone usage, the dialer can be used with transaction (point-of-sale and/or credit) terminals, digital voice messages, radio and mobile telephones, and remote or process control. Cost and performance advantages make this dialer highly competitive with other dual-tone and pulse dialers currently available.

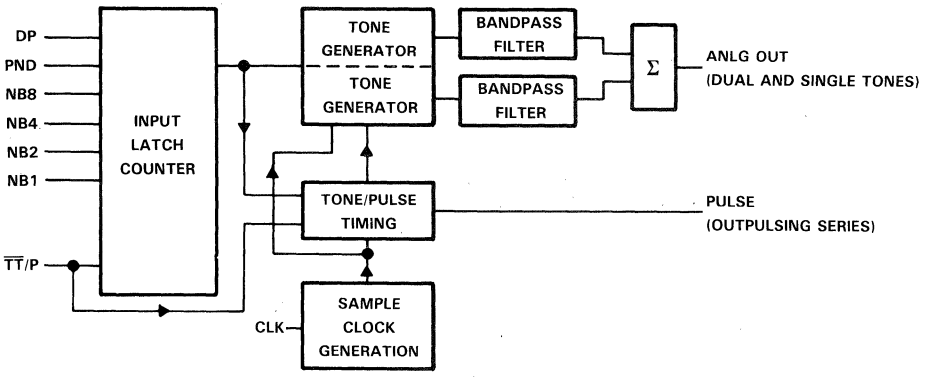
In the pulse mode, the TMS99531 can dial all 10 digits (0-9). In the dual-tone mode, it can dial the 12 dual-tone combinations (0-9, *, #) used by the standard pushbutton telephone keypad. The TMS99531 also generates the appropriate interdigit delays for pulse and tone modes.

A test-enhancement feature in the pulse mode (accelerated pulse rate) reduces the test time needed to verify functionality of all digits. For tone applications, single-tone generation of each of the frequencies is provided.

The TMS99531 is characterized for operation from 0°C to 70°C.

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANLG OUT	1	O	Dual-tone (or single-tone) analog output. Normally capacitively coupled to the EXI input on the TMS99532A modem
CLK	12	I	4.032-MHz master clock input. Received from an external source. Normally connected to OSCOUT of TMS99532A
DP	9	I	Digit present input. A high indicates that a digit is present (and stable) on NB1 through NB8.
NB8	4	I	Digit select input (MSB)
NB4	5	I	Digit select input (third order)
NB2	6	I	Digit select input (second order)
NB1	7	I	Digit select input (LSB)
PND	10	O	Present next digit. When high, the dialer is ready to accept another digit. The DP input must be low for PND to go high.
PULSE	11	O	Pulse dial series. Used with the off-hook relay. A high indicates an off-hook condition. A low indicates an on-hook condition.
$\overline{TT}$/P	8	I	Dual tone or pulse select. When low, the dual-tone mode is selected. When high, the pulse dial mode is selected.
V_{BB}	14		−5-volt nominal supply voltage
V_{CC}	3		5-volt nominal supply voltage
V_{DD}	2		12-volt nominal supply voltage
V_{SS}	13		Ground

functional block diagram



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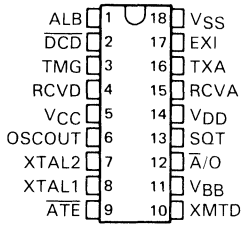
MARCH 1986

PRODUCT SUMMARY

This data is excerpted from the *TMS99532A/TMS99534A Modem Products Data Manual*
 Literature Code: SPPS004.

- **Compatible with Bell Standard 103**
- **On-Chip Filtering, Modulation, and Demodulation**
- **Simplex, Half-Duplex, and Full-Duplex Capability**
- **Originate and Answer Modes**
- **Data Rates from 0 to 300 Bits per Second**
- **Adjustable Carrier Detect Timing**
- **On-Chip Crystal-Controlled Oscillator**
- **Analog Loopback Test Mode**
- **Automatically Disables Bell-Echo Suppressor**
- **TTL-Compatible Digital Interface**
- **N-Channel Silicon Gate Process**
- **Switched-Capacitor Technology**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



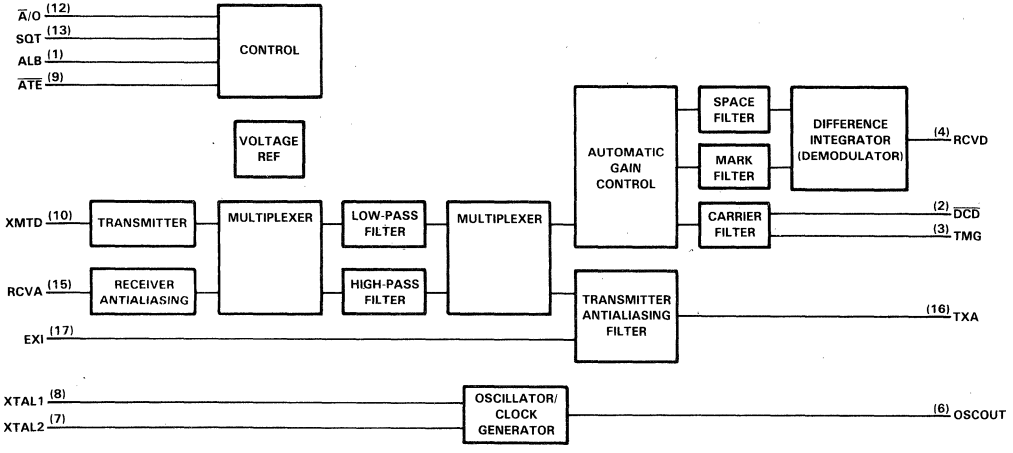
description

The TMS99532A frequency-shift-keyed (FSK) modem is a telecommunication device that transmits and receives binary serial data over the U.S. public switched telephone network using frequency-shift-keyed modulation. The TMS99532A is compatible with the Bell 103 Series data sets and will communicate at up to 300 bits per second. It provides all the necessary modulation, demodulation, and filtering required to implement a serial asynchronous communication link. It is designed for users who are not experts in the telecommunications field. This device is an easily implemented cost-effective alternative to standard discrete modem design. Large-scale integration NMOS technology provides the advantages of small size, low power, and increased reliability. The TMS99532A modem design assures compatibility with a broad installed base of low-speed modems and acoustic couplers. Applications include interactive terminals, desk-top computers, point-of-sale (POS) terminals and credit-verification systems.

The TMS99532A is characterized for operation from 0°C to 70°C.

PIN NAME	PIN NO.	I/O	DESCRIPTION
ALB	1	I	Analog Loopback input. When high, data on the XMTD input will appear on the RCVD output.
$\overline{ATE}$	9	I	When low, the CCITT V.25 answer tone (2100 Hz) is enabled and RCVD is in a high-impedance state.
$\overline{A}$/O	12	I	Answer/Originate input. When high, the originate mode is selected. When low, the answer mode is selected.
$\overline{DCD}$	2	O	Data Carrier Detect output. When low, a valid carrier signal is being detected by the TMS99532A.
EXI	17	I	External input. Any external analog signal to be transmitted is connected to the EXI input. A coupling capacitor is required.
OSCOUT	6	O	Oscillator output. The master clock output frequency is 4.032 MHz.
RCVA	15	I	Received analog carrier signal from the telephone network. A coupling capacitor is required.
RCVD	4	O	Received Digital output. When the $\overline{ATE}$ input is low, RCVD goes to a high-impedance state.
SQT	13	I	Squelch transmitter input. When high, some signals at the TXA output are disabled.
TMG	3		This pin is used to set the carrier detect turn-on and turn-off times.
TXA	16	O	Transmitted Analog output. Transmitted analog carrier output to the telephone network. A coupling capacitor is required.
V_{BB}	11		Supply voltage, −5 volts nominal
V_{CC}	5		Supply voltage, 5 volts nominal
V_{DD}	14		Supply voltage, 12 volts nominal
V_{SS}	18		Ground
XMTD	10	I	Transmitted Digital input. Serial data input line
XTAL1	8	I	Crystal connection for internal oscillator. Can be used for optional external clock input.
XTAL2	7		Crystal connection for internal oscillator

functional block diagram



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Quality and Reliability Assurance

Texas Instruments has improved the quality and reliability of integrated circuits through routine updating of existing specifications and programs as well as advancements in materials, processes, test equipment, and test methods. Since the early sixties, these programs have provided cumulative improvements to increase average outgoing quality (AOQ) and reliability by more than an order of magnitude.

Stringent performance and manufacturing standards are defined prior to product design to assure leadership in the industry. In addition, the following product/process qualifications and evaluations are performed to assure that these standards are met on every device released to the market:

- Verification of manufacturability through testing of bar compatibility with piece parts and automated assembly techniques and equipment
- Proof of process repeatability through definition of minimum acceptable assembly and test yields
- Testing to data sheet limits through test program certification and guard bands between probe, final test, and QRA final acceptance
- Assurance of quality performance through a comprehensive statistical process control program coupled with tight product acceptance standards
- Assessment of device reliability performance through an extensive reliability test and qualification program.

Quality is . . .

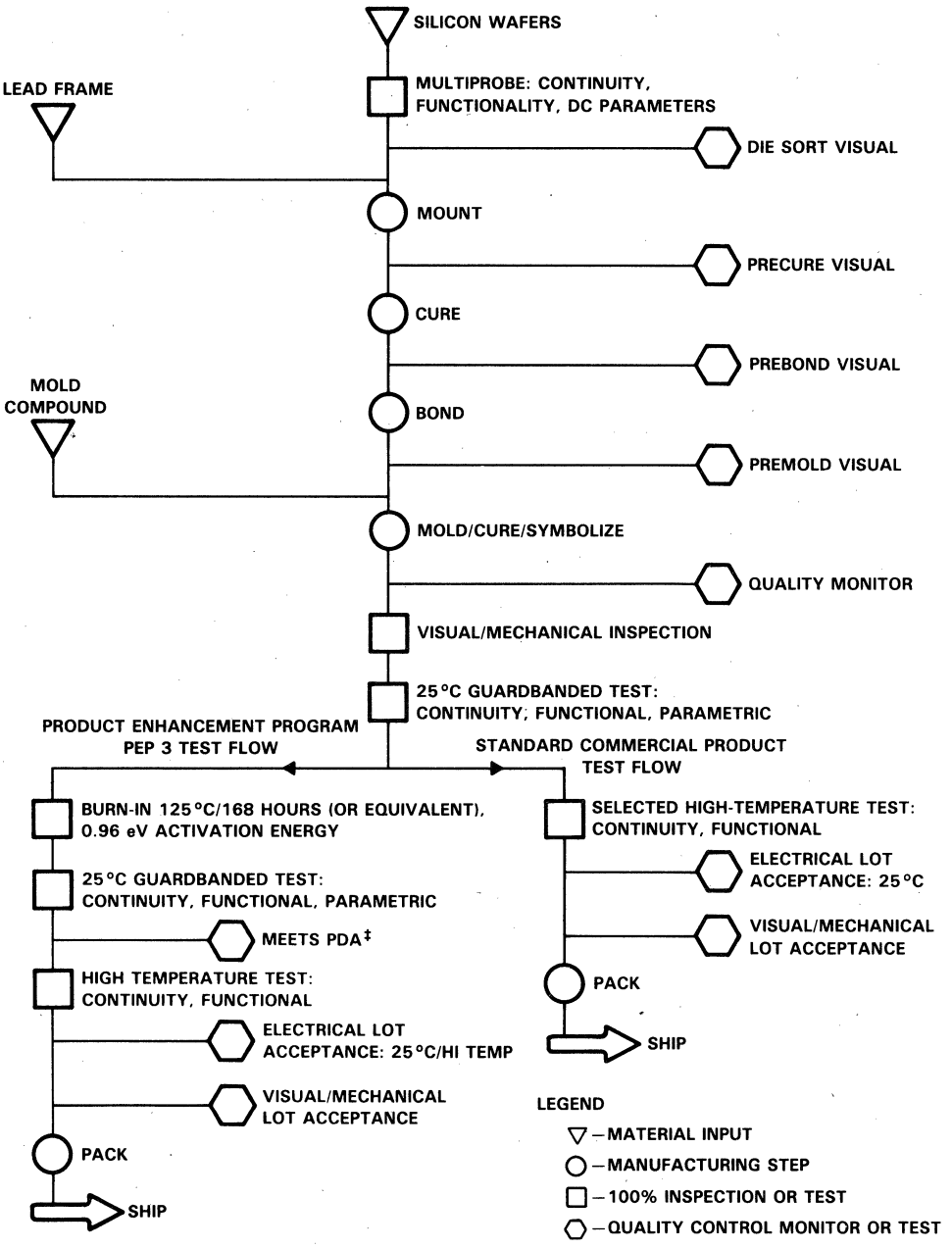
a product's degree of conformance to its specified parameters. It pertains to the probability of defective units existing in a given lot when received by the user. Although zero defects is a goal, the probability of some level of defective units still exists in any lot of mass produced items. The number of defective units received by the user is a function of the average outgoing quality (AOQ) achieved by the supplier.

Reliability is . . .

a measuremnt of how well an initially good product will perform over time to its specified characteristics. Semiconductor failures occur primarily during the early-life phase of operation. A continually diminishing failure rate can be expected until the wear-out phases is eventually reached. System reliability is improved if these potential early-life failures are removed.

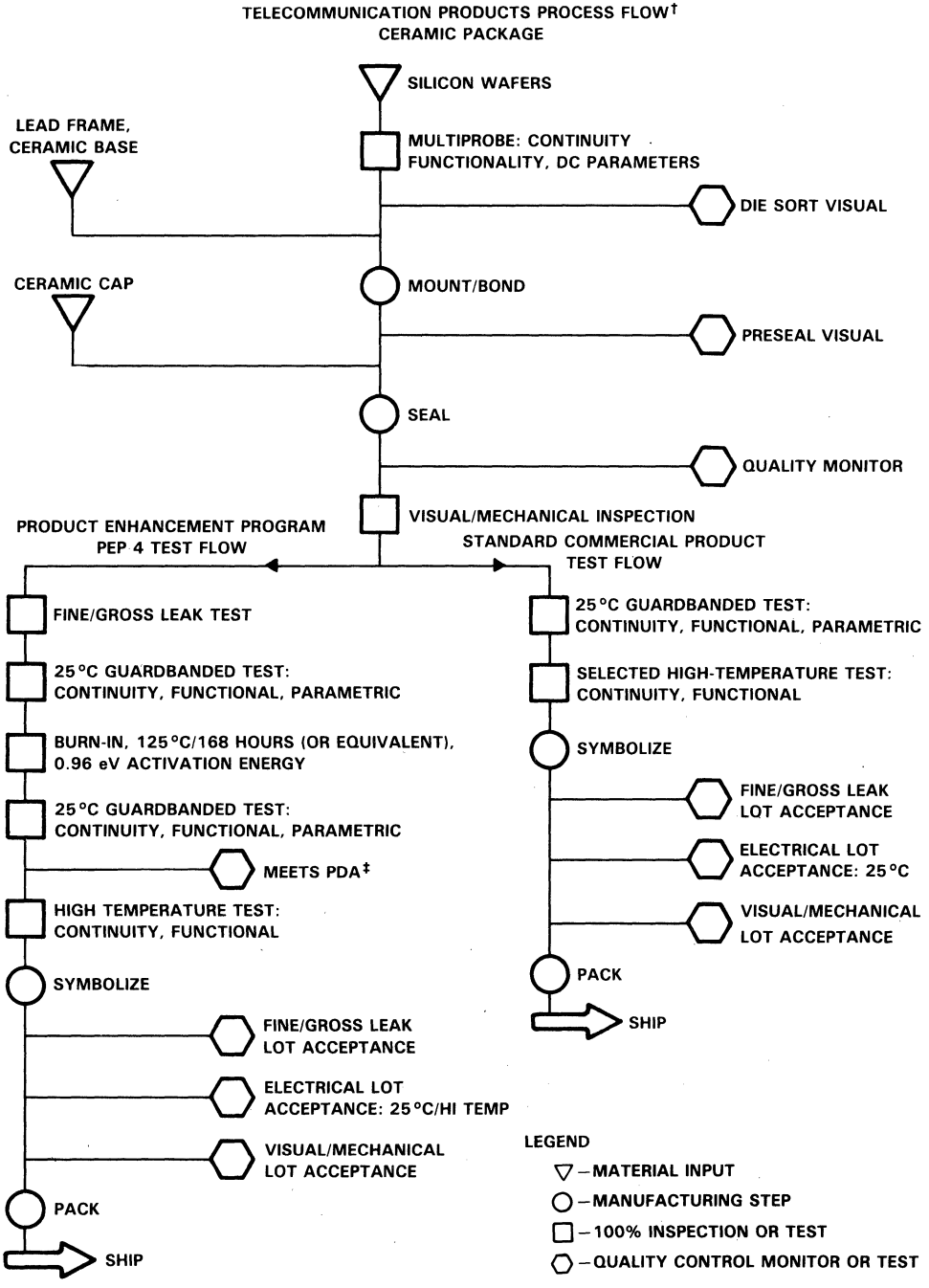
The following process flows for plastic and ceramic packages show the extensive efforts used to maintain high quality and reliability standards for Telecommunication products from Texas Instruments. These flows apply to TCM prefix devices only.

TELECOMMUNICATION PRODUCTS PROCESS FLOW†
PLASTIC PACKAGE



† Applies to TCM prefix devices only.

‡ Post burn-in percent defective (PDA) is 5%. Lots failing this PDA may be burned in one additional time but must pass a PDA of 2.5%.



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‡ Post burn-in percent defective (PDA) is 5%. Lots failing this PDA may be burned in one additional time but must pass a PDA of 2.5%.

FSK Modems

TEXAS INSTRUMENTS

Contents

List of Illustrations

List of Tables

Basic Principles of Modem Operation

A modem is a device that enables two digital electronic systems to communicate over the telephone network. To accomplish this, the digital signals must be converted to analog signals. The short pulses used by digital equipment contain high frequency components that are not supported by the limited bandwidth of telephone networks (300 Hz - 3400 Hz).

There are two major schemes of modulation used in modems for telephone networks. These are Frequency Shift Keying (FSK) and Phase Shift Keying (PSK). In FSK, serial data is modulated so that a "mark" is represented by a sine wave of one frequency, and a "space" is represented by a different frequency. In PSK, transitions in the digital bit stream are represented as shifts in phase angle of a single carrier frequency. The FSK concept is used by the TCM3105. The telephone network is a single-twisted pair of wires, usually 24 or 26 gauge. Two separate paths of communication are required by digital equipment systems in order to communicate with each other. Each system must have transmit and receive capability. This interface is supplied by the modem. Full duplex operation is the simultaneous transmission and reception on a single pair of wires. A two-to-four-wire converter, or hybrid as it is called in the telecommunications industry, is required (see Figure 1). This device removes the transmitted data from the receive path so that transmitted data does not interfere with valid received data.

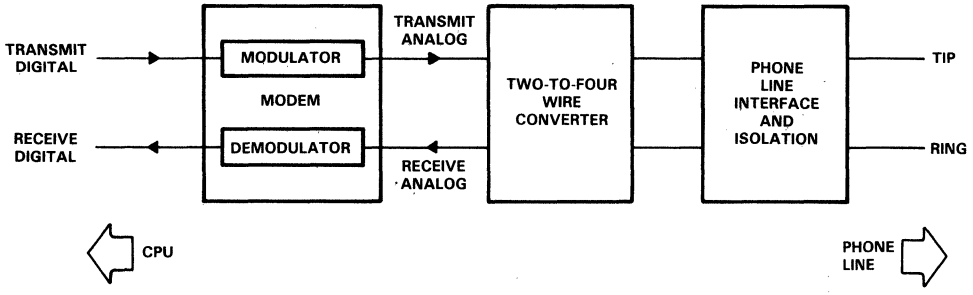


Figure 1. Typical Modem System Configuration

The two-to-four-wire converter requires matching the ranges of telephone network impedances. The impedance of the telephone network varies from line to line due to manufacturing and installation tolerances of the communications hardware. It is difficult to obtain good cancellation in a mass-produced piece of equipment.

Four separate frequencies, two transmit and two receive, are used to properly balance the two-to-four-wire converter. This is to ensure that transmitted and received data do not interfere with each other.

The TCM3105

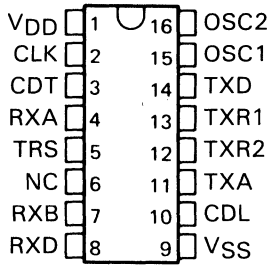
The TCM3105 provides a majority of the functions required of a medium speed FSK modem in a single 16-pin DIP. The device is manufactured using silicon-gate complementary MOS technology. The TCM3105 features single 5-V supply operation and typical power consumption of approximately 40 mW. This makes the device ideally suited for use in battery operated equipment applications, as well as in standard applications. The TCM3105 device pinout is shown in Figure 2. Refer to pin description listed in Table 1 for the function and significance of each pin.

The TCM3105 is characterized for operation from 0°C to 70°C (JL suffix) as well as over the extended free-air temperature range of −40°C to +85°C (JE suffix).

Table 1. Pinout Description

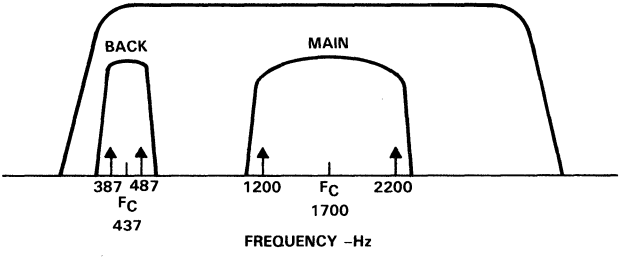
PIN NAME	PIN NO.	I/O	DESCRIPTION
CDL	10	I	Carrier Detect Level—Sets the threshold level for the carrier detect decision. Refer to Description of the Carrier Detect Adjustment paragraph.
CDT	3	O	Carrier Detect — A high logic level output indicates the presence of a carrier at the RXA pin.
CLK	2	O	Clock — Continuous output clock signal at 16 times the highest selected transmit or receive baud rate.
OSC1 OSC2	15 16		Oscillator 1 and 2 — Input connections for external 4.4336 MHz crystal. See Table 2 for list of crystal manufacturers. If an external clock input is provided, then the OSC1 pin is left open and the clock is connected to the OSC2 pin.
RXA	4	I	Receive Analog — This input is referenced to an internal voltage and must be ac coupled.
RXB	7	I	Receive Bias Adjust — This input sets the threshold level of the slicer that allows the bias distortion on the RXD pin to be minimized. Refer to Description of the Receive Bias Adjustment paragraph.
RXD	8	O	Receive Digital Output — Outputs the demodulated receive data in positive logic, i.e., a mark is indicated by a high level and a space is indicated by a low level. The RXD output pin will remain high if there is no analog input on the RXA pin.
TRS	5	I	Transmit/Receive Standard Select Input — This pin along with TXR1 and TXR2 select the standard and mode to be used. See Table 1.
TXD	14	I	Transmit Digital — Digital input to the modulator in positive logic, i.e., a mark is indicated by a high level and a space is indicated by a low level. The data can be accepted at any rate from zero up to the selected baud rate and may be totally asynchronous.
TXR1 TXR2	13 12	I I	Transmit Rate 1 and 2 — These signals along with TRS set the standard and mode to be used. See Table 1.
V_{DD}	1		Positive supply voltage — 5 volts nominal.

J DUAL-IN-LINE PACKAGE
(TOP VIEW)

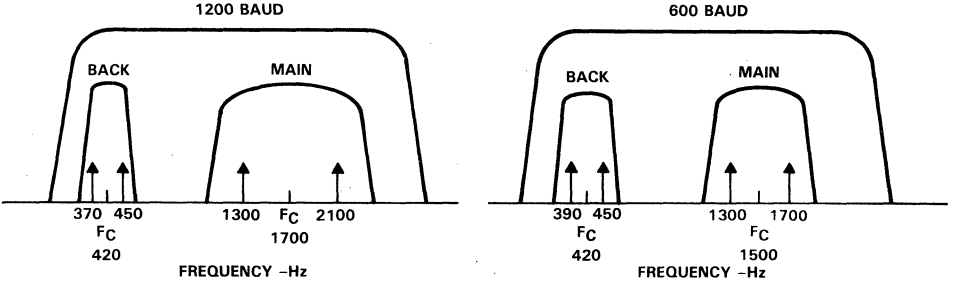


NC—No internal connection

Figure 2. TCM3105 Pinout



(a) Bell 202 Channel Assignments



(b) CCITT V.23 Channel Assignments

Figure 3. Bell 202 & CCITT V.23 Channel Assignments

Modes of Operation of the TCM3105

The TCM3105 is an FSK type modem that is designed to implement the Bell 202 and CCITT V.23 Standards (see Figure 3), which define mark and space frequencies, and the maximum data rate that can be transmitted for a given mark/space pair.

The TCM3105 can be placed into a given mode of operation by applying the proper signals to the TRS (Transmit/Receive Status) and the TXR1 and TXR2 (Transmit Rates 1 and 2) input pins. The various modes of operation for the modems are summarized in Table 2. The CLK signal pin operates at a clock frequency of 16 times that of the selected receive or transmit bit rate, whichever is higher.

Table 2. TCM3105 Modes of Operation

Standard	TRS	TXR1	TXR2	Transmit Bit Rate (Bit/s)	Receive Bit Rate (Bit/s)	Transmit Freq (Hz)	Receive Freq (Hz)	Clock (kHz)
CCITT V.23	0	0	0	1200	1200	M 1300 S 2100	M 1300 S 2100	19.11
	1	0	0	1200	75	M 1300 S 2100	M 390 S 450	19.11
	0	0	1	600	75	M 1300 S 1700	M 390 S 450	9.56
	1	0	1	600	600	M 1300 S 1700	M 1300 S 1700	9.56
	0	1	0	75	1200	M 390 S 450	M 1300 S 2100	19.11
	1	1	0	75	600	M 390 S 450	M 1300 S 1700	9.56
	0	1	1	75	75	M 390 S 450	M 390 S 450	1.19
BELL 202	$\overline{CLK}$	0	0	1200	1200	M 1200 S 2200	M 1200 S 2200	19.11
	$\overline{CLK}$/8	0	1	1200	150	M 1200 S 2200	M 387 S 487	19.11
	$\overline{CLK}$/8	0	1	1200	5	M 1200 S 2200	M 387 S 0	19.11
	CLK	1	0	150	1200	M 387 S 487	M 1200 S 2200	19.11
	CLK	1	1	150	150	M 387 S 487	M 387 S 487	2.39
	*	1	*	5	1200	M 387 S 0	M 1200 S 2200	19.11
	1	1	1	Transmit Disabled	1200	Transmit Disabled	M 1200 S 2200	19.11

*In this mode, the modulation is controlled by the TRS and TXR2 inputs, TXD is set to 1.

If TRS = CLK & TXR2 = 0, then TXA = 387 Hz
If TRS = 1 & TXR2 = 1, then TXA = 0 Hz

Architectural Description of the TCM3105

The modem has four main functional blocks: a transmitter, a receiver, a carrier detector, and timing and control (see Figure 4).

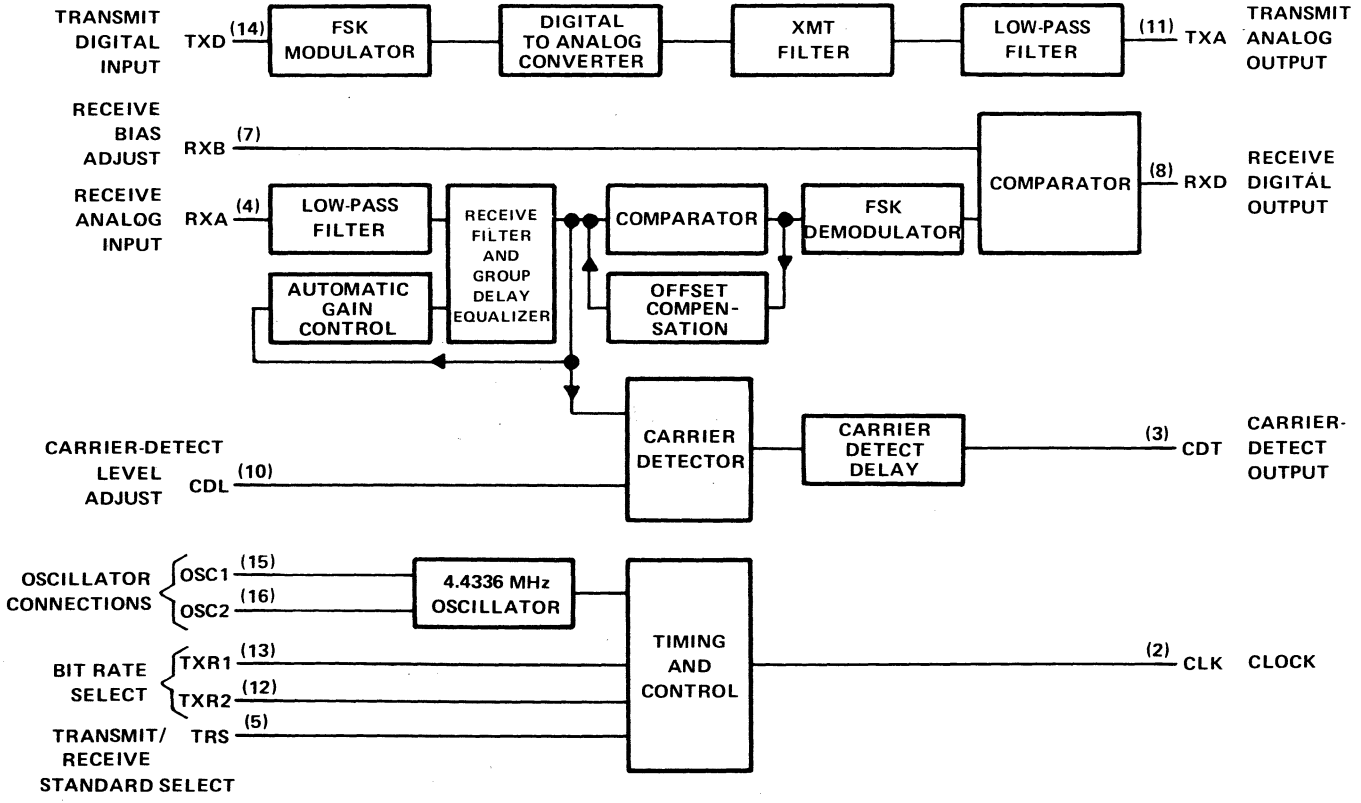


Figure 4. TCM3105 Functional Block Diagram

Transmitter

The transmitter consists of a phase-coherent FSK modulator with a transmit filter and transmit amplifier. The modulator is a programmable frequency synthesizer that obtains the required output frequencies for the modem by dividing the 4.4336 MHz master clock. The division ratio is set by the states of the TXD (Transmit Digital), TXR1, TXR2 and TRS inputs (see Table 2). The transmit filter consists of a switched-capacitor filter stage and a continuous-time filter stage. The switched-capacitor filter samples at a rate dependent upon the transmit frequency selected. This arrangement offers the optimum rejection of out-of-band terms, regardless of the transmit frequency. The continuous-time filter is a second-order Bessel function filter that rejects the clock feedthrough from the switched capacitor filter. The analog output (TXA) pin of the modem is dc biased at approximately 50% of the supply voltage and should be coupled to the two-to-four-wire converter. The overall transmit gain is adjustable within the two-to-four-wire converter.

Receiver

The receiver section consists of an antialiasing prefilter, receive amplifier, receive filter, compromise line equalizer, limiter, demodulator, post demodulator filter, and slicer.

The antialiasing prefilter is a continuous-time low-pass filter that prevents aliasing of high frequency components and sets the band limits of the input signal.

The receive amplifier is part of the receive filter. The receive filter is an elliptic switched-capacitor design, composed of three sections. The first section is a filter that has a high discrimination against the transmit frequencies. The second section is a bandpass filter that includes an automatic gain control function to regulate the amplitude of the signal to the slicer. The last stage is a low-pass filter that attenuates high frequency interference. Overall, the receive filter attenuates broadband interference and removes out-of-band energy that would interfere with demodulation.

The compromise line equalizer is a switched-capacitor equalizer that compensates for the group delay distortion of the receive filter and telephone network. The output of the equalizer is converted to a square wave by a hard limiter.

The demodulator is a conventional monostable multivibrator configured to trigger on the rising and falling edges of the limiter output. The output of the demodulator is a train of fixed-length pulses at a frequency equal to twice that of the received analog signal. Thus, the dc component of this signal is proportional to the frequency of the received signal.

The post demodulator filter is a switched-capacitor low-pass filter that extracts the dc component from the output of the demodulator.

The final stage of the receiver is a slicer that has an externally adjusted reference voltage applied to the RXB (Receive Bias) pin. The RXB reference voltage is necessary to compensate for offsets introduced in the switched-capacitor circuitry. The output of the slicer is the RXD (Receive Digital) pin. The RXB reference voltage need not be readjusted when changing modes of operation, as the modem compensates internally.

Carrier Detector

The carrier detector section consists of an in-band energy detector and a digital delay. The energy detector measures the total energy level at the output of the receive filter and compares this level to a bias level that is set at the CDL (Carrier Detect Level) output pin. The CDT (Carrier Detect) pin is a logic high in the presence of a carrier.

A degree of protection against false output, due to brief signal dropouts, is present. The energy detector is buffered by a short time delay qualifier before the carrier detect signal is sent through to the CDT pin. In addition, the detector exhibits approximately 4 dB of hysteresis to prevent output oscillation.

Timing and Control

The timing is controlled by an external 4.4336 MHz crystal oscillator. Refer to Table 3 for a list of suggested crystal manufacturers. From this master frequency, the timing section generates all the clock control signals and supplies the CLK output signal.

Table 3. 4.4336 MHz Crystal Manufacturers

Manufacturer	CL	Tolerance	Comments
Midland-Ross PH. 414-763-3591	20 pF	±0.005% @ 25°C	Stock Number C 1721N Part Number MPC 18 Requires a 27 pF capacitor from each leg to ground
CTS Knights PH. 815-786-8411	20 pF	±0.005%	Part Number R 1335-5BA4433619 Requires a 27 pF capacitor from each leg to ground
Erie Frequency Control PH. 717-249-2232	30 pF	±0.005%	Part Number L 01-0096-004433618 Requires a 50 pF capacitor from each leg to ground
Seiko Instruments PH. 213-530-8777	15 pF	±0.005%	No Part Number Available Requires a 15 pF capacitor from each leg to ground

Description of the Interface Line

FCC REGISTRATION

The Federal Communications Commission (FCC) has imposed certain restrictions on terminal equipment, including modems, that is connected to the telephone network. FCC Part 68 documents these requirements, which include the following limitations: leakage current, hazardous voltage, signal power, and on-hook impedance. Any device connected to the telephone network must conform to these requirements and be assigned an FCC registration number. The primary interest to modem designers is the hazardous voltage requirements and leakage current limitations. The most practical way to meet the FCC requirements is to electrically isolate the modem from the telephone network with a transformer. This is the most widely accepted method for interfacing direct-connect modems to the telephone network.

Preassembled direct connect devices that perform the modem-to-telephone network interface are available. These devices have typically been assigned an FCC registration number and they include many features such as line powering, ring detection and regulation of loop current. One manufacturer of such products is Cermetek Microelectronics.

FCC registration is not required when the modem is acoustically coupled to the telephone network through a telephone handset. However, this method presents serious drawbacks because telephone sets have very different frequency responses, which make high performance acoustically-coupled modems difficult to design.

TWO-TO-FOUR WIRE CONVERTER OPERATION

The two-to-four-wire converter is part of a typical telephone network interface (see Figure 5). This circuit is necessary to interface the two separate digital channels (transmit and receive) to the single-pair telephone network. A simplified two-to-four-wire converter is shown in Figure 6. This is one of several possible solutions.

To understand how the converter operates, the signal is traced from the transmit input to the receive output. A signal entering the transmit node is buffered by U1A and the output signal is placed across an effective load of $Z_T + Z_L$ in parallel with $Z_T' + Z_L'$. The signal across Z_L is then placed on the telephone network via a transformer. A signal being received from the telephone network is buffered by U1B and placed at the receive node. To reduce the amount of the transmit signal that appears at the receive node, U1B is used in the differential mode to cancel two transmit signals that are 180 degrees out of phase with one another. The two transmit signals appearing at U1B must be of comparable levels. By correctly selecting Z_T' and Z_L', the transmit signals at U1B will be approximately of the same level. Z_T' and Z_L' should be selected to satisfy the following equation:

$$\frac{Z_T}{Z_L} = \frac{Z_T'}{Z_L'}$$

Note: The above equation does not have a restriction on the absolute magnitude of Z_T' and Z_L', only on the ratio of the two. They are therefore scaled versions of the termination and line impedances. This scaling allows small capacitances and large resistances to be incorporated in the network.

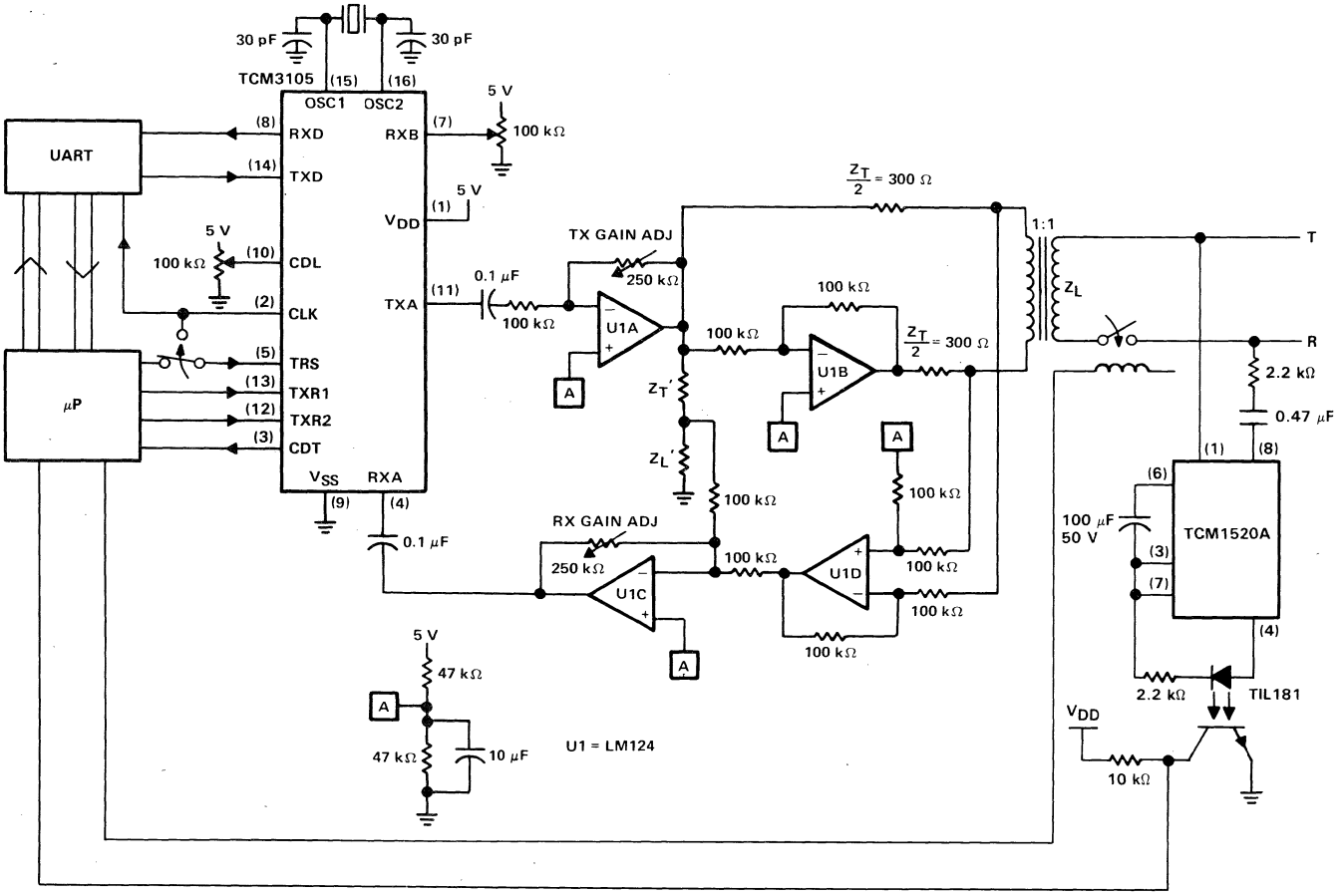


Figure 5. Typical Application Circuit

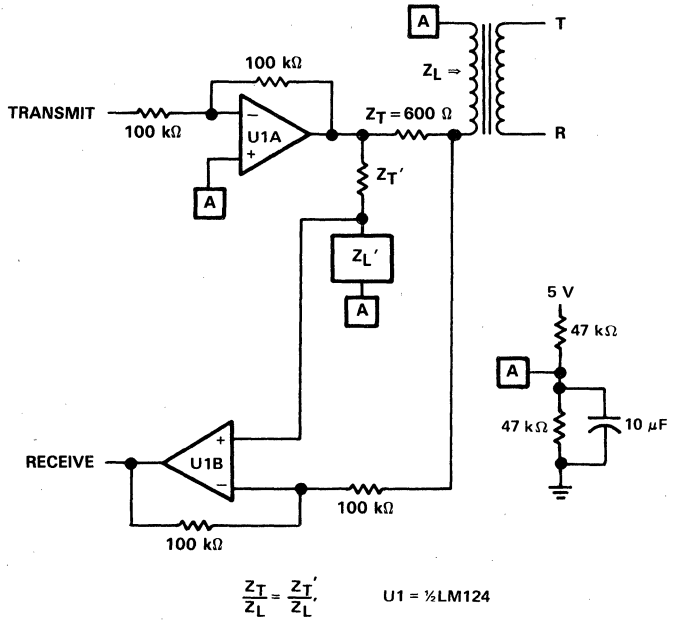


Figure 6. Simplified Two-To-Four Wire Converter

Description of the Carrier Detect Adjustment

The threshold of the carrier detect circuitry in a modem can be adjusted by an external voltage bias at the CDL pin. The minimum detected level is set between the limits of −55 dBm to −35 dBm. A plot of the threshold versus the bias at the CDL pin is shown in Figure 7. The procedure for adjusting CDL is as follows:

1. Apply 4 V to the CDL pin.
2. Place the correct inputs to pins TXR1, TXR2, and TRS so that the TCM3105 is in the desired mode. Refer to Table 2.
3. Apply an ac-coupled, sinusoidal signal to the RXA pin at a frequency between the mark and space frequencies for the mode selected. The amplitude of this signal is set to the lowest signal level that is desired for the modem to detect. A nominal signal level is −44 dBm.
4. The CDT pin should be low.
5. Decrease the voltage at the CDL pin until the voltage at the CDT pin becomes high.

Note: The TCM3105 has a carrier detect delay of 20 ms to 80 ms depending on the receive rate selected. A wait for this delay to time out is required before the CDT pin is monitored.

6. The carrier detect level adjustment is now set.

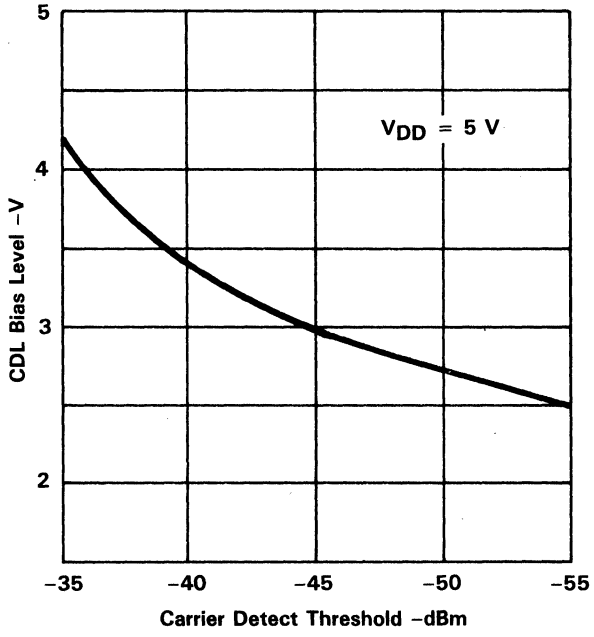


Figure 7. CDL Bias Level Vs Carrier Detect Threshold

Description of the Receive Bias Adjustment

An adjustment of the bias voltage at the RXB pin is required to minimize the bias distortion of the demodulated receive signal at the RXD pin. The bias voltage applied to the RXB pin is used by the slicer to set an internal threshold. A plot of the bias distortion of the RXD signal versus the bias level at the RXB pin is shown in Figure 8. The receive bias can be adjusted by one of two methods.

Method 1

1. Apply the desired signals to pins TXR1, TXR2, and TRS to set the modem in the 1200 baud transmit/1200 baud receive half-duplex mode (for either CCITT V.23 or Bell 202 Standards).
2. Set the modem in the loopback mode (as shown in Figure 9). The attenuator ensures that the analog signal from the TXA pin to the RXB pin is less than 0.78 V peak to peak.
3. Apply a ground to V_{DD} and a 600 Hz square wave to the TXD pin.
4. Monitor the RXD pin with an oscilloscope and adjust the voltage at the RXB pin until the output signal at the RXD pin has a 50% duty cycle.

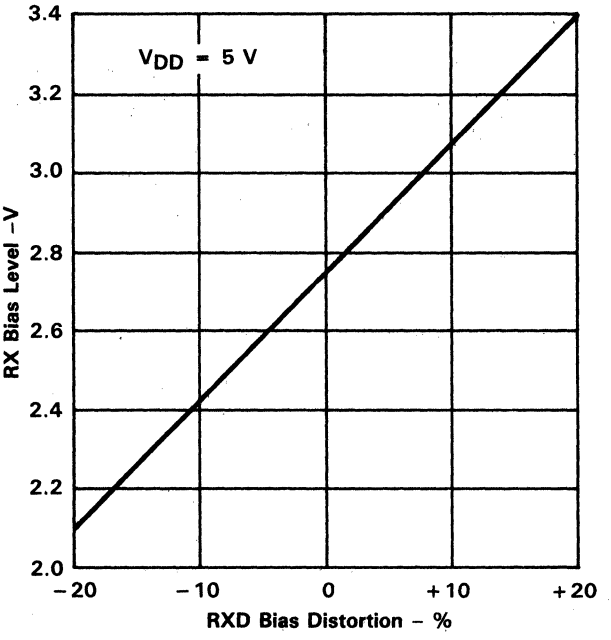


Figure 8. RXB Bias Level Vs RXD Bias Distortion

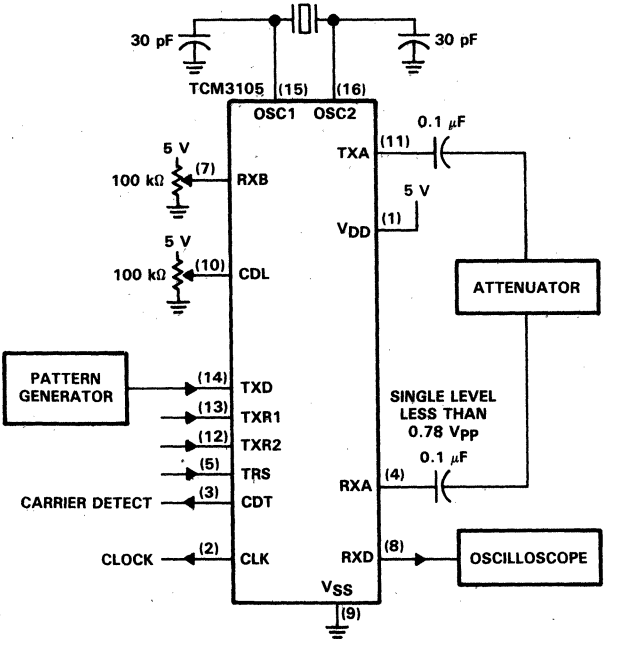


Figure 9. Loopback Circuit Diagram

Method 2

1. Apply the desired signals to pins TXR1, TXR2, and TRS to set the TCM3105 in any proper mode.
2. Apply a signal with an amplitude of less than 0.78 V peak to peak to the RXA pin. The frequency of the input signal should be exactly in the middle of the mark and space frequencies for the mode selected.

   For example, if the Bell 202 1200 baud receive mode is selected, the signal should then have a frequency of 1700 Hz which is the center of the mark frequency of 1200 Hz and the space frequency of 2200 Hz.
3. Apply 3.5 V to the RXB pin, and the RXD pin should exhibit a mark (or high).

   Reduce the voltage at the RXB pin until RXD pin exhibits a low (space), then increase the voltage at the RXB pin until the RXD pin exhibits a high (mark). The bias at the RDX pin is now set.

   Either method will correctly set the bias required for the RXB pin to minimize the bias distortion. Once the adjustment has been set for one particular mode of operation, no further adjustment should be necessary for the remaining modes. The bias distortion should not vary with the baud rate.

Output Jitter Measurement

To measure the demodulated receive output data jitter at the RXD pin, it is necessary to set the modem into a loopback mode (see Figure 9). Apply the proper signals to pins TRS, TXR1, and TXR2 to place the modem in the 1200 baud transmit/1200 baud receive half duplex mode (for either CCITT V.23 or Bell 202). Apply a ground to V_{DD} and a 600 Hz square wave to the TXD pin. With an oscilloscope (set for leading edge triggered) look at the signal at the RXD pin. It should appear as illustrated in Figure 10. The jitter of the output is the difference between T_{max} and T_{min}.

Notes: A. Section VII must be accomplished before the jitter measurement.

B. 4.4336 MHz is from a 4.43361875 MHz crystal (European color burst crystal).

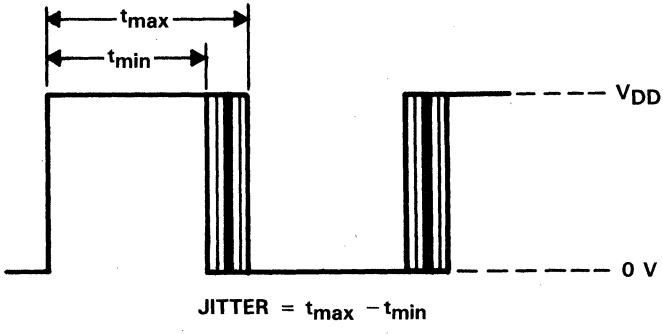


Figure 10. Jitter Timing Diagram

Conclusion

The TCM3105 Modem is a simple solution for many medium-speed data communications systems. On a single chip, there is a FSK modulator/demodulator with all the necessary filtering and equalization to provide full asynchronous operation up to 1200 baud. A complete data communications solution with the TCM3105 can be implemented with a minimal amount of design effort and chip count. The low-power consumption (40 mW typ) and the extended operating temperature range (−40°C to 85°C for the JE suffix) make the TCM3105 ideal for battery operated equipment that must withstand a harsh environment. Refer to the TCM3105 data sheet for detailed specifications.

Applications Report: Subscriber Line Control Circuits

TEXAS INSTRUMENTS

Contents

List of Illustrations

Introduction

In a typical telephone network, the subscriber device (usually a telephone) is connected to a pair of wires called the tip and ring. This pair of wires, known as the subscriber or local loop, connects the subscriber apparatus to the central office (CO) or private branch exchange (PBX). The CO or PBX contains many line cards, each of which interfaces with one or more local loops.

Line-card functions are similar for CO and PBX, with the PBX requirements being less stringent. The functions of line cards are commonly known as the BORSCHT functions. This term is an acronym that stands for **B**attery feed, **O**ver-voltage protection, **R**inging, **S**upervision, **C**odec and filter, **H**ybrid, and **T**est. The arrangement of the BORSCHT functions for a single local loop is illustrated in Figure 1. These functions can be separated into two groups: high voltage and low voltage. In the high-voltage group are battery feed, over-voltage protection, ringing, and test, while the remaining functions fall into the low-voltage group.

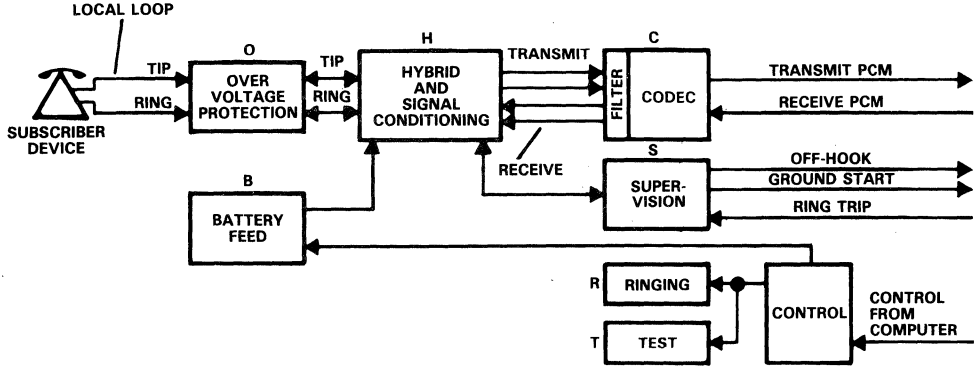


Figure 1. Typical Arrangement of the BORSCHT Functions

In recent years, the trend has been towards increasing the packing density for the CO and PBX. This goal has been realized through the use of LSI circuits to perform one or more of the BORSCHT functions. This in turn has enabled the number of lines handled by each line card to be increased from one to as many as eight. These circuits not only have decreased the space per line ratio for CO components, but also have reduced the cost per line and have improved reliability.

Texas Instruments initial step towards consolidation of the BORSCHT functions was the introduction of the TCM2910 and TCM2911 Codecs and the TCM2912 filter. System integration was further advanced by combining both Codec and filter on the TCM2913 and TCM2914 combos. Today, however, Texas Instruments has further integrated the line card by providing hybrid, supervision, and controlling functions with a family of CMOS LSI circuits called the Subscriber Line Control Circuits (SLCC). Offered are three versions of the SLCC (TCM4204A, TCM4205A, and TCM4207A), each of which is designed for a specific application. (See Functional Description.)

High-Voltage Functions

Battery Feed

The battery-feed function provides the loop with a dc current to power the telephone and is usually supplied by a 48-V battery. For long rural lines, a higher voltage is often used (96 V).

Over-Voltage Protection

Over-voltage protection suppresses high-voltage transients induced by lightning or high-voltage utility lines.

Ringing

This function supplies a ring signal to the subscriber device by switching a ring generator onto the local loop. The signal is typically a 90 V rms sine wave at 20 Hz and is gated for one second on with three seconds off.

Test

Testing involves the use of relays to provide access to the local loop and to the switching circuits in order to test the line.

Low-Voltage Functions

Supervision

When the subscriber apparatus is taken off-hook, the local loop is closed and a dc current is allowed to flow. The supervisor function monitors this loop current to determine when the telephone goes on- or off-hook. It is also used to perform dial-pulse accumulation when rotary-dial telephones are used. Dial pulses are generated by opening and closing the loop in rapid succession.

Codec and Filter

The Codec function is performed when an analog line is interfaced with a digital trunk. Encoding is carried out on the analog signal from the loop, and decoding is performed on the bit stream from the trunk. A voice-band filter (300 Hz to 3500 Hz) is used before encoding and after decoding.

Hybrid

The hybrid function separates the bidirectional voice signals from the two-wire loop into distinct transmit and receive paths. This separation facilitates the use of analog repeater amplifiers or digital processing circuits. The hybrid function is named for the specialized transformer that has traditionally performed this two-wire to four-wire conversion.

Theory of Operation

Signaling

In addition to the supervision signaling previously described, two other types of signaling are used: ring and dial pulse signaling.

Ring Signaling

A ring signal is initiated in the CO or PBX and is used to alert the subscriber to an incoming call. The ring signal is injected onto the local loop by switching a ring generator in series with the battery.

The ring signal in the United States is a sine wave ranging in frequency from 15.3 Hz to 68 Hz, and in amplitude from 40 V rms to 150 V rms. The signal is gated on and off in a particular 'cadence.' A typical ring signal in the U.S. is 90 V rms at 20 Hz gated for one second on and three seconds off.

Dial-Pulse Signaling

Dial pulses are generated by making and breaking the subscriber loop in rapid succession. Figure 2 shows loop current as a function of time during dialing. In the United States, the recommended timing requirements for dial pulses are given by the Electronics Industries Association RS-470 standard. This document specifies a pulse period from 91 to 125 ms, with a percent break between 58 and 64. Here, percent break is defined as follows:

$$[(\text{break duration})/(\text{break duration} + \text{make duration})] \times 100$$

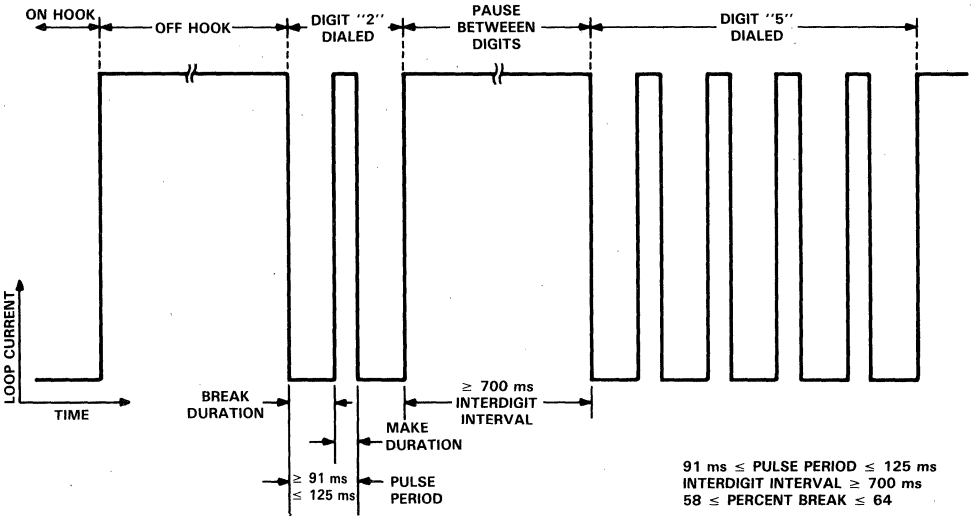


Figure 2. Dial Pulse Timing Diagram

Device Description

The pin functions of TI's three SLCCs are given in Table 1, and the functional block diagram is shown in Figure 3. Each SLCC can be divided conceptually into digital, analog, and supervisor functions.

Digital Functions

The heart of the digital section of the SLCC is a 24-bit data storage unit (DSU). This DSU contains bits of read only and read/write data to provide hook status, relay control, transmit and receive gain control, and line-balance selection.

The bits in the DSU are accessed through a single DATA pin. A low transition on the chip enable input ($\overline{CE}$) causes the DATA pin to change from a high impedance to an active state, and sets the pointer/counter to bit 0. The pointer is advanced by a positive transition on the clock (CLKM) input. The read/write ($R/\overline{W}$) input determines the direction of information flow on the DATA pin. See the TCM4204A data sheet for a detailed timing diagram.

Analog Functions

The analog functions consist of the receive and transmit signal paths, with attenuators, and the hybrid function. The receive and transmit attenuators increase the versatility of the SLCC. The receive path gain is variable from −7.8 dB to +4.8 dB in 0.2-dB increments. The transmit path gain is variable from −12.6 dB to 0.0 dB in 0.2-dB increments.

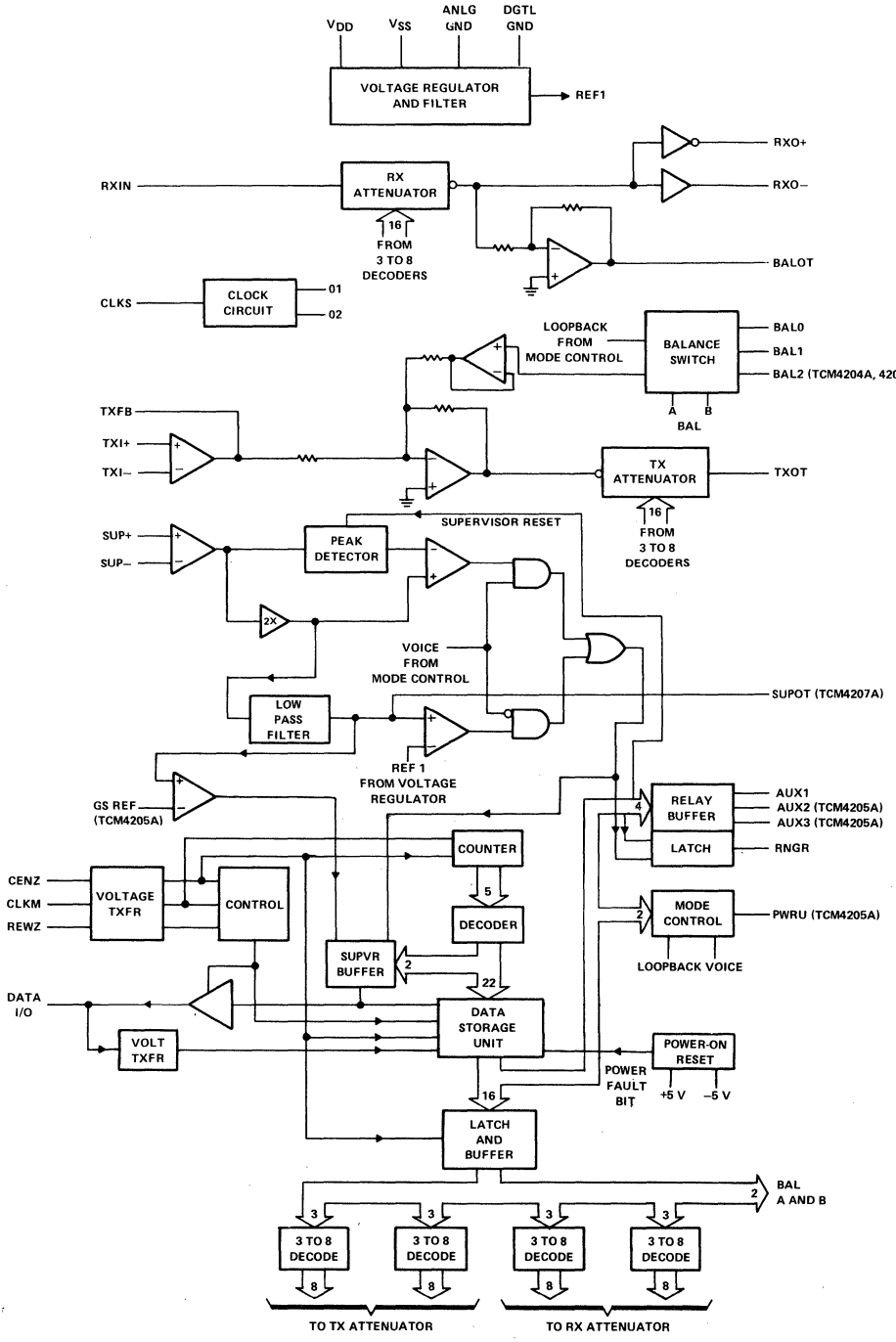


Figure 3. Internal Configuration of the Subscriber Line Control Circuits

Table 1. Pin Functional Description

NAME	PIN			DESCRIPTION
	TCM4204A	TCM4205A	TCM4207A	
ANLG GND	4	4	4	Analog ground
AUX1 AUX2 AUX3	11	11 12 13	11	Latched digital outputs for relay control
BAL0 BAL1 BAL2	19 18 17	23 22 21	19 18	Analog input to balance network selection
BALOT	5	5	5	A buffered form of the RX signal for application to the external balance network
$\overline{CE}$	9	9	9	Chip enable. Activated by a logic low input.
CLKM	7	7	7	Digital clock input that advances the pointer counter of the digital storage unit (DSU) allowing the information in the DSU to be accessed. When R/$\overline{W}$ and $\overline{CE}$ are low, information on the DATA I/O pin is latched into the DSU by the falling edge of CLKM.
CLKS	13	15	13	A continuous clock input (from 1.536 to 2.048 MHz) used for internal logic. This signal is not synchronous with any other signal.
DATA I/O	10	10	10	Digital data input/output. When $\overline{CE}$ is low and R/$\overline{W}$ is high, the DATA I/O pin is in the output mode. When $\overline{CE}$ is low and R/$\overline{W}$ is low, the DATA I/O pin is in the input mode. When $\overline{CE}$ is high, the DATA I/O pin is in the high-impedance state.
DGTL GND	12	14	12	Digital ground
GS REF		20		Analog reference voltage input used for ground start supervision.
PWRU		17		Decoded digital output of Mode Control used to control an external power supply.
RNGR	14	16	14	Latched digital output to control the ring relay. The output turns off (low) when off-hook is detected, but the controller must program the ring bit low to ensure that the output remains low.
RXIN	6	6	6	Analog input to the receive section
RXO+ RXO−	2 3	2 3	2 3	Complementary analog output of the receive amplifier
R/$\overline{W}$	8	8	8	Digital input control for the direction of response of the digital storage unit. A logic high on R/$\overline{W}$ sets the DSU to transmit information. A logic low on R/$\overline{W}$ enables the DSU to receive information.
SUP+ SUP−	15 16	18 19	15 16	Differential analog supervision inputs. Inputs to SUP+ and SUP− are used to detect off-hook status during normal and ringing supervision.
SUPOT			17	Filtered supervisory analog output
TXFB	20	24	20	Feedback out of TX input amplifier
TXI+ TXI−	21 22	25 26	21 22	Analog differential inputs to TX input amplifier
TXOT	23	27	23	Analog output of TX output amplifier
V_{DD}	24	28	24	Supply voltage (5 V ±5%)
V_{SS}	1	1	1	Supply voltage (−5 V ±5%) referenced to ANLG GND

Supervision Functions

Line supervision is performed using differential inputs SUP+ and SUP−. When loop current flows, a voltage appears across the inputs from an external resistor network. The low-pass filter (LPF) shown in Figure 3 is used when off-hook detection is required during ringing. The LPF is a switched-capacitor filter, and its cutoff frequency is determined by the frequency of the input CLKS. Figure 4 shows the filter characteristics as a function of CLKS frequency. The LPF filters out the ac component from the supervision signal to detect a valid off-hook condition during ringing. The output of the LPF is used to set

bit 0 (on/off-hook) of the DSU. By virtue of the CLKS input, the SLCC can be used with any frequency ring generator. With the SLCC in the voice mode of operation, the LPF is ignored. This condition allows dial pulses to pass undistorted to the DSU.

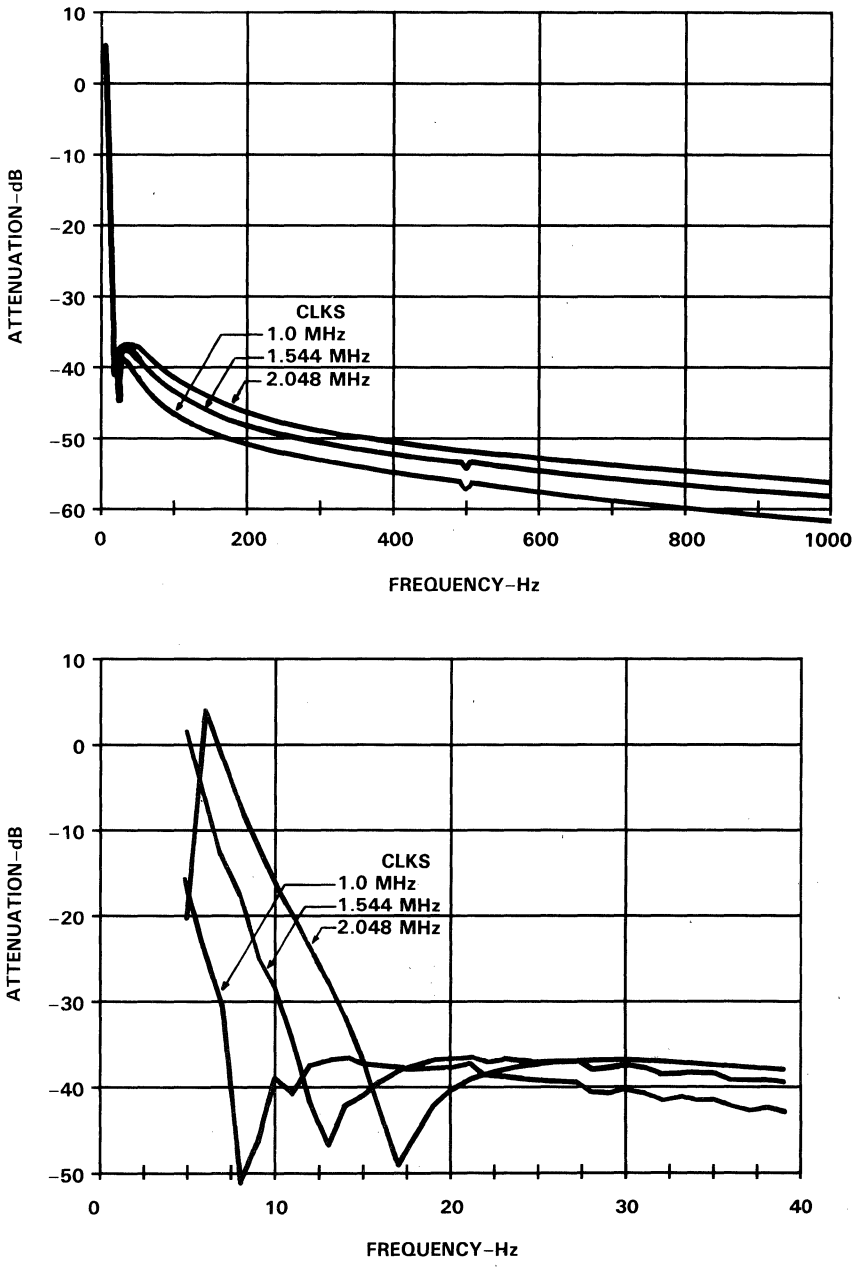


Figure 4. Filter Characteristics as a Function of CLKS Input

Functional Description

The three versions of the SLCC (TCM4204A, TCM4205A, TCM4207A) have some functional differences. Each is designed to accommodate a different type of application, as outlined below.

TCM4204A

The TCM4204A, a 24-pin device, is configured to operate in a standard loop-start CO or PBX environment. It provides a ring relay output, plus one auxiliary output to control the test relay. A provision for three balance networks allows the same card to operate on virtually any length of line through a simple software manipulation.

TCM4205A

The TCM4205A is a 28-pin version of the SLCC and is ideal for ground-start applications. It performs all those functions found in the TCM4204A, with the addition of two extra relay outputs, a PWRU pin used to signal the power supply, and a GS REF ground-start reference input.

TCM4207A

The TCM4207A is identical to the TCM4204A aside from the addition of a supervisor output, which replaces one of the line-balance networks. This supervisor output provides a voltage that is proportional to the supervisor input-voltage. The output is used in driving a flux-cancelling winding in the battery-feed transformer.

System Design

Supervision Circuit

A typical application of the TCM4204A in a loop-start system is shown in Figure 5. In the normal (nonringing) state, the loop current (typically 20 mA to 80 mA) flows through the path defined in Figure 6. The loop current causes an IR drop across each of the 200-Ω resistors, which shifts the voltage levels on the supervision inputs (SUP+ and SUP–). Figure 7 gives SUP+ and SUP– voltages as a function of loop current. When the differential voltage between the two exceeds the threshold, the SLCC responds by setting the hook-status bit in the DSU to a logic high, indicating the off-hook condition.

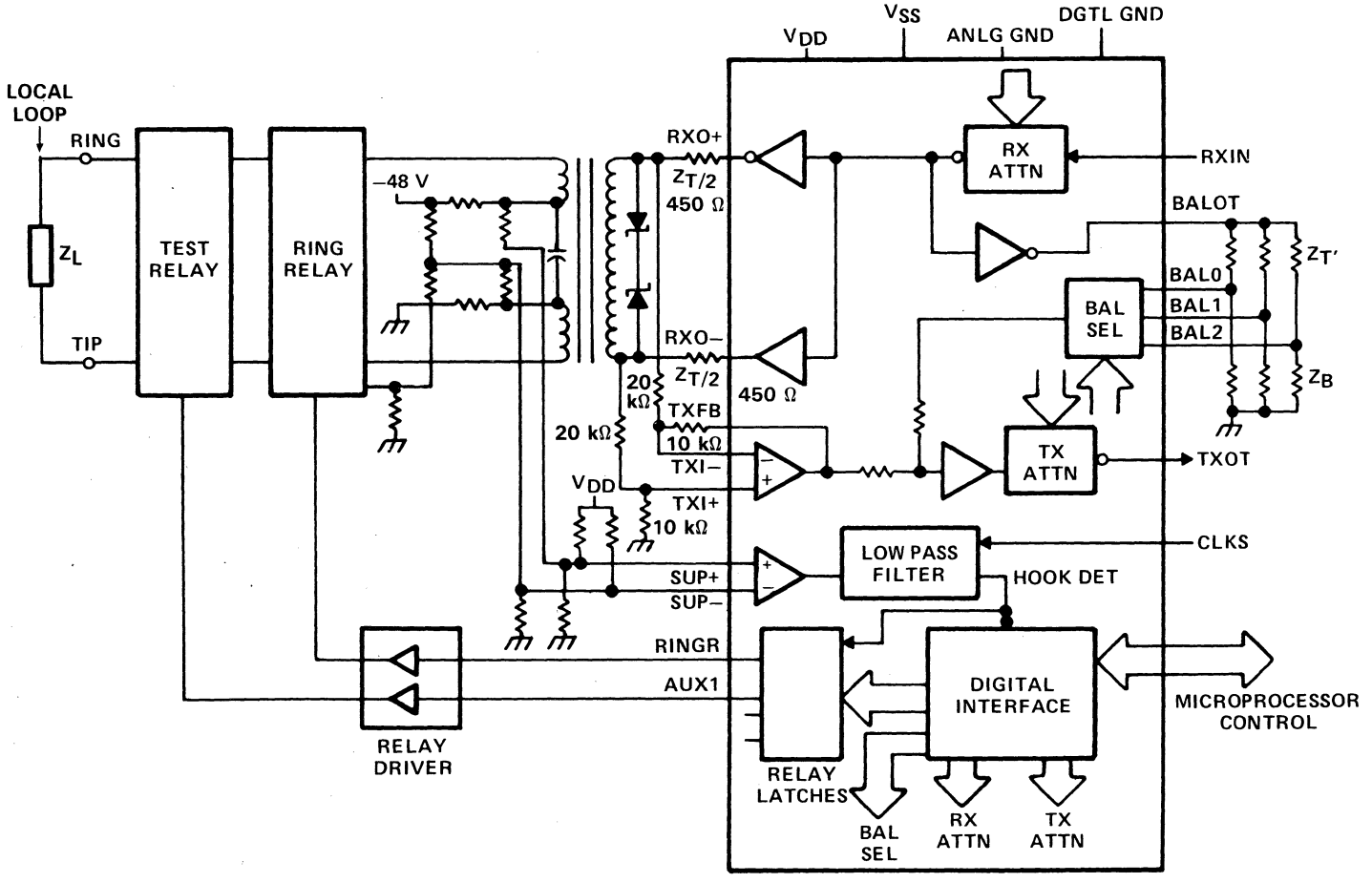


Figure 5. Typical Loop Start Application for the TCM4204A

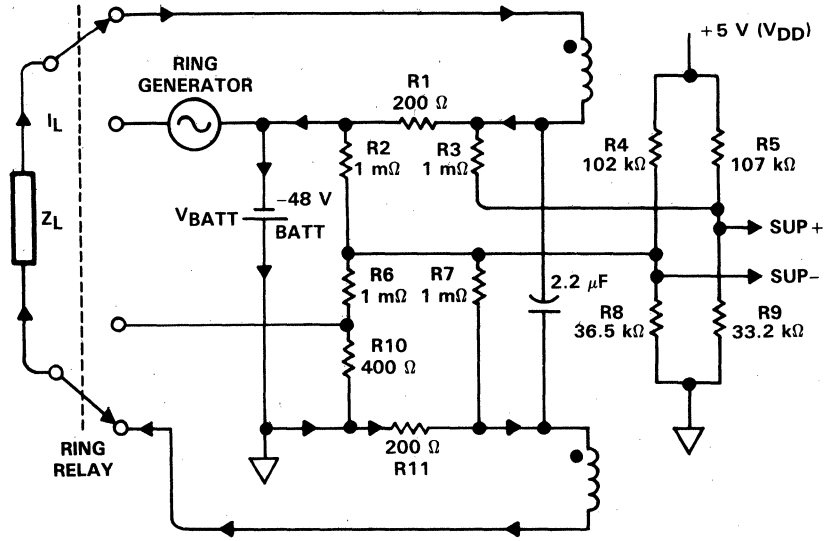


Figure 6. Off-Hook Loop Current Path During Nonringing Condition

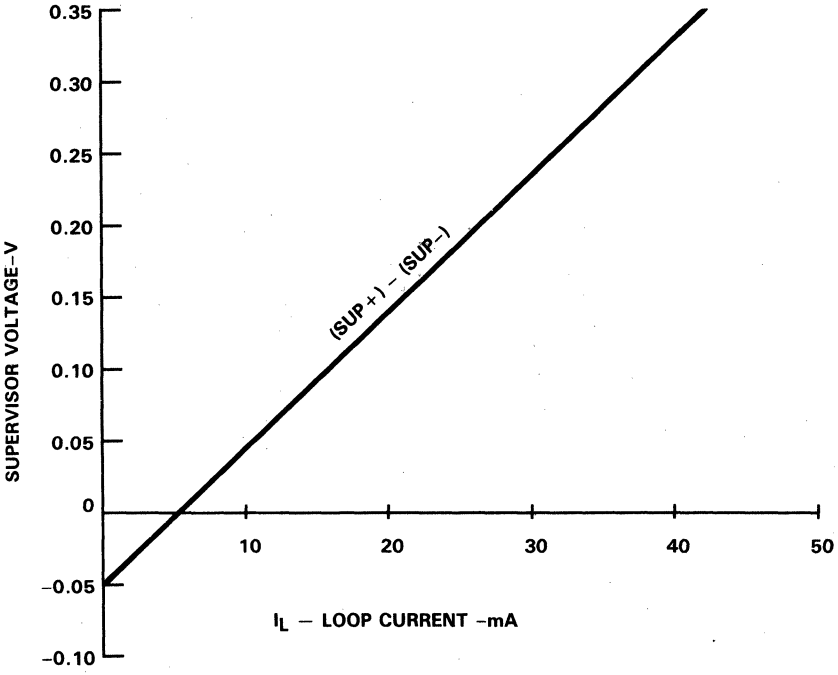


Figure 7. Supervision Voltage vs Loop Current

A detailed diagram of the supervision circuitry of the SLCC is given in Figure 8. The details of supervisor operation are as follows:

1. A differential voltage across the SUP+ and SUP– inputs, referenced positive on SUP+ is required to initiate the off-hook condition (bit 0 high) in the standby or power-down mode.
2. Initial off-hook detection is always done in the standby or power-down mode.
3. The voltage across SUP+ and SUP– required for off-hook detection is 50 mV.
4. For rejection of the ring signal, the supervisor information is filtered with a switched capacitor low-pass filter when not in the voice mode.
5. When the ring bit is set high, an off-hook detection causes the ring relay output to go low; however, the ring bit must be reset to low by the controller before the controller changes the SLCC to the voice mode.
6. The voltage on either SUP input should always be between –2 V and +2.5 V. Outside this range, the supervision circuits become non-linear and the SUP inputs may require significant current. For this reason it is recommended that SUP+ and SUP– both be near 0 V for no-loop current.
7. After initial off-hook detection, the SLCC should always be placed into the voice mode.
8. When the SLCC is placed in the voice mode, on-hook is detected using a peak-detector circuit. The peak-detector samples and stores the peak value of the SUP differential voltage. On-hook is detected when the SUP voltage falls below half the stored voltage. This circuit provides the ability to detect dial pulses and on-hook at the termination of a call.
9. The peak-detector circuit capacitor is discharged to 0 V whenever the SLCC is placed in the ring mode or when the Supervisor reset bit is set to a high. The Supervisor Reset should be used if off-hook is detected during standby mode to eliminate any accumulated charge on the capacitor due to noise.

If the subscriber returns to on-hook status while the Supervisor Reset bit is being used, then the SLCC cannot accurately detect the on-hook condition since, both the SUP voltage and the peak detector are at 0 V. This inability can be prevented by providing a dc bias-voltage in the reverse direction on the SUP+ and SUP– inputs when no loop current is flowing.

During pulse dialing, the loop current is pulsed off and on approximately ten times per second. When the SLCC is in the voice mode (set through the microprocessor interface), the supervisor information from SUP+ and SUP– is routed through a peak detector circuit, bypassing the low-pass filter. The pulses toggle the hook status bit in the DSU as the loop current is pulsed. The controlling microprocessor monitors this bit and counts the dial pulses. Dial-pulse accumulation can be accomplished only in the voice mode, because the low-pass filter will distort the dial pulses.

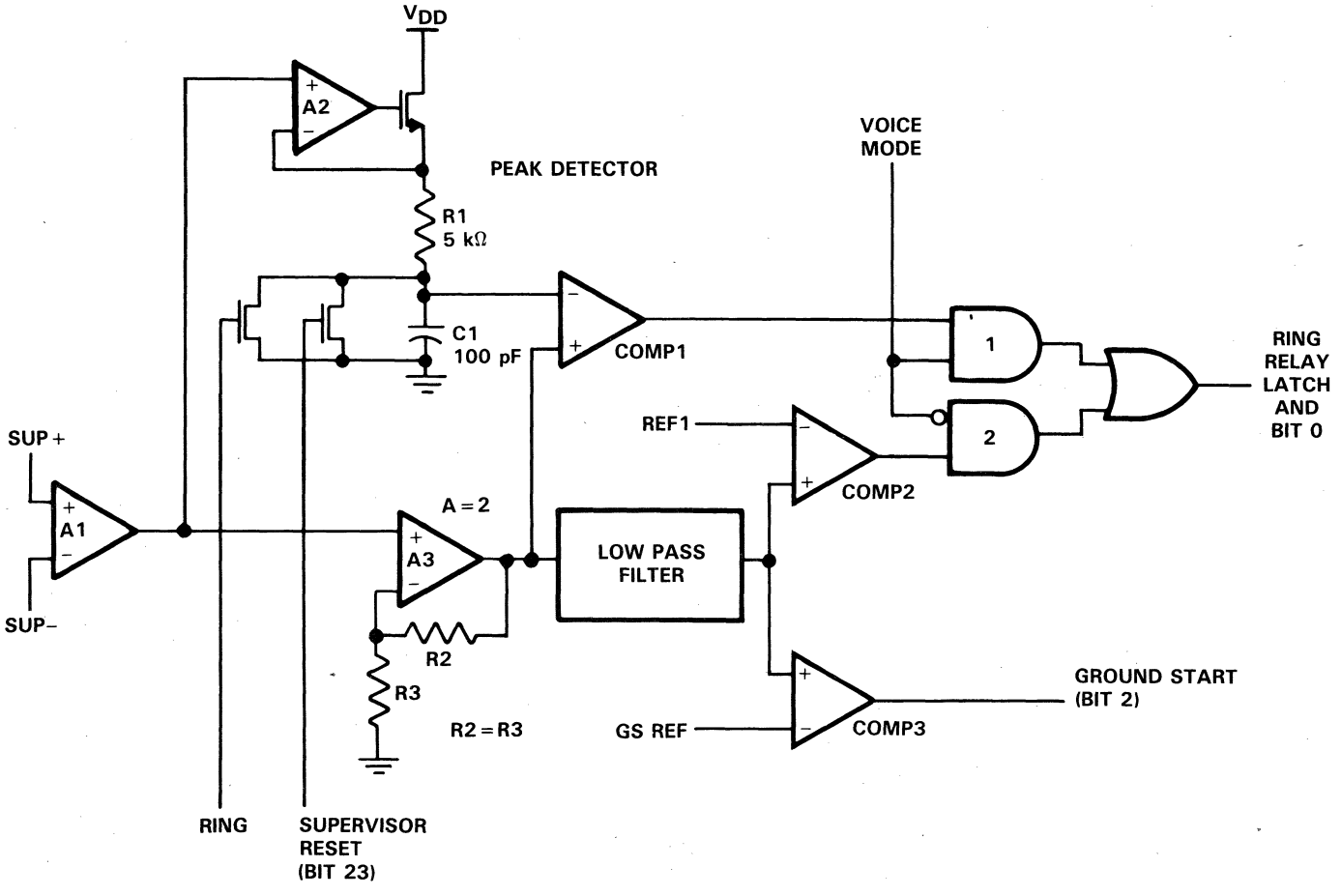


Figure 8. Supervision Circuit Block Diagram

Ring-trip is the supervisor function which involves detecting off-hook during the ringing condition and resetting the ring relay. The SLCC must be in the standby or power-down mode when the ring bit is set to allow the LPF to reject the ring signal from the supervisor information.

When the ring relay is activated, the system is reconfigured as shown in Figure 9. The off-hook dc current path has been traced to illustrate the ring-trip function. When the telephone goes off-hook in the ringing condition, the IR drop across the 400-Ω resistor causes the potential at the SUP– input to drop below that at the SUP+ input. The SLCC automatically turns off the ring relay output when the hook status bit has been set. The controller must then reset the ring bit as soon as an off-hook condition has been determined.

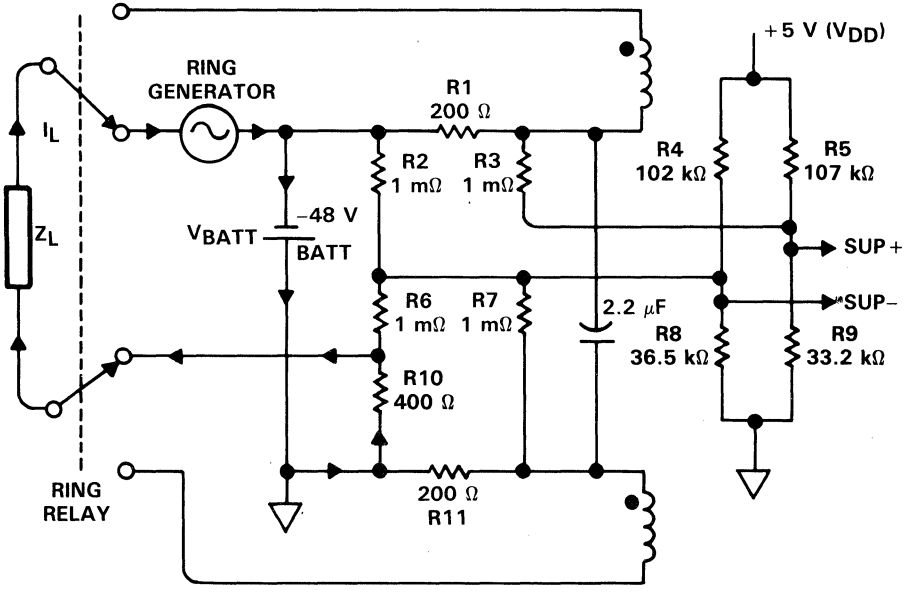


Figure 9. Off-Hook Loop Current Path During Ringing Condition

The Supervision circuit shown in detail on Figure 6 and Figure 8 was designed to the following criteria:

1. A 10-mA loop current represents off-hook.
2. A –50-mV reverse bias exists when the loop current equals 0.

The simplified loop equations are as follows:

1. Nonringing condition:

$$V_{SUP+} = [V_{DD}(1/R5) + V_{BATT}(1/R3) + I1(R1)(1/R3)]/[1/R5) + (1/R9) + (1/R3)]$$

$$V_{SUP-} = [V_{DD}(1/R4) + V_{BATT}(1/R2) - Il(R11)(1/R7)]/[(1/R2) + (1/(R6 + R10)) + (1/R8) + (1/R4) + (1/R7)]$$

2. Ringing condition:

$$V_{SUP+} = [V_{DD}(1/R5) + V_{BATT}(1/(R3 + R1))]/[(1/(R1 + R3)) + (1/R9) + (1/R5)]$$

$$V_{SUP-} = [V_{DD}(1/R4) + V_{BATT}(1/R2) - Il(R10)(1/R6)]/[(1/R2) + (1/(R7 + R11)) + (1/R6) + (1/R8) + 1/R4)]$$

Circuit values:

Derived values	Typical Values
R1 = 200 Ω	200 Ω
R2 = R	1 MΩ
R3 = R	1 MΩ
R4 = R/9.8	102 kΩ
R5 = R/9.4	107 kΩ
R6 = R	1 MΩ
R7 = R	1 MΩ
R8 = R/27.2	36.5 kΩ
R9 = R/29.6	33.2 kΩ
R10 = 400 Ω	400 Ω
R11 = 200 Ω	200 Ω
V_{DD} = 5 V	
V_{BB} = −48 V	
Typically R = 1 MΩ	

Substitution of the circuit values yields the following:

Nonringing condition:

$$V_{SUP+} = (5)I_L - 0.025 \text{ V}$$
$$V_{SUP-} = (-5)I_L + 0.025 \text{ V}$$
$$V_{SUP+} - V_{SUP-} = (10)I_L - 0.050 \text{ V}$$

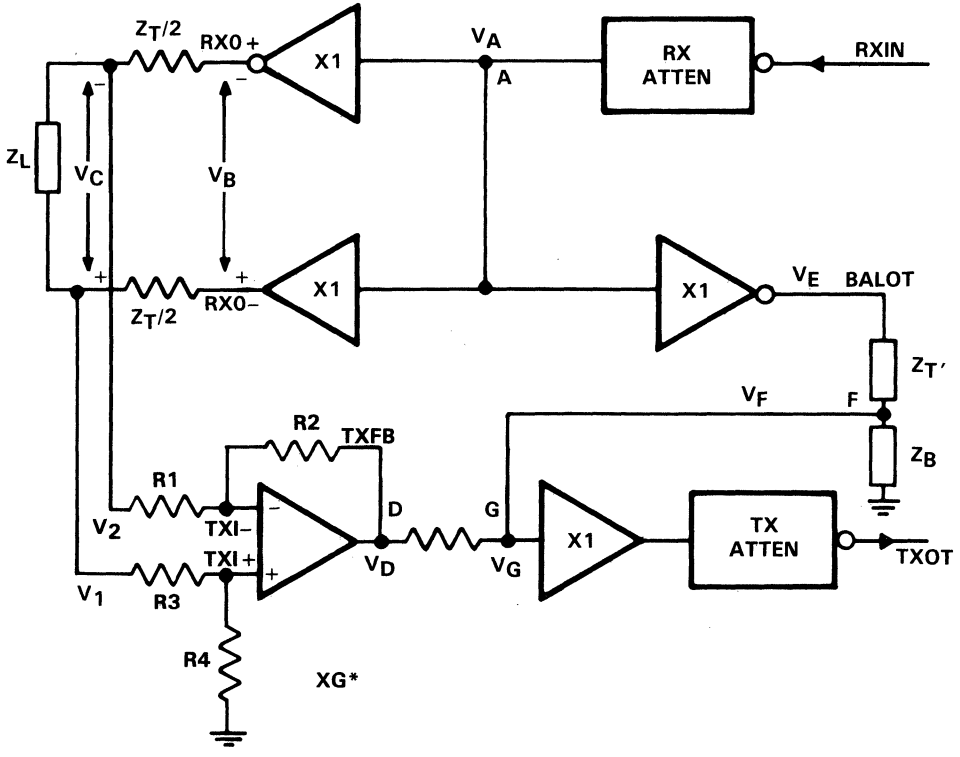
Ringing condition:

$$V_{SUP+} = -0.025 \text{ V}$$
$$V_{SUP-} = (-10)I_L + 0.025 \text{ V}$$
$$V_{SUP+} - V_{SUP-} = (10)I_L - 0.050 \text{ V}$$

NOTE: I_L is in mA

Hybrid Circuit

Figure 5 shows that any signal that is applied at the receive input (RXIN) will appear across the transmit-amplifier inputs. The hybrid prevents the received signal from being returned on the transmit output (TXOT). The SLCC performs the hybrid function with the amplifier configuration of Figure 10. With a proper balance network, the receive signals at nodes D and F will be equal in amplitude and opposite in phase, cancelling completely at node G.



*The gain of this amplifier is set by the user. If R1/R2 = R3/R4, the output is $V_O = \frac{R2}{R1}(V_1 - V_2)$, or G = R2/R1.

Figure 10. SLCC Hybrid Function Amplifier Configuration

In the illustration, the gains of all internal amplifiers are unity, except for the transmit-input amplifier, which has a gain G that is set by the user with external resistors. The impedance Z_T is the termination impedance and Z_L is the line impedance, which is reflected through the battery-feed transformer.

Analysis of the hybrid can be accomplished by assuming that a signal is applied at RXIN such that $V_A = 1$ V. By tracing the signal to the various nodes, the following voltages are obtained:

$$V_A = 1 \text{ V}$$
differential voltage $V_B = 2$ V
differential voltage $V_C = 2[Z_L/(Z_T + Z_L)]$ V
$V_D = 2G[Z_L/(Z_T + Z_L)]$ V
$V_E = -1$ V
$V_F = -Z_B/(Z_T' + Z_B)$ V

For proper signal cancellation:

$$V_D = -V_F \text{ or}$$
$$2G[Z_L/(Z_T + Z_L)] = Z_B/(Z_T' + Z_B)$$
$$(1/2G)[Z_T/Z_L + 1] = Z_T'/Z_B + 1$$
$$1/2G[(Z_T/Z_L) + 1] = Z_T'/Z_B + 1$$

If G is set to 1/2, for proper signal cancellation:

$$Z_T/Z_L = Z_T'/Z_B$$

NOTE: If G is not equal to 1/2, proper balance cannot be obtained.

The impedances Z_T' and Z_B can be scaled versions of Z_T and Z_L. By scaling the impedances up, large resistors and small capacitors can be used in the balance networks. The impedance of the three balance networks in parallel must be greater than 10 kΩ to prevent loading the balance output (BALOT).

Flux-Cancelling Drive Circuit

In the CO or PBX, the dc loop current flows through the transformer coil. This dc current in turn produces a dc flux in the core of the transformer. As the size of the transformer decreases, its core tends to become saturated at lower flux levels. In order to use the smaller transformers required to conserve space, a means of preventing core saturation is necessary.

Many transformers now have a flux-cancelling winding. This extra winding provides a means of generating a dc core-flux to oppose that created by the local loop. Normally, the CO-side to subscriber-side turns ratio is 1:1. If the CO or subscriber-side has n turns, the flux-cancelling winding usually has 3 n to 5 n turns. By forcing a current through the flux-cancelling winding that is 1/3 (for 3 n turns) to 1/5 (for 5 n turns) of the loop current, the dc core-flux is kept at 0, even for large loop currents. Using the standard dot convention, if the loop current flows into the dot on the subscriber side, the flux-cancelling current must flow out of the dot in the flux-cancelling winding.

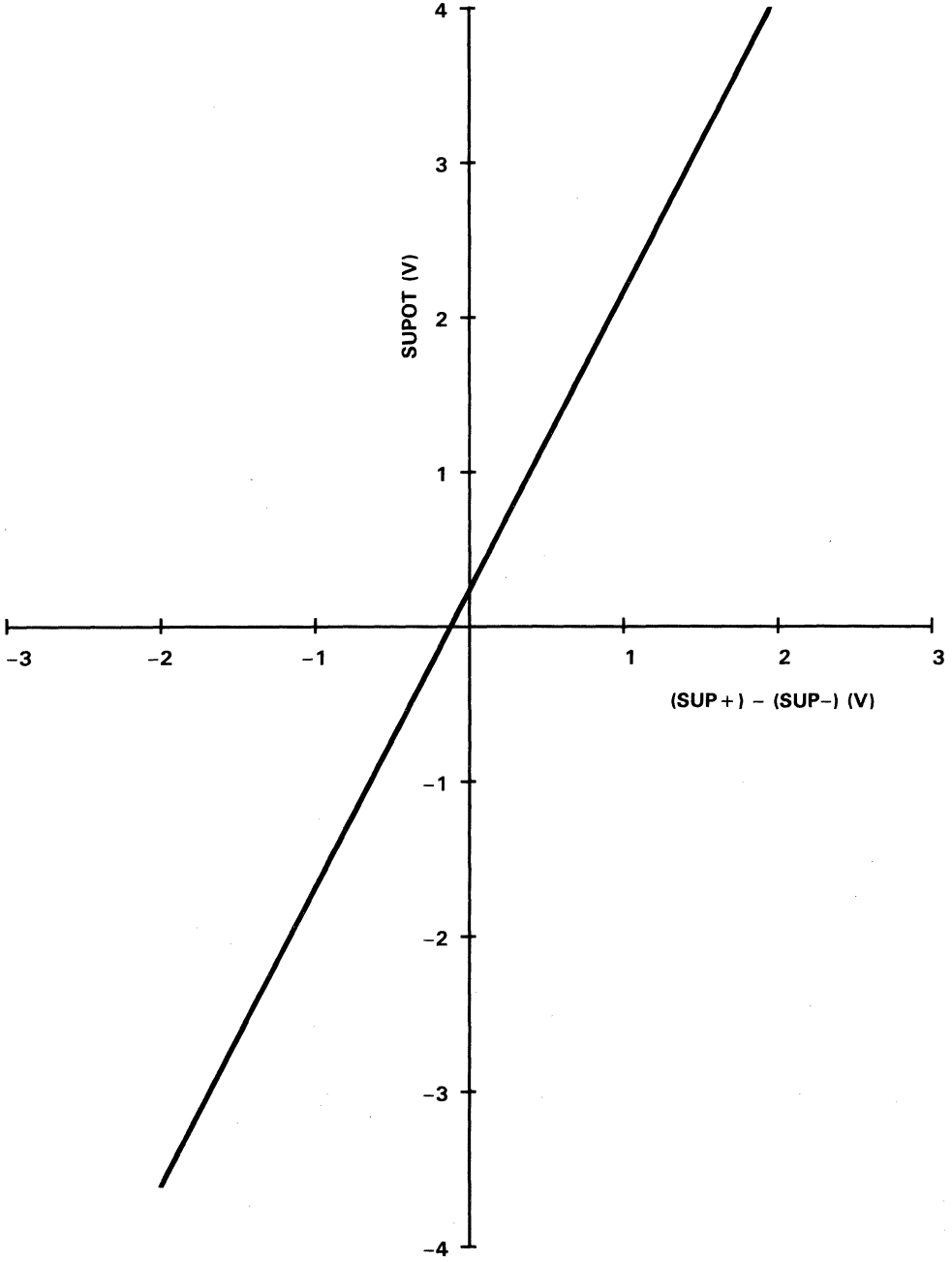


Figure 11. SUPOT as a Function of Supervision Input

Driving the flux-cancelling winding of the transformer requires a high impedance current source. This fact is indicated by the impedance transformation across the transformer. If a transformer has a flux-cancelling to subscriber-side turns ratio of n:1, the flux-cancelling drive circuit impedance is reflected to the CO side as 1/n its actual value. For a turns ratio of 5:1, which is a typical value, the impedance is reflected as 1/25th of its value. Unless the impedance of the drive circuit is high, it will load the output from the CO.

Figure 11 is a plot of SUPOT versus differential supervision input-voltage, (SUP+) -(SUP-). SUPOT is a high impedance output that provides a voltage twice that of the differential input. From Figures 7 and 11, a plot of SUPOT versus loop current is obtained (see Figure 12).

The linear relationship between SUPOT and loop current allows the use of a voltage-controlled current source as the flux-cancelling winding drive circuit. Figure 13 is one possible example. The voltage at node A is the negative of SUPOT. Proper choice of R1 provides the correct flux-cancelling current. Since the voltage at node A exactly follows SUPOT, this circuit offers a very high impedance to the transformer.

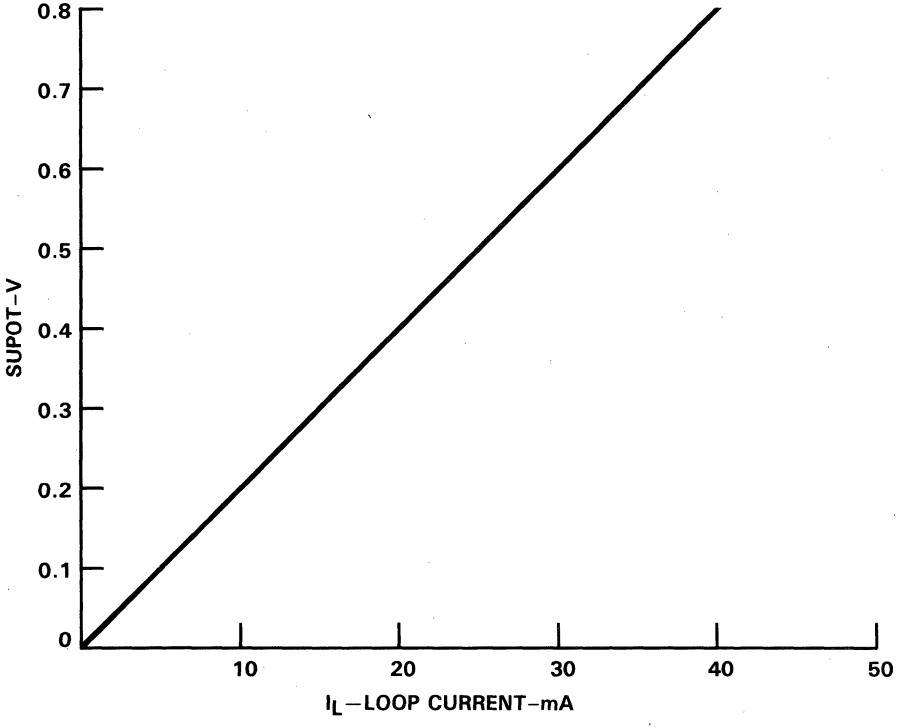


Figure 12. SUPOT as a Function of Loop Current

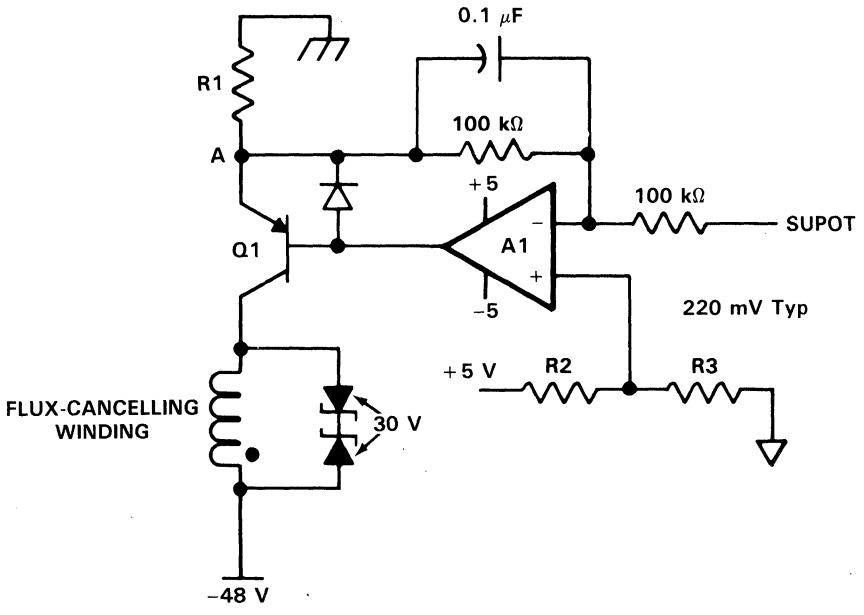


Figure 13. High-Impedance Drive Circuit for a Flux-Cancelling Winding

Increasing the gain of the op-amp circuit and adjusting R1 accordingly minimizes the dissipation of power in Q1. The upper limit on R1 is determined by the maximum current that must be provided, plus the dc resistance of the winding. At maximum current, Q1 must remain out of saturation; that is, $V_{CE} > V_{CE(sat)}$.

A design example is a flux-cancelling to subscriber-to-CO turns ratio of 5:1:1. From Figure 12, notice that at 0 mA loop current SUPOT is 0 V, and at 20 mA loop current SUPOT is 0.4 V. These points give a slope of (0.4 - 0)/(0.02 -0) = 20. Since only one fifth the loop current is required, R1 is chosen as 20 × 5 = 100. The power dissipated in Q1 is the following:

$$\begin{aligned} P_{diss} &= I_C \times V_{CE} \\ &= I_C[48 - I_C(R1 + RW)] \\ &= I_C[48 - RT \times I_C];\ RT = R1 + RW \end{aligned}$$

where RW is the dc resistance of the winding. The maximum power dissipation occurs where the first derivative is 0:

$$dP_{diss}/dI_C = 48 - 2RT \times I_C = 0$$
$$I_C = 24/RT$$

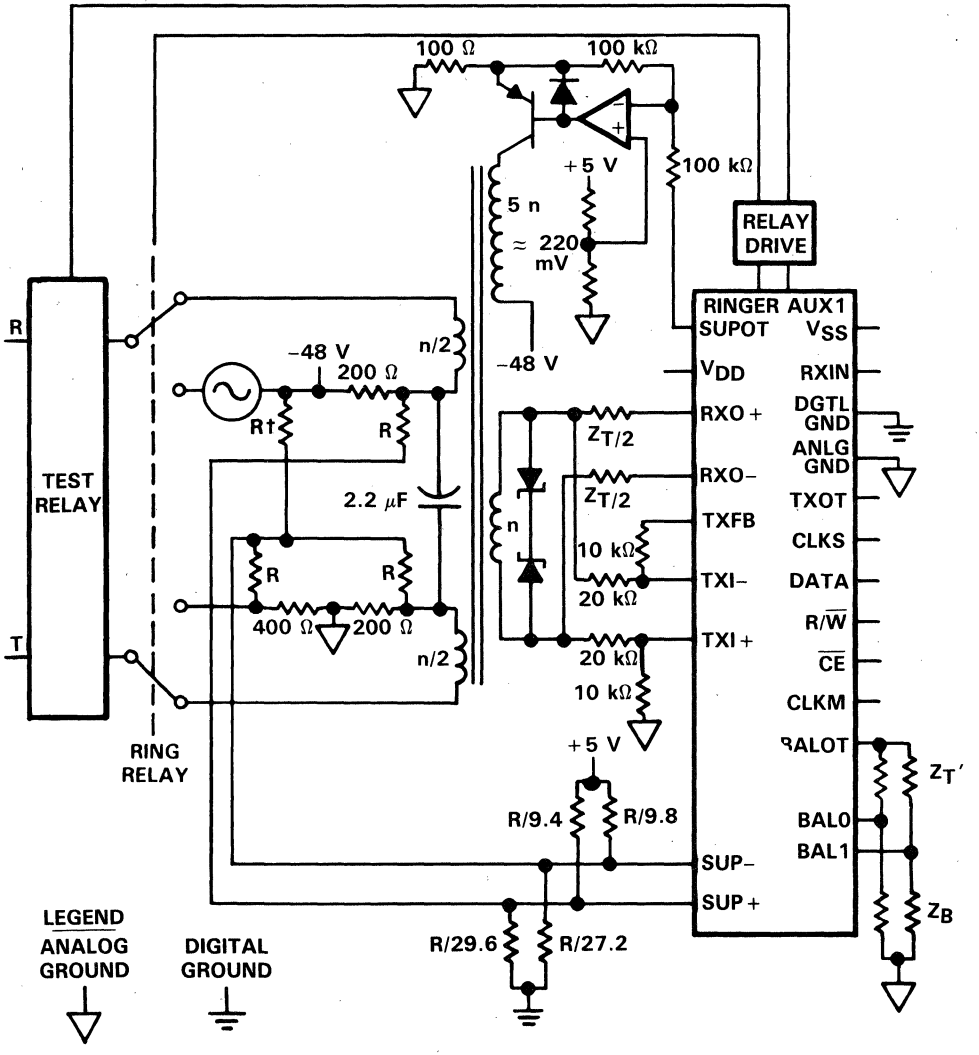
Substituting this value into the power equation gives

$$\begin{aligned} P_{diss}(max) &= (24/RT)[48 - RT(24/RT)] \\ &= 24/RT \\ &= 576/RT. \end{aligned}$$

The collector-to-emitter breakdown voltage of Q1 must be considered. This transistor must tolerate a V_{CEO} of 48 V, and one possible component for this position is the 2N2905A.

The operational amplifier A1 in the diagram can be any inexpensive circuit that will operate from +5 V to -5 V, such as the MC1458 dual op-amp.

Figure 14 shows a TCM4207A application with the flux-cancelling drive circuit.



†Typically, R = 1 mΩ

Figure 14. TCM4207A SLCC Standard Subscriber Line

Conclusion

The Subscriber Line Control Circuits from Texas Instruments offer all low-voltage line-card functions on a single CMOS IC. This solution provides high performance while using less board space than conventional solutions. The low power consumption (typically 75 mW) of the SLCC also gives it improved reliability over other solutions. For further specifications of the TCM4204A series, refer to the data sheet elsewhere in this book.

TISP Series Transient Suppressors

M.J. Maytum
Member Group Technical Staff
Power Products Application Manager
Texas Instruments Ltd.

TEXAS INSTRUMENTS

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List of Illustrations

Introduction

The rapid growth of the semiconductor content in telephone systems has dramatically altered the kind of protection required against such hazards as lightning and accidental connection to ac lines. Protection methods developed for the previous generation of exchange interfaces and subscriber sets are no longer adequate. New protection devices must offer faster response, well defined voltage levels, reliable operation, and no interference with normal system operation.

Texas Instruments has developed three families of transient suppressors that cover the most common subscriber line interface circuit (SLIC) configurations. These bidirectional devices provide shunt protection against transient static voltages between the wires of an exchange pair or from either wire to ground. In addition, they are capable of providing protection against damage from induction from or even accidental connection to some kinds of ac sources.

This report describes the important characteristics of the TISP1XX, TISP2XX, and TISP3XX families of transient suppressors, defines the dc parameters, and discusses the various system stresses under ac line contact testing.

Basic Characteristics

Construction

The successful and reliable operation of any protection system depends to a large extent on the design and fabrication of the components used. The active part of the TISP transient suppressor is a silicon chip structured with alternate layers of P and N type material. The chip is fabricated using Texas Instruments Ion-Implanted Planar (I^2P) process which permits precise control of the electrical characteristics, extremely stable parameters, and the monolithic integration of two bidirectional suppressors on a single chip.

The chip's back surface has a multimetal system deposited on it to ensure good contacting and solderability. In assembly, the back is soldered to a plated copper tab which acts as the common connection for the two suppressors and provides a thermal path for heat losses to the external ambient. Two soldered connections are made to the chip's top surface metallization pattern to bring out the active suppressor leads. A third central lead is soldered and keyed to the copper tab to provide the common connection. All the leads are formed from punched and plated 0.38 mm copper strip. The chip is protected against mechanical and environmental damage by a nonflammable plastic cap which is filled with epoxy.

Operation

The TISP series of shunt protectors are breakover-voltage-triggered, high-holding-current, bidirectional devices (Figure 1). Voltage transients are initially clipped by avalanche action until the protector current rises to the breakover level, which causes the device to trigger to the "on" state. Spurious triggering is avoided by ensuring the breakover current is greater than 150 mA and the dV/dt rating is better than 5 kV/μs. After breakover, the protector's low voltage condition allows it to sink very large currents without incurring the temperature and voltage rise of conventional "zener" protectors. A high holding current, which is greater than 150 mA at 25°C and 100 mA at 70°C, avoids system dc latch-up as the transient subsides.

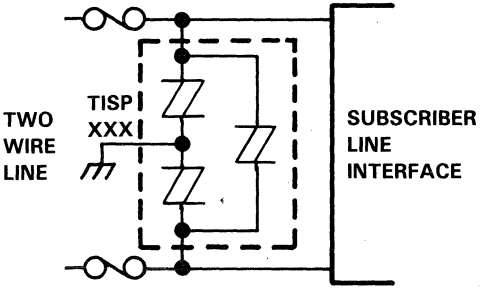


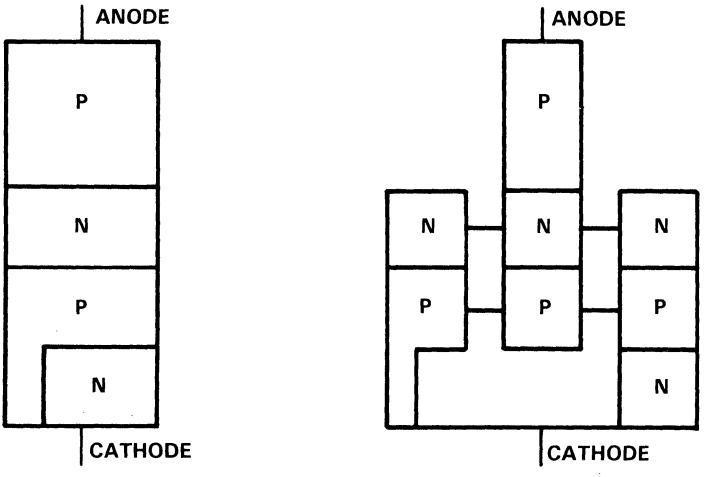
Figure 1. Typical Applications Circuit

The high thermal mass of the TO-220 package copper tab strongly contributes to the device protection performance with short- and medium-duration transients. Long-term transients, such as shorts to outside voltage supplies, can be protected against by the use of fuses or positive temperature coefficient (PTC) thermistors to terminate or reduce the fault current.

Under normal operating conditions the TISP series presents negligible loading on the telephone line due to its very low leakage planar construction and precise avalanche voltage.

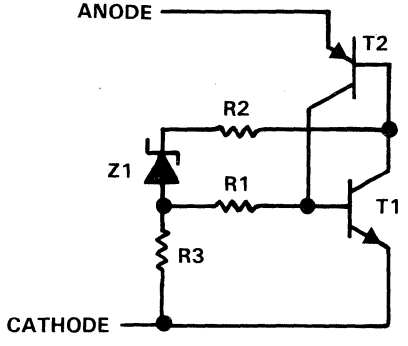
Equivalent Model

Each protector section consists of two opposing thyristors connected in parallel to give bidirectional operation. It is sufficient to analyze only one thyristor in the appropriate polarity as the two thyristors are almost symmetrical in structure. Figure 2 shows how the PNPN thyristor structure can be segmented into a PNP transistor, T2, and an NPN transistor, T1, with a common collector-base junction. Triggering occurs by collector-base junction avalanche breakdown depicted in the equivalent circuit by zener diode Z1 and the normal slope resistance R2. The thyristor's P gate region is shorted by the cathode metallization to produce a low-value resistance, the equivalent shown as resistors R1 and R3 across the NPN transistor's base-emitter junction to give the thyristor its high holding current.



(a) SIMPLIFIED STRUCTURE

(b) STRUCTURE COMPONENTS



(c) CIRCUIT EQUIVALENT

Figure 2. Two Transistor Analog of the Thyristor

Model Analysis

This analysis is extremely simplistic and is only intended to provide an overview of the device's operation to enable designers to estimate how it will interact with system voltage and current conditions.

Definition of Symbols

V_{BE1} — Transistor, T1, base-emitter voltage
V_{BE2} — Transistor, T2, base-emitter voltage
V_Z — Zener diode avalanche voltage
$\alpha 1$ — Transistor, T1, alpha current gain
$\alpha 2$ — Transistor, T2, alpha current gain

Voltages Below V_Z

As the voltage is increased from zero, the only current flowing will be due to junction and surface leakage, which will be very small. Data sheet measurements of leakage are performed at the typical dc voltage level of −50 V.

Avalanche Region

When the applied voltage exceeds $V_Z + V_{BE2}$ the thyristor will start to conduct. The onset of the avalanche region is defined as the voltage developed across the suppressor at a current level of 1 mA. At a current level of I_X the terminal voltage, V_X, in Figure 3 will be:

$$V_X = V_{BE2} + V_Z + I_X(R2 + R3)(1 - \alpha 2) + R3I_X\alpha 2$$

giving

$$V_X = V_{BE2} + V_Z + I_X[R3 + R2(1 - \alpha 2)]$$

Differentiating this with respect to I_X gives the avalanche slope resistance, R_A, which is:

$$R_A = R3 + R2(1 - \alpha 2)$$

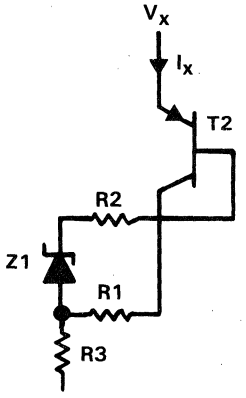


Figure 3. Circuit Analogy for Avalanche Condition

Experienced transistor users might have expected the PNP transistor, T2, to avalanche initially at $BV_{BE2} + BV_{CBO2}$, breaking back to BV_{CEO} as the current increased. In practice this effect is negligible, because to block in the negative direction transistor T2 must be implemented with a low gain, $\alpha 2$ which results in the two breakdown voltages being almost equal.

Breakover

The avalanche characteristic terminates with the regenerative turn-on of transistors T1 and T2. This initiates when the voltage drop across resistors R1 and R3 in Figure 4 reaches V_{BE1} at a current level of I_{BO}.

Thus:

$$V_{BE1} = I_{BO}R3 + I_{BO}\alpha_2 R1$$

giving

$$I_{BO} = \frac{V_{BE1}}{R3 + \alpha_2 R1}$$

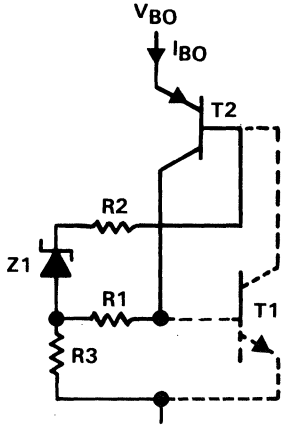


Figure 4. Circuit Analogy for Breakover Condition

The breakover voltage level, V_{BO}, will be the value of V_X when $I_X = I_{BO}$. Substituting and simplifying gives:

$$V_{BO} = V_{BE2} + V_Z + \frac{V_{BE1}[R3 + R2(1 - \alpha_2)]}{R3 + \alpha_2 R1}$$

The above equation predicts the voltage excursion from initial avalanche to breakover will be:

$$\frac{V_{BE1}[R3 + R2(1 - \alpha_2)]}{R3 + \alpha_2 R1}$$

When the suppressor triggers "on" its current will greatly increase, ensuring that regeneration is maintained. Consider a voltage source, V_S, and internal resistance, R_S, at breakover.

$$V_S = V_{BO} + I_{BO}R_S$$

Neglecting the thyristor "on" voltage drop, the crowbar current, I_{TM}, will be:

$$I_{TM} = \frac{V_S}{R_S} = I_{BO} + \frac{V_{BO}}{R_S}$$

This is the initial crowbar current. In cases where V_S is time variant, much higher current values can be achieved later in the suppression cycle. The 5-A "on" voltage level is specified as 3 V maximum for TISP series devices.

Regenerative Condition

After breakover has occurred, the transistors will remain in conduction until the current drops to a critical value called the holding current, I_H, whereupon regeneration stops and the transistor pair delatches. If the system continues to supply current with sufficient voltage compliance, the voltage will rise until it is limited by the avalanche characteristic. The base current available to drive transistor T1 in Figure 5 is:

$$\alpha_2 I_H - \frac{V_{BE1}}{R1 + R3}$$

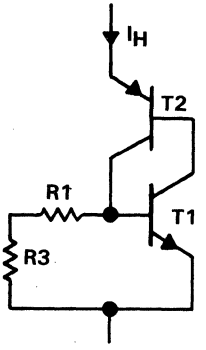


Figure 5. Circuit Analogy for Holding Current Condition

Its base current requirement to maintain regeneration is:

$$\frac{I_H(1 - \alpha_2)(1 - \alpha_1)}{\alpha_1}$$

When these two values are equal, regeneration is just maintained. Setting these two equations equal and simplifying gives:

$$I_H = \left(\frac{V_{BE1}}{R1 + R3}\right)\left(\frac{\alpha_1}{\alpha_1 + \alpha_2 - 1}\right)$$

Because the alpha current gain of the NPN transistor, T1, will be close to unity, the holding current equation may be approximated to:

$$I_H = \frac{V_{BE1}}{(R1 + R3)\alpha_2}$$

Negative Voltages

Reverse voltages are blocked by the reverse biased base-emitter junction of PNP transistor, T2, and the only current flowing will be due to junction and surface leakage.

The reverse breakdown voltage of the base-emitter junction is designed to be higher than the breakover voltage so that the opposing thyristor limits the voltage in the negative polarity.

Definition of DC Parameters

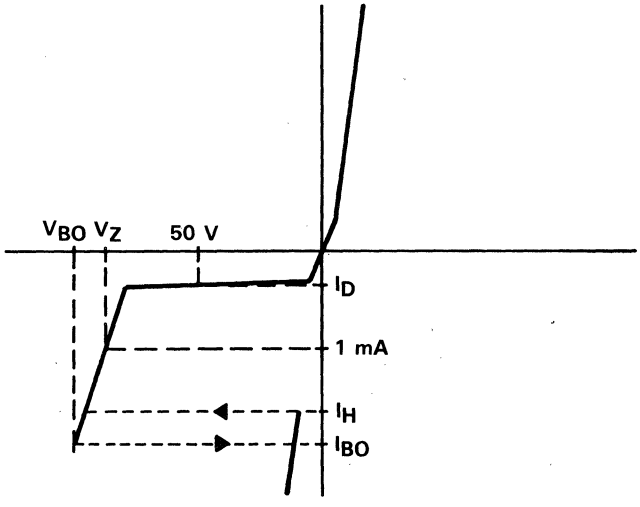
Device Characteristics

The two outer TO-220 package leads, each connected to a line wire, are termed A and B. The center lead, termed C, is the ground connection. Thus, wire-to-ground voltages are V_{AC} and V_{BC}, and the wire-to-wire voltage is V_{AB}.

TISP1XX

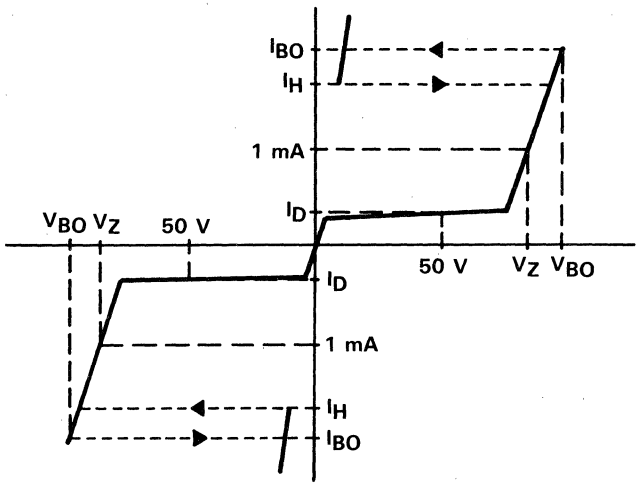
Figure 6(a) shows the wire-to-ground characteristics of the TISP1XX family of suppressors. For positive voltages the devices have a forward biased diode characteristic. The negative characteristic is that of a voltage-triggered thyristor. For this report the relevant measurement points on this characteristic are:

I_D — The leakage current at the test voltage V_D
V_Z — The initial clipping or avalanche voltage measured at 1 mA.
I_{BO} — The current level (pulsed) at which the device triggers to the "on" state.
I_H — The current at which the device triggers back to the "off" state.



(a) AC AND BC CHARACTERISTIC

Figure 6. TISP1XX Characteristics



(b) AB CHARACTERISTIC

Figure 6. TISP1XX Characteristics

Figure 6(b) shows the wire-to-wire, symmetrical, voltage-triggered thyristor characteristic of the TISP1XX family. These devices start to clip wire-to-wire and negative wire-to-ground voltages at V_Z.

TISP2XX

Figure 7 shows the symmetrical, voltage-triggered thyristor characteristic of the TISP2XX family of suppressors. At the current levels being considered there is little

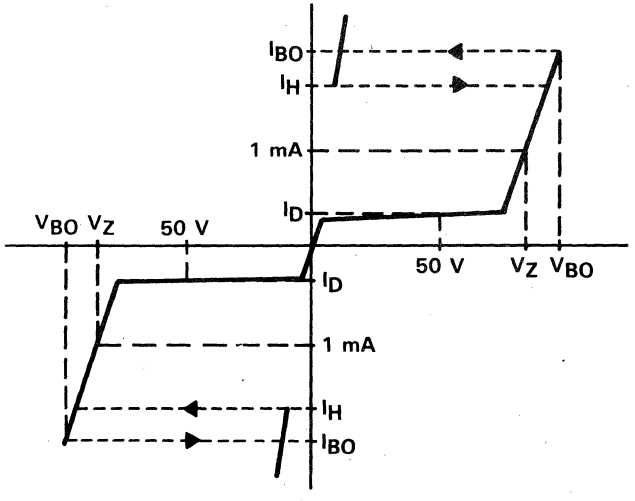
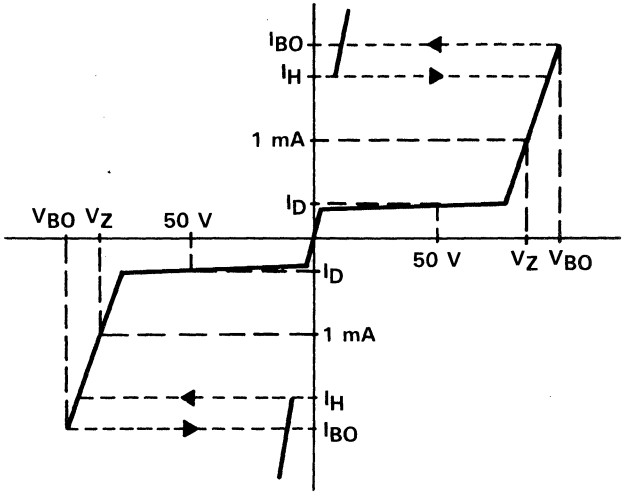


Figure 7. TISP2XX AC, BC, and AB Characteristic

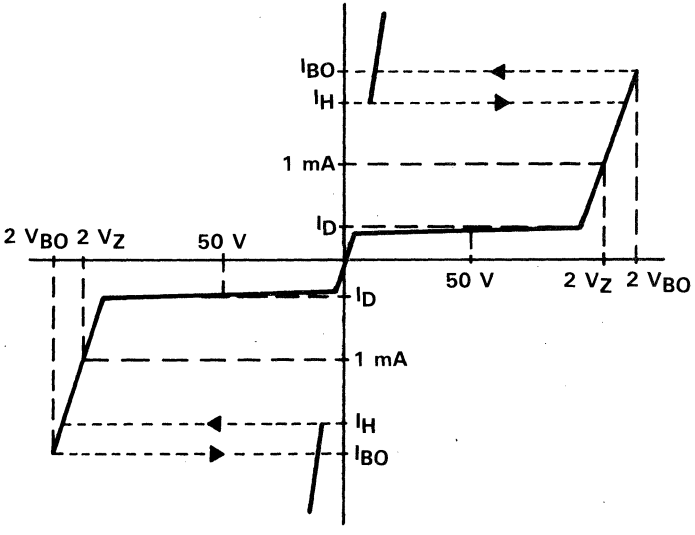
difference between the wire-to-ground and the wire-to-wire characteristics. Thus, these devices start to clip both wire-to-ground and wire-to-wire voltages at V_Z.

TISP3XX

Figure 8(a) shows the wire-to-ground, symmetrical, voltage-triggered thyristor characteristic of the TISP3XX family of transient suppressors. In respect it is the



(a) AC AND BC CHARACTERISTICS



(b) AB CHARACTERISTIC

Figure 8. TISP3XX Characteristics

same as the TISP2XX family. The difference between the two families occurs in the wire-to-wire characteristic. Figure 8(b) shows the TISP3XX devices start to clip wire-to-wire voltages at $2V_Z$. Although the suppressors are monolithically integrated into a single chip, the TISP3XX devices provide the same functionality as two bidirectional single-wire suppressor chips with a common ground connection.

On-Hook Conditions

When the telephone is on hook, its dc line loading is negligible. Typically, one wire of the line would be close to ground potential and the other wire would be at the line driving source potential, normally about −50 V (the exchange battery).

Under these conditions the dc line loading is limited to a current value which will not activate the dc off-hook detection circuit. Loading values of several mA are often permissible, and it would be reasonable to allow 20% of this for suppressor leakage under worst case conditions, e.g., 0.5 mA.

The suppressor leakage current increases with temperature, and its value is the sum of surface and bulk leakages. The significance of any particular component will depend on the temperature and the family being considered. Under normal conditions the device junction temperature will be almost the same as the local ambient. The example given of 0.5 mA and 50 V would cause a junction-to-ambient differential of about 1.5°C (0.5 mA × 50 V × 62.5°C/W). If the maximum exchange temperature were 70°C, the required specification would be:

$$I_D < 500\ \mu A \quad T_{CASE} = 71.5°C,\ V_D = -50\ V$$

In practice, consideration also needs to be given to the off-hook detection circuit to determine the effective system leakage current of the suppressor. Ideally it should only monitor the dc flowing wire-to-wire (I_{AB} is a guarded three terminal measurement). Typically, wire-to-ground leakage will also contribute to the monitored current. For example the Texas Instruments European SLIC IC system would sense an effective current $I_{AB} + (I_{AC} - I_{BC})/(2)$ (all these currents are quoted as three terminal guarded measurements). In this situation the most prudent way to specify the leakage current measurement is with the third (floating) terminal connected to the most positive potential to maximize the leakage. Thus, if the the current through A and B were to be measured with A negative, it would be $-I_{AB/C}$ and if B were negative (A positive) then it would be $-I_{BA/C}$.

Ringing Conditions

It is normal to apply (battery) dc voltage as well as the ring voltage to to the line during the ringing condition. There are several ways in which this can be implemented, and the most common configurations are examined in the following subsections. The maximum battery voltage is designated V_{BATM} and the peak of the maximum ringing voltage $V_{RINGPKM}$. It is assumed that ringing conditions cause the greatest voltage excursions in normal operation and so set the voltage limits.

Battery-Backed Ringing

In the configuration of Figure 9, one wire has the series combination of battery and ring generator applied to it while the other wire is returned to ground. If the line is unloaded (worst case condition) only one terminal of the suppressor will be exercised, the other being at 0 V. Clearly in this arrangement the maximum voltage wire-to-wire will be the same as the wire-to-ground and the TISP2XX family, with its completely symmetrical characteristics, will give the most effective suppression.

The maximum negative voltage will be $V_{BATM} + V_{RINGPKM}$ and the maximum positive voltage will be $V_{RINGPKM} - V_{BATM}$. In this case the negative excursion dominates and defines the value of avalanche voltage V_Z to avoid peak clipping.

Clipping would not normally reduce the ringing power significantly and, typically, insufficient current ($< I_{BO}$) is available to trigger the suppressor and grossly distort the negative peaks. Clipping needs to be avoided to remove the possibility of false off-hook detection. This could occur because clipping causes partial rectification of the ringing voltage, resulting in a net circuit dc which is then interpreted by the off-hook detector as the telephone handset being picked up. Temperature effects on voltages have been taken into account for the suppressor avalanche, V_Z, the battery, and the ring generator. Normally the quoted battery and ring generator levels comprehend the exchange temperature variation. The temperature coefficient of avalanche breakdown, S_Z, is about 0.1%/°C. Thus to cover operation down to a minimum exchange temperature of T_{MIN}, the required 25°C avalanche voltage, V_Z, would be:

$$V_Z = \frac{V_{BATM} + V_{RINGPKM}}{1 + \frac{T_{MIN} - 25}{1000}}$$

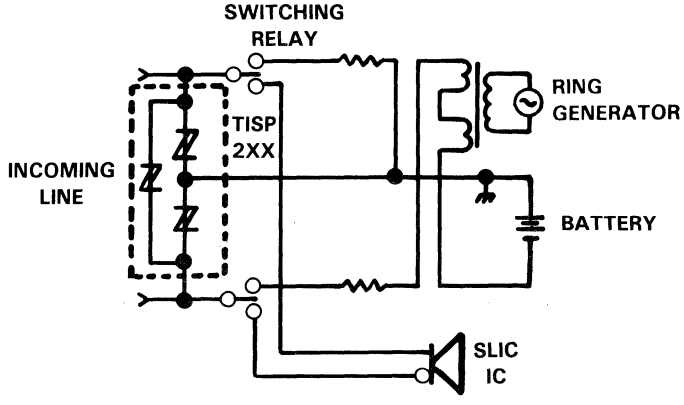


Figure 9. Battery-Backed Ringing Circuit

If, for example, V_{BATM} = −58 V and the ringing voltage were 95 V_{RMS} then the minimum avalanche voltage, V_Z, should be:

$$V_Z = 58 + (\sqrt{2} \times 95) = 192 \text{ V}$$

For a minimum exchange temperature of −15°C, the 25°C measurement becomes:

$$V_Z = \frac{192}{1 + \frac{-15 - 25}{1000}} = 200 \text{ V}$$

When the effects due to line and bell loading are taken into account this typically results in 5% to 10% extra safety margin in clipping level.

Ground-Backed Ringing

In the configuration of Figure 10, one wire has the battery connected to it and the other has the ground referenced ring generator. In the unloaded case the peak voltages on the wires will be $-V_{BATM}$ on the battery wire and $\pm V_{RINGPKM}$ on the ring generator wire. Usually the ringing voltage will be the largest and will set the wire-to-ground avalanche requirement. However, the wire-to-wire voltage will be greater than this, being $V_{BATM} + V_{RINGPKM}$, necessitating the use of a TISP3XX series device which has a wire-to-wire rating of 2V_Z.

Taking the values used in the battery-backed ringing case gives a 25 °C value of V_Z wire-to-ground of:

$$V_Z = \frac{V_{RINGPKM}}{1 + \frac{T_{MIN} - 25}{1000}} = \frac{\sqrt{2} \times 95}{1 + \frac{-15 - 25}{1000}} = 140 \text{ V}$$

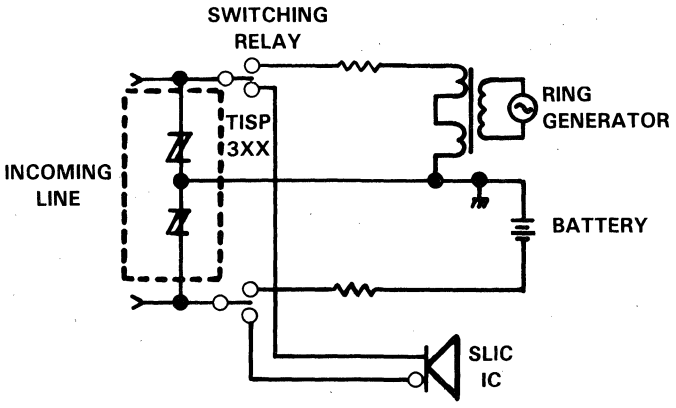


Figure 10. Ground-Backed Ringing Circuit

The peak voltage between the wires will be the sum of the battery and generator voltages, which was found to be 192 V in the previous subsection. Also, the 25°C requirement was found to be 200 V. This is comfortably inside the 2 × 140 = 280 V wire-to-wire avalanche rating that results from the TISP3XX structure.

Again, the practical effects of line and bell loading increase the clipping safety margin.

Balanced Ringing

In the configuration of Figure 11, the battery is connected to one wire and the ringing voltage is shared equally between the two wires to balance its voltage with respect to ground. The battery wire will have peak voltages of ($V_{RINGPKM}/2$) − V_{BATM} and −($V_{RINGPKM}/2$) + V_{BATM}. The other wire will have ±$V_{RINGPKM}/2$. Between the wires, there will be a peak voltage of: $V_{RINGPKM}$ + V_{BATM}. Allowing for temperature effects gives 25 °C avalanche voltages of:

$$V_Z = \frac{\frac{V_{RINGPKM}}{2} + V_{BATM}}{1 + \frac{T_{MIN} - 25}{1000}}$$

$$V_{Z(AB)} = \frac{V_{RINGPKM} + V_{BATM}}{1 + \frac{T_{MIN} - 25}{1000}}$$

If the earlier example values are substituted, then V_Z > 130 V and $V_{Z(AB)}$ > 200 V. Again this is an application for the TISP3XX series of devices.

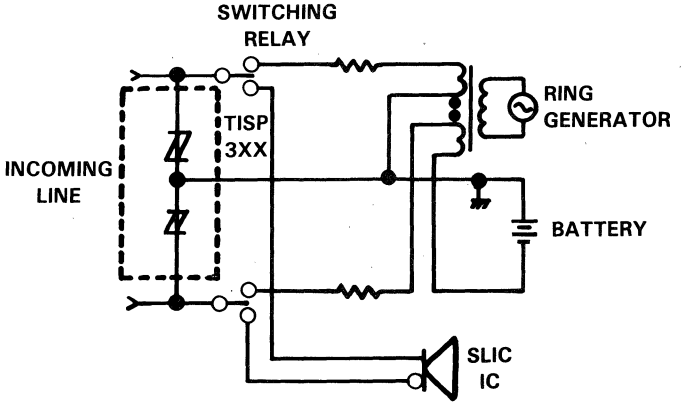


Figure 11. Balanced Ringing Circuit

Test Access

In fault finding and preventative maintenance operations, test signals are applied to the line and SLIC. If the applied voltage levels exceed normal telephone operation, these levels would determine V_Z. Extremely high levels of test signal to the line and correspondingly high V_Z requirements could lead to the loss of adequate SLIC protection. In this situation, the transient suppressor should be connected to the SLIC side of the test access relay so that V_Z can be set by normal system operating levels and SLIC protection maintained.

Minor Transients

The pervasive nature of the telephone network means the possibility of induced transients is very high. While the energy levels of these may not be substantial, they can cause the voltage to rise to a level which makes the suppressor clip. Pulse dialing telephones, which periodically short the line, can, under certain conditions, also cause suppressor clipping. This situation is aggravated by the increasing use of electronic ringers, such as the TCM1506, whose antitapping function is achieved electronically rather than by bell loading. Obviously the interference level would be compounded if breakover occurred. Under these conditions a reasonable compromise is to make $I_{BO} = I_H$ for the minimum values.

SLIC Only Protection

Certain integrated SLIC implementations utilize medium-voltage IC technology and cannot be subjected to ringing voltage levels. This is not a major problem as it is possible to configure the system to switch out the SLIC during the ringing operation. In this case a transient suppressor on the line would not provide complete SLIC protection. Adequate protection can be achieved by the use of a TISP1XX transient suppressor connected directly across the SLIC output. This configuration is shown in Figure 12.

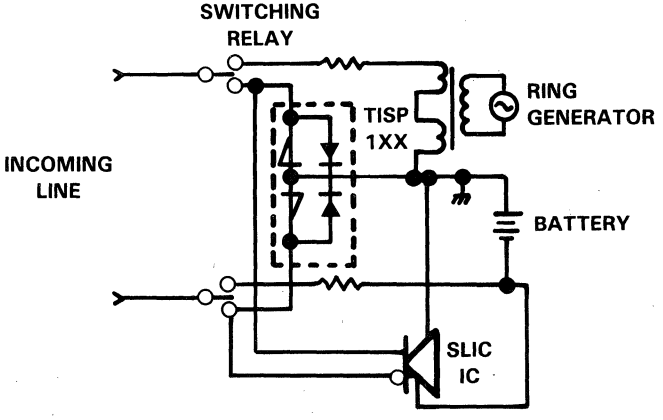


Figure 12. SLIC Only Protection Circuit

Typically the supply lines to the IC are 0 V and battery. Sometimes the battery voltage may be boosted to comprehend long lines and an additional +5 V supply used for logic interfacing. The TISP1XX family of transient suppressors ensures the SLIC is protected against positive voltages by having a forward biased diode characteristic in this direction. In the negative direction the value of V_Z will be set by the SLIC output swing which will be $V_{BATM} - V_{SAT}$, where V_{SAT} is the saturation voltage of the IC's driver stage. Using the previous values of voltage and temperature and assuming $V_{SAT} = 2$ V gives a 25°C value of V_Z wire-to-ground of:

$$V_Z = \frac{V_{BATM} - V_{SAT}}{1 + \frac{T_{MIN} - 25}{1000}}$$

$$= \frac{58 - 2}{1 + \frac{-15 - 25}{1000}}$$

$$\approx 58 \text{ V}$$

In operation, both wires of the line will be negative and the wire-to-wire voltage magnitude will be less than the value of V_Z calculated above.

Holding Current I_H

Large single pulse transients will exercise the suppressor in the following manner. When the transient's leading edge reaches the line card it will override the existing voltages until the suppressor starts to clip. In nondiode cases, once the current in the suppressor exceeds I_{BO}, the suppressor saturates, absorbing the transient current at low voltage.

As the transient current decays, the saturated suppressor will be left carrying whatever current the system can provide. The worst case condition is for negative transients when the suppressor could be left with the line dc feed current, I_{dc} (in the case of a positive transient current, negative dc feed current would actually help to terminate the crowbar action of the suppressor). It is necessary that the suppressor recover from this condition so that normal system operation is resumed. This can be ensured by making $I_{dc} < I_H$ over the system operating temperature range. Although the junction temperature of the suppressor will rise as a result of the transient, it quickly cools back to the system ambient due to the high thermal capacity of the TO-220 copper tab.

The variation of I_H with temperature is not linear, as shown in Figure 13, but up to about 80°C it is approximately −0.8%/°C. In this range the resultant 25°C value of I_H can be approximated by:

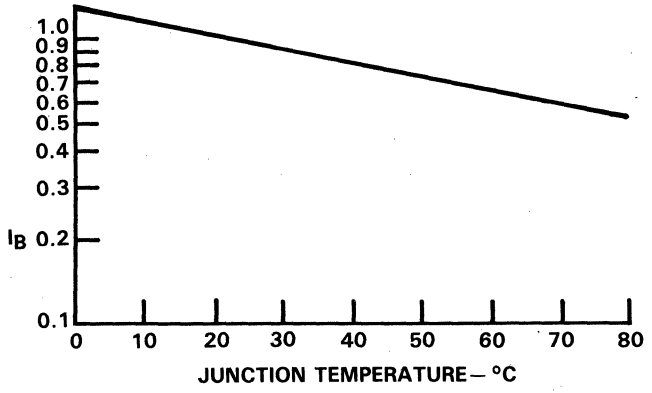


Figure 13. TISP229 Normalized Holding Current Versus Junction Temperature

$$I_H = I_{dc} \Big/ \left[1 - 0.8\left(\frac{T_{MAX} - 25}{100}\right)\right]$$

Using the previous example values and setting the maximum-high-temperature I_{dc} at 100 mA (for a maximum temperature of 70°C ambient) gives:

$$I_H = 100 \Big/ \left[1 - 0.8\left(\frac{70 - 25}{100}\right)\right] = \frac{100}{0.64} \approx 156 \text{ mA}$$

This quantifies the value of I_H expected at 25°C. However, the system designer should specify the exact requirement, i.e., $I_H > 100$ mA at 70°C ambient, rather than an iterated value. If the maximum value of I_{dc} varies substantially with temperature, the minimum holding current requirements should be quoted at several temperatures. This should only be necessary in extreme cases as even the crudest semiconductor current limit is −0.5%/°C and copper coils are −0.4%/°C.

When the suppressor unlatches there is often sufficient transient energy left to force the suppressor into its avalanche region until all the transient's energy is dissipated. Under these conditions it is desirable that I_{BO} is comparable with I_H, otherwise there is not a stable dc operating locus and high level oscillations can occur until the current falls below I_{BO} value.

AC Line Contact Conditions

Design Considerations

There can be a great diversity in ac line contact specifications between the various central office and PABX applications. In this introductory note only the general principles will be addressed rather than specific cases. The Texas Instruments TISP1XX, TISP2XX, and TISP3XX transient suppressor families provide excellent

peak voltage limitation due to their voltage-triggered crowbar action on the low frequency test waveform. This action completely protects the following SLIC against overvoltage. The major parameters of this overvoltage shunt protector will have been set by normal exchange operation, SLIC voltage ratings, and lightning withstand requirements. The ac line contact issues are mainly thermal, in particular the package dissipation capability.

In contrast, the series overcurrent protector has most of its major parameters defined by normal exchange operation and the ac line contact conditions. It is necessary to to understand the interaction of the series and shunt protectors under ac line contact conditions in order to determine the series protector specification. As the interaction depends on the respective specifications, the development tends to be iterative. Generally the loop will be:

1. Choose some appropriate initial values for the series protector.
2. Establish the ac voltage source and resistance values that the protection network and the system can withstand without failure.
3. Compare these with required test levels.
4. Repeat the design exercise until the desired level of protection is achieved.

When failure occurs, even though it may be at test levels far beyond the specification, it should be in a safe manner without creating fumes or flames. Shunt protectors are expected to fail by shorting, and thereby continue to protect the SLIC. In the Texas Instuments TO-220 packaged TISPXXX transient suppressors, soldered connections are made to the chip, thereby avoiding any possibility of bond wires fusing and creating an open circuit. Consideration has also been given to the current carrying capability of suppressor to SLIC PCB tracking to ensure this does not act as a fuse and open circuit the shunt protection. Certain specifications will concede minor damage during testing provided it is easily repairable. Generally this is to cover the use of series fuses in the line for protection.

Configuration

Figure 14 shows a typical SLIC system with the protection, test access, and ringing being separately identified. Depending on the system design requirements the latter two items could be placed either before or after the protection as described in the Definition of DC Parameters section. The ac line contact generator consists of a defined voltage source, V_{GEN}, and output resistance, R_{GEN}, operating at a frequency which is normally specified as 50 to 60 Hz. The generator values can be singular or defined between maximum and minimum limits.

Testing is done with the generator connected between common (ground) and one or both of the line wires. In some cases the generator will also be connected between the two line wires. The application period can be continous, periodic, or for a specified time.

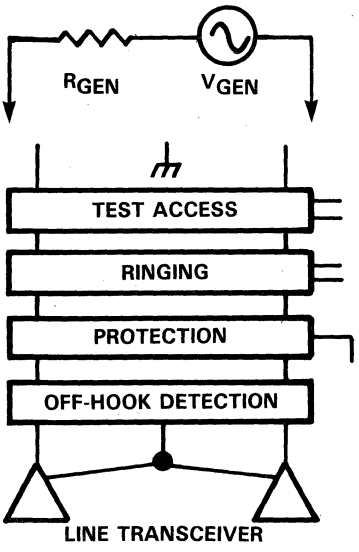


Figure 14. AC Line Contact Testing

The Protection Network

In the protection network, Figure 15, the TISP transient protector provides shunt overvoltage protection and twin fuses, fusible resistors, or PTC thermistors are used for series overcurrent protection.

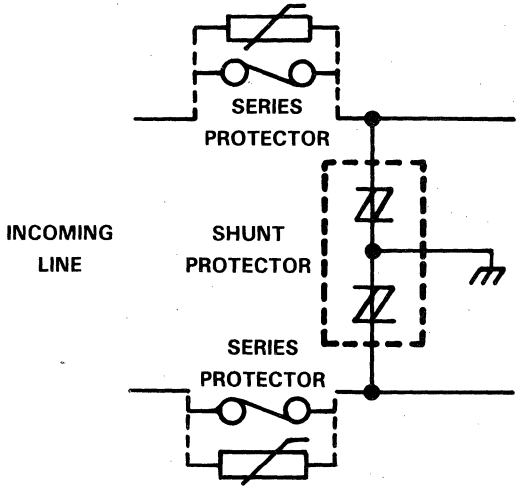


Figure 15. Protection Network

Fuses

A protection policy based on fusing provides the "ultimate" protection for the severest overloads by isolating the equipment, but automatically dictates board rework after an overstress. In this situation it matters little if it is the fuse which needs replacing due to overcurrent, or the transient suppressor due to overdissipation. Fuse performance can be made relatively insensitive to temperature and be extremely stable in spite of overloads close to the fusing level.

It is imperative that "nuisance" fusing does not occur in normal operation or during the specified lightning test. As a result, the fusing current versus time characteristic tends to be of a TT or T nature (i.e., slow blow, antisurge, or time lag fusing, see Reference 1, Chapter 6). For example, a fuse expected to carry 100 mA dc on a continous basis might only be guaranteed to fuse at currents above 250 mA dc. Moreover, for a period of 1 s, currents in excess of 1 A rms could be required to cause fusing. In this situation it may be possible with certain ac contact tests to set up rms current levels which overdissipate the shunt protector in the long term, causing it to short without blowing the fuse.

Figure 16 shows a typical fusing characteristic. The problem area tends to occur at the longer time periods (> 10 s) where the TISP TO-220 package-to-ambient thermal time constant starts to dominate the maximum suppressor dissipation.

PTC Thermistors

Thermistor based protection systems are intended to recover once the overload is removed. During the ac line contact condition the rms current, I_{GEN}, flowing through

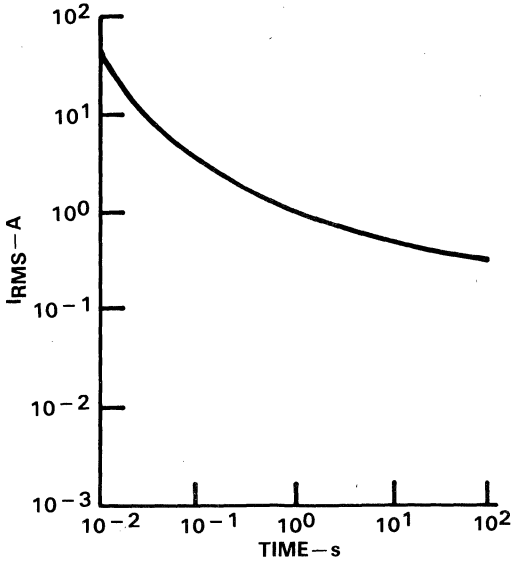


Figure 16. Typical Fusing Characteristic

the thermistor causes heating. When the PTC temperature rises to a critical "switch" temperature, its dynamic resistance starts to increase dramatically as shown in Figure 17 (often four to seven orders of magnitude) reducing I_{GEN}. Finally an equilibrium is reached where the $I_{GEN}^2 R_{PTC}$ losses are just sufficient to maintain the temperature which corresponds to that value of R_{PTC}. Depending on the overload current level, the reaction time of the PTC can vary from less than a second to several minutes. When the overload is removed, it may take several tens of seconds before the PTC resistance has dropped sufficiently to allow normal system operation.

It is usual for the PTCs to be supplied in pairs with guarantees on matching with age and overload for line balance considerations. It is important that the "switching" temperature is considerably above the maximum exchange ambient temperature to avoid premature "switching" and to lessen the effects of ambient temperature on the overload conditions. Self-heating due to the line dc and voltage drop considerations, leads to typical PTC 25°C resistance values from a few ohms to several hundred ohms.

Determination of the protection circuit operating point is complicated by the PTC's nonlinear resistance-current characteristic, shown in Figure 18. Initially, as the voltage applied to the PTC is gradually increased from zero, the PTC has a constant resistance which is shown by the vertical portion of the characteristic. The linear increase of current with increasing applied voltage continues until the PTC reaches its "switching" temperature and the resistance starts to increase. When this starts to happen, the current level, I_{MAX}, is given by:

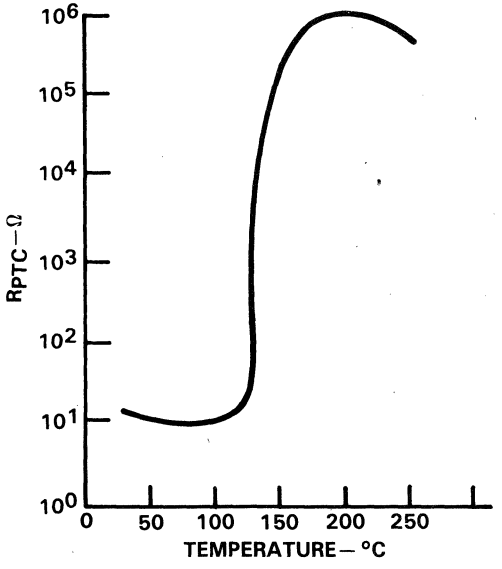


Figure 17. PTC Resistance Versus Temperature

$$I_{MAX} = \sqrt{\frac{T_C - T_{amb}}{R_{PTCamb} \times \theta_{PTC-amb}}}$$

where:

T_C = the "switching" temperature
T_{amb} = the ambient temperature
R_{PTCamb} = the initial PTC resistance
$\theta_{PTC-amb}$ = the PTC's thermal resistance to ambient.

On reaching this condition further increases in applied voltage result in decreasing current (although the power dissipated by the PTC increases slightly). This condition is shown by the sloping part of the characteristic in Figure 18. Very high continuously applied voltages can cause excessive temperatures to occur. Under these conditions the PTC's resistance starts to decrease with further increases in voltage which leads to a rapid increase in dissipated power. Such situations are potentially unstable and could lead to PTC failure.

Transient Suppressor

The major parameters of the TISP transient suppressors were discussed in the first two sections of this report. The major device losses will be caused by operation in the avalanche (zener) region and the saturated (on) condition. The TISP1XX family has a diode clipping characteristic for positive wire-to-ground voltages which maximizes the positive half cycles in the series protector. This enhances the series protector operation when compared with the symmetrical TISP2XX and TISP3XX families, which will inhibit current flow until the avalanche level, V_Z is exceeded.

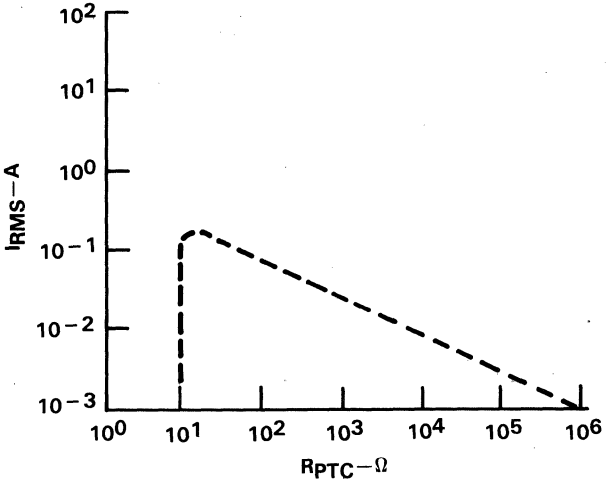


Figure 18. PTC AC Resistance Locus Versus Temperature

As far as the transient suppressor heating is concerned, the junction temperature rise will be governed by the chip's thermal capacity for periods below 10 ms, by the substantial TO-220 copper-tab thermal capacity (about 1 Joule/°C) for periods in the 10 s range, and finally by the junction-to-ambient thermal resistance over much longer periods (typically 50°C/W without an external heatsink).

AC Generator

Test specifications generally call up single phase type voltage generators with $0 < V_{GEN} < 250$ V (rms) and source impedances of $4 < R_{GEN} < 2000\ \Omega$. Worst case short circuit current capability is in the range of 6 A to 15 A (rms).

Graphical Analysis

A first pass analysis of the system operating conditions can be made graphically. This will establish the major system parameters and identify sets of conditions warranting more intensive examination. The analysis is simplified by combining the generator source resistance, R_{GEN}, and the series protector resistance together as a single resistance, R_S If fuse protection is used the few extra ohms is only significant at very low values of generator resistance (unless the fuse blows, of course). PTCs however can increase the net resistance, R_S, considerably, sometimes to hundreds of kilohms when heated. Figure 19 shows how the test generator can be considered as a load line, of slope R_S, drawn from a sinusoidally moving point on the horizontal axis of the symmetrical suppressor characteristic, which corresponds to the instantaneous value of generator voltage. For clarity, only the positive quadrant of the characteristic is shown. Specific voltage levels A, B, C, and D, are highlighted where the suppressor operation changes or values are maximum.

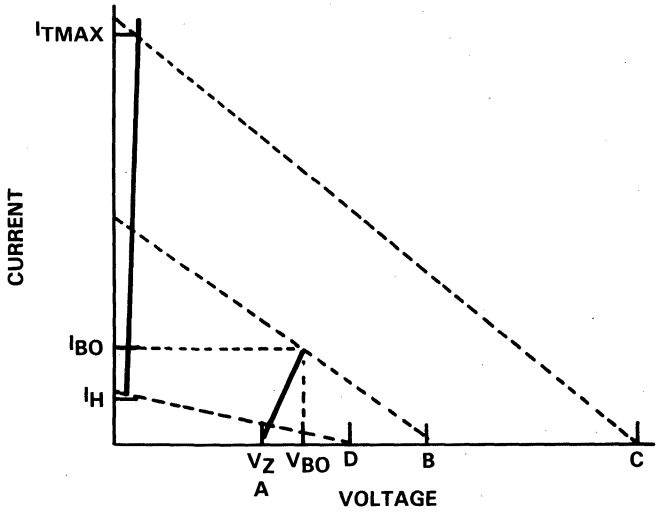


Figure 19. Voltage Generator Load Line and Waveforms

The suppressor starts to clip, causing current flow, when the instantaneous value of generator voltage, denoted by the lower case letters v_{gen}, reaches V_Z at point A.

When point B is reached breakover occurs and the instantaneous value of the generator voltage, v_{gen}, is:

$$v_{gen} = V_{BO} + I_{BO} \times R_S$$

where V_{BO} and I_{BO} are the suppressor's breakover voltage and current.

For a given value of rms generator voltage, V_{GEN}, the maximum value of source resistance, R_{SCMAX}, which will just initiate breakover is given by:

$$R_{SCMAX} = \frac{V_{GEN}\sqrt{2} - V_{BO}}{I_{BO}}$$

In operation, as the suppressor warms up, the breakover current, I_{BO} will decrease, causing the critical value of source resistance, R_{SCMAX}, to increase. This can lead to situations where the suppressor initially only avalanches rather than triggering due to $R_S > R_{SCMAX}$, resulting in a high suppressor power dissipation but a low rms current. As the suppressor warms up, the decrease in breakover current, I_{BO}, allows the original value of source resistance to initiate triggering. The mean dissipation in the suppressor then drops substantially but the rms current greatly increases, enhancing the potential operation of the series protection. Because of this, the possible rms current range is not a continous spectrum but has a gap between the avalanche and the crowbar modes of operation. This aspect is further considered in the Analysis of Fuse Protected Systems subsection.

In the "on" condition for TISP2XX and TISP3XX devices and for the TISP1XX diode operation, the peak value of suppressor current, I_{TMAX}, caused by the peak value of generator voltage at C will be approximately given by:

$$I_{MAX} = \frac{V_{GEN}\sqrt{2}}{R_S}$$

Point D illustrates the condition where the load line intersects the avalanche characteristic as the holding current is reached and, once delatching occurs, the suppressor clamps for the second time in that half cycle. If the "on" voltage of the suppressor at the holding current, I_H, is V_{TH} then the critical value of source resistance, R_{SZ}, for this to happen is:

$$R_{SZ} = \frac{V_Z - V_{TH}}{I_H}$$

Usually, in practice, this condition only occurs over a narrow range of generator values. More typically the unlatching point is reached when the instantaneous generator voltage is below the avalanche voltage, V_Z, and hence a second period of avalanche conduction does not occur.

RMS Generator Current

Because the protection system is nonlinear and temperature sensitive, the calculation or measurement of rms current and power is not straightforward. Based on the above analysis it is possible to to devise a simple computer simulation of the protection system. This model can be used to establish the full range of operating conditions with practical measurements as verification checks.

In the practical tests, true rms meters (rather than those types which scale peak or mean values) should be used. They should have a wide frequency response and large peak-to-rms capability to avoid overload inaccuracies. The rms current due to thermal effects in the protection elements often rapidly changes with time, and some form of data logging system greatly aids the analysis of the series element operating conditions. Oscilloscopes which permit the multiplication of the instantaneous suppressor voltage and current can be used to determine the dissipation levels. Accurate zeroing of the signals is very important to avoid substantial errors because usually one large quantity is multiplied by a much smaller one. In the avalanche region dissipation can be the product of a high voltage and a small current, while in the saturated condition it is the product of a low voltage and a typically high current.

System Effects of Generator Peak Voltage Amplitude

This subsection considers the system effects as the generator voltage amplitude is varied from below the transient suppressor avalanche voltage, V_Z, to the maximum available. Only the wire-to-ground test condition will be discussed but the same general principles, appropriately modified to comprehend the suppressor A-B characteristics, can be applied to the wire- to-wire situation. The discussion will concentrate on the latest generation of "transformerless" SLICs because they are the most susceptible to failure under ac line contact.

$\sqrt{2} \times V_{GEN} < V_Z$, TISP2XX and TISP3XX Families

Under these conditions the transient suppressor will not be exercised at all, but the output stage of the SLIC may be if connected to the line at that time. Although many of the specifications are not definitive about the SLIC condition during this test, it would be reasonable to examine the situation when the SLIC is in an active-state driving the appropriate line current into a simulated line impedance to comprehend any potential service problems.

The reaction of the SLIC to this condition strongly depends on the design implementation. Often there will be several feedback loops employed to stabilize operating conditions and minimize dissipation. One scenario could be the SLIC control system would interpret the ac line contact as a common mode signal which it would try to counter by driving an antiphase current.

Another possibility, particularly for unidirectional systems which do not have a sink and source capability on each wire, is that the control loops would be totally overloaded, leading to the output stage switching and driving high peak currents into

the test generator. Both these conditions could lead to abnormally high dissipation in the SLIC output section, leading to device failure. Obviously some form of thermal shutdown incorporated in the SLIC design would guard against this.

The average voltage from the generator is zero and some SLIC loops may treat this test as a resistive load (= R_S) to ground. This condition could then be reasonably safe because wire shorts to ground obviously have to be considered in any SLIC design.

The performance of the system under these conditions is purely a function of the SLIC implementation. It is doubtful that the SLIC will produce rms currents high enough to cause the series protection to operate.

$\sqrt{2} \times V_{GEN} < V_Z$ TISP1XX Family

The TISP1XX family has a diode characteristic for positive voltages. Thus most of the current from the generator during the positive half cycle will be shunted to ground. If the SLIC is capable of sinking current from the generator, the ac voltage from the generator system will be displaced by a dc voltage of $I_{LINE} \times R_{GEN}$ in the negative direction. Hence the positive voltage period will be made shorter than the negative voltage period and the TISP1XX diode will conduct for less than 180° over a complete cycle.

Similar comments on the SLIC operation as in the previous subsection apply, but in this case there is a real chance the series protection elements will operate for source resistances under several hundred ohms, due to the higher rms current caused by the diode clipping.

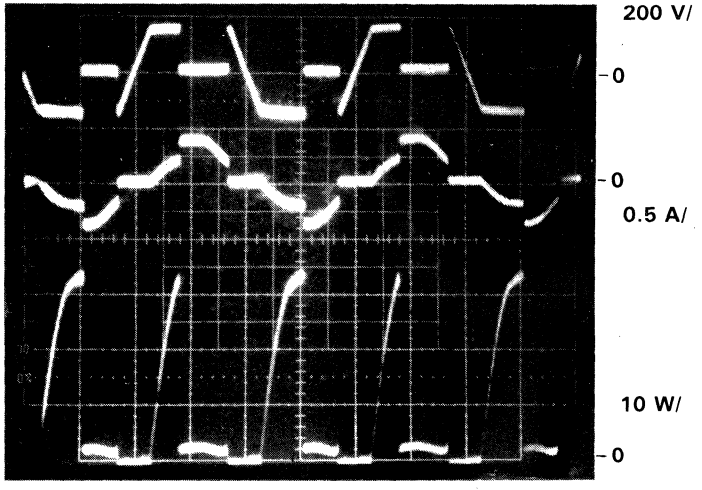


Figure 20. TISP2XX and TISP3XX AC Line Contact Conditions

$\sqrt{2} \times V_{GEN} > V_Z$, TISP2XX and TISP3XX Families

This situation will result in suppressor conduction if the SLIC is not active. As discussed earlier the reaction of an active SLIC depends on the implementation, but typically it can be expected to introduce asymmetry into the positive and negative clipping of the ac waveform. For simplicity the following assumes the SLIC is inactive.

In this condition, Figure 20, the suppressor will definitely avalanche and depending on the generator values, it may trigger "on" (See Graphical Analysis subsection).

$\sqrt{2} \times V_{GEN} > V_Z$, TISP1XX Family

In this condition, Figure 21, the positive voltage excursion will be clipped as before when the voltage was less than V_Z. Also the suppressor will avalanche in the negative direction and depending on the generator values, it may trigger "on" (See Graphical Analysis subsection).

Analysis of Fuse Protected Systems

Figure 22 reproduces the fusing characteristic from Figure 16. In this example a fuse resistance of 6 Ω is assumed, a voltage generator range of 0 to 250 V rms, and generator resistance of 4 Ω and 2000 Ω. The TISP transient suppressor rms current capability will vary with the device type, dissipation mode, test generator, circuit configuration used, temperature, and test time. Semiconductor ratings are usually well controlled but obviously the quoted values will be worst case. The suppressor dissipation curves shown dotted are based on a 150 V symmetrical type device. When the source resistance, R_S, is very low the main dissipation is from "on" condition

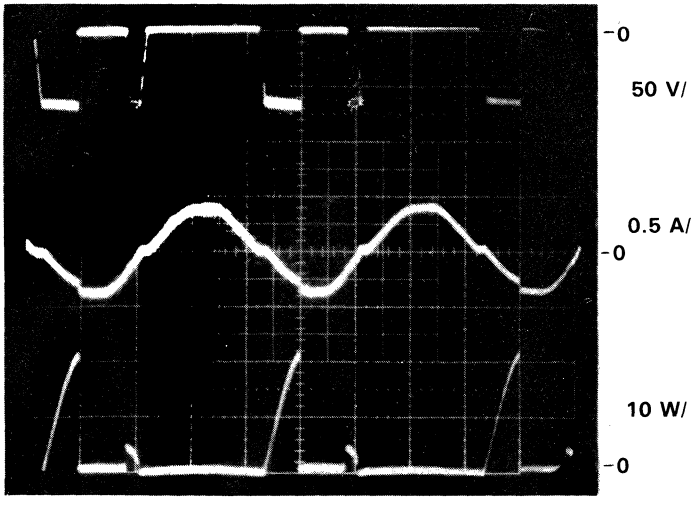


Figure 21. TISP1XX AC Line Contact Conditions

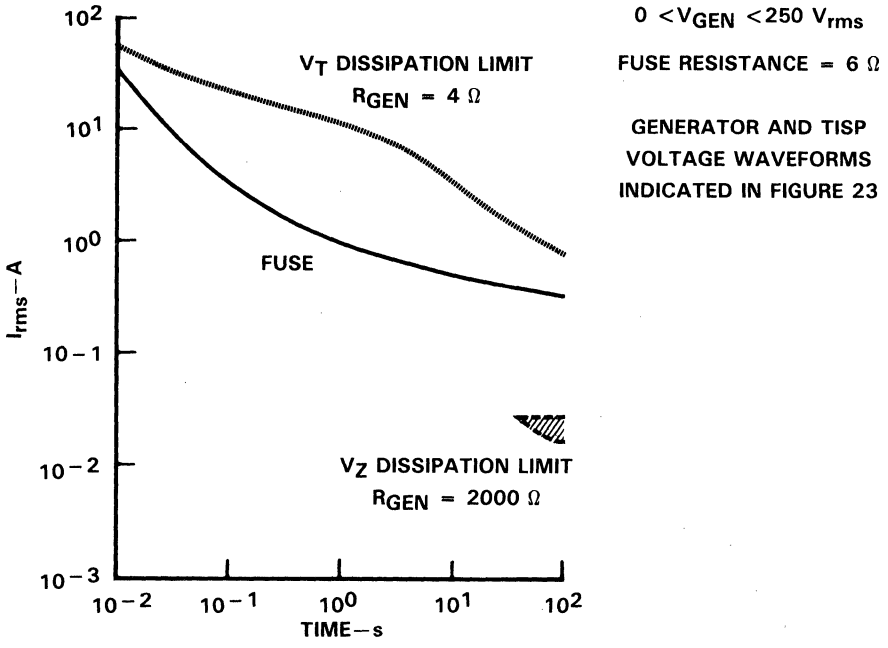


Figure 22. RMS Current Versus Time for Fuse Protection

losses with very little loss from the avalanche mode. Hence this curve can be regarded as generalized for the specified suppressor.

Due to the reasons explained in the Graphical Analysis subsection, high source resistances will greatly restrict the current levels and possibly give excessive dissipation in the avalanche mode. The avalanche dissipation area for this case will be highly specific to generator values and will occur only quite some time after the start of the test. It is also unlikely in this case that a second curve due to "on" condition dissipation limits would be possible due to the very restricted current flow leading to minimal saturated dissipation.

The 4-Ω generator case causes very large currents to flow because the suppressor can easily trigger. As indicated in Figure 23, the current varies between 8 A rms and 24 A rms with the specified generator voltage range. For this range of currents the fusing current is always below the suppressor saturated dissipation limit curve, and the fuse will operate in under 150 ms.

The 2000-Ω generator case severely limits the current. As indicated in Figure 23, a current of 75 mA to 120 mA flows when only avalanching occurs. At higher voltages the suppressor dissipates power in the avalanche and saturated modes. Medium voltages will only dissipate power in the avalanche mode. The worst case power dissipation occurs when the peak current is just below the breakover level. In the short term even this level of power dissipation is acceptable, but often this rms current is

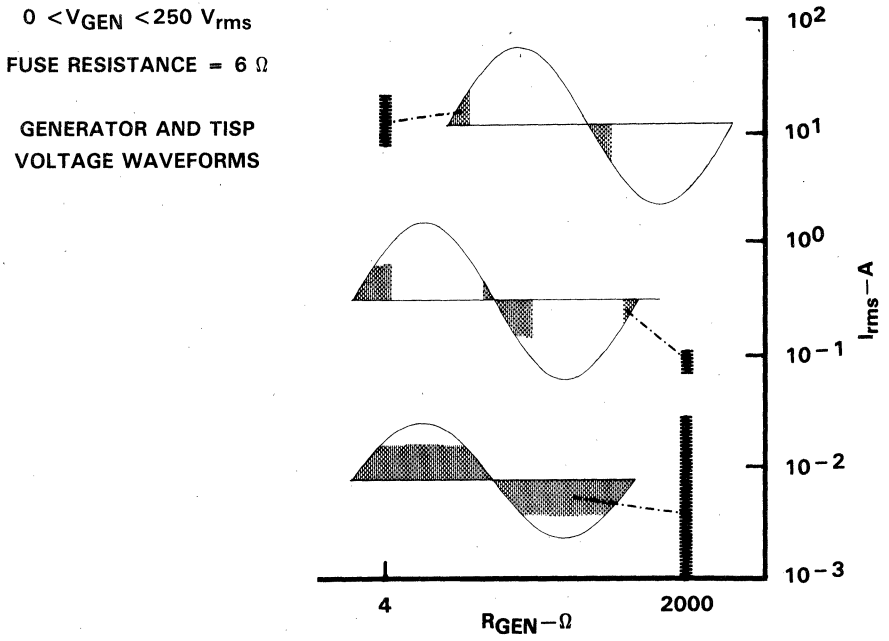


Figure 23. RMS Current Versus Generator Resistance

insufficient to guarantee fusing. Hence in the longer term (if the generator application is of a continuous nature) then the suppressor could overheat and possibly fail. The time scale for this to happen will be governed by the thermal package-to-ambient parameters and the dissipation level. This creates the " ⌒ " shaped potential failure area in Figure 22 for periods greater than 10 s and the specified generator levels.

This has been a very simplistic analysis of the conditions. Fusing curves are often based on dc tests, however, because the transient suppressor parameters are temperature dependent (principally I_{BO} and I_H) the rms system current will be changing with time which will modify the fusing characteristic. In addition fuses, being thermal in nature, will tend to fail at specific points in the ac cycle (Reference 1). Another factor neglected is whether the SLIC is shunting the suppressor and passing additional current through the fuse.

Analysis of PTC Protected Systems

Figure 24 reproduces the PTC characteristic given in Figure 18. Also shown are the rms currents which would flow when a 150 V symmetrical suppressor is used. Curves are shown for minimum, 4 Ω, and maximum, 2000 Ω, generator resistance, R_{GEN} and for two suppressor junction temperatures. The reason for showing device curves for high and low temperatures is that some idea of the working point trajectory can be gained.

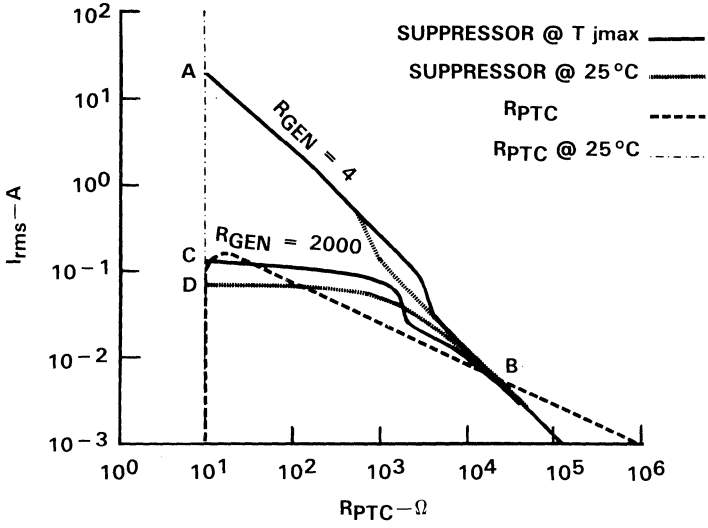


Figure 24. RMS Current Versus PTC Resistance

Initially the 4 Ω generator resistance combines with the unheated 10 Ω PTC resistance to give the working point A. As the PTC heats up due to the high current a stable working point is achieved at B. Initially the suppressor heavily saturates but as the resistance increases a temperature sensitive point is reached when saturation stops. This condition is shown by the step in the suppressor's current characteristic. Although the rms current drops considerably at this point there is still thermal inequality in the PTC for its dissipated power which is only removed when point B is reached.

When the generator resistance is 2000 Ω the initial working point is D. This condition is stable for the PTC but the suppressor power loss curves, shown in Figure 25, indicate excessive long term dissipation. As the suppressor warms up, breakover occurs, and dissipation is reduced. A working point which is just stable occurs at C. In practice, due to thermal capacity differences and thermal coupling, the final working point is more likely to be at B.

Although operating end points can be predicted using this method, computer simulation or practical testing is necessary to ensure the devices do not fail during the intermediate period.

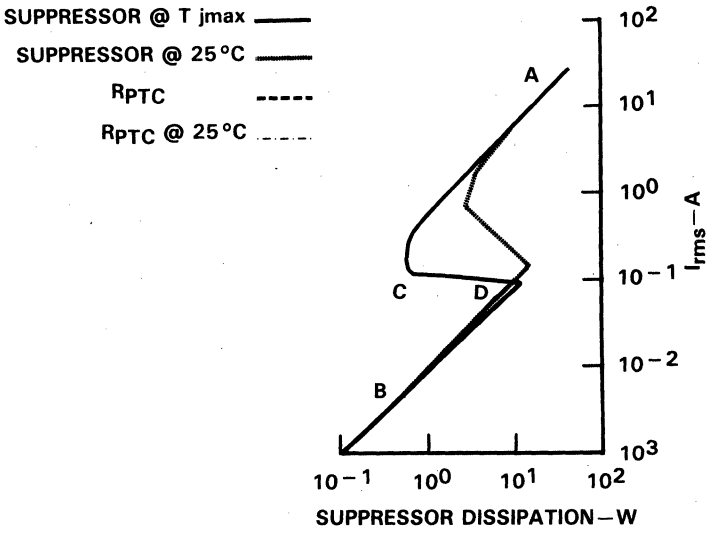


Figure 25. RMS Current Versus Average Suppressor Power

Summary

The TISP transient suppressors provide telephone designers with a new cost-effective way to protect the increasing number of semiconductors, particularly integrated circuits, in their equipment. Specifications for the main dc parameters I_D, I_H, I_{BO} and V_Z can be determined from system parameters:

1. on-state and off-state line currents
2. on-state line current variation with temperature
3. maximum values of battery and ringing voltages
4. maximum value of test voltages
5. maximum negative voltage voltage of the SLIC.

The example values used in this report represent only typical system requirements.

The basic evaluation techniques for ac line contact shown in this report will identify critical areas for further study. The effects on the system of other shunt elements have been ignored to simplify the presentation at the risk of inaccuracy at high values of source resistance, R_S. Some of the ac data used is not normally specified in this form by the industry, although it is available in other forms. With the increasing popularity of crowbar suppressors, it is hoped that manufacturers will start to provide data in a form compatible with computer analysis and design.

References

1. Electric Fuses, A. Wright & P. G. Newbery, Peter Peregrinus Ltd.
2. PTC materials technology, 1955-1980, B. M. Kulwicki, Advances in Ceramics, Volume 1, Grain Boundary Phenomena in Electronic Ceramics, 1981, The American Ceramic Society.

Designing with TCM1500A Tone Ringer Drivers

TEXAS INSTRUMENTS

Contents

List of Illustrations

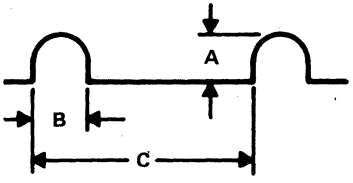
Introduction

TI's patented BIDFET† process has allowed the combination of high-voltage circuitry to handle signals of up to 150 V and low voltage CMOS technology for dense logic, thus enabling Texas Instruments to offer a series of monolithic ICs that will detect the ring signal on a telephone line. The purpose of this report is to explore the use of these circuits in different applications and understand various technical issues.

Features

Some of the common features of the TCM1501A, TCM1506A, TCM1512A and TCM1520A include:

1. Lightning Protection: When used in series with the proper resistor and capacitor, these devices will withstand 1500 V/200 μs transients.
2. Antitapping: These devices are designed to ingnore high voltage transients generated by dial pulses from a parallel phone, as shown in Figure 1.



A	B	C
800 V	2 ms	50 ms
200 V	10 ms	60 ms

Figure 1. Dial Pulse Transients

3. High Standby Impedance: In the absence of a ring signal, these devices are powered down and present a shunt impedance of greater than 100 kΩ (typically 1 MΩ).
4. High Voltage Output: The output drive capability is up to 40 V peak to peak for the TCM1501A, TCM1506A and TCM1512A. The TCM1520A has TTL/MOS compatible output.
5. The ICs require a minimum number of external components.

†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip—patented process.

Ringer Functional Description

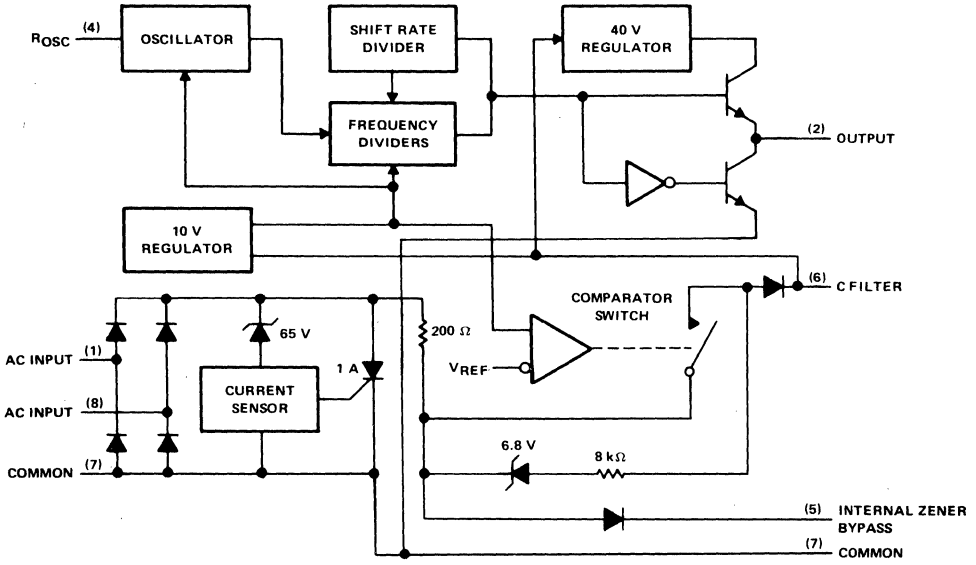
A block diagram schematic of the ringer series and 1520A ring detector is shown in Figure 2(a) and (b). The network formed by C_1 (the dc blocking capacitor), 2.2-kΩ current limiting resistor and the full wave bridge rectifier supply the IC power from the phone lines. The rectified ac ring signal is filtered by an external 10 μF/100-V capacitor connected between pin 6 and 7. The value of C_1 will determine the minimum input voltage. Value of C_1 along with the filter capacitor also affects the turn-on time of the IC. The filter capacitor value with the internal IC circuitry is used to suppress dial tapping. Tapping is a false ringing of the bell to pulses on the phone line from rotary dials or pulse dialing ICs.

The IC is kept off (in standby) until the incoming signal across pin 1 and 8 reaches a peak voltage of approximately 8.9 V. This threshold can be lowered by externally connecting pin 5 with a lower value zener and resistor to pin 6. Since the IC is kept off below 8.9 V, the IC offers a standby impedance of approximately 1 MΩ to 3 V rms signals, thus offering minimum distortion to DTMF or voice signals. However, when the voltage across the IC pin 1 and 8 reaches a threshold of approximately 17 V, an internal switch is closed which bypasses the 6.8-V zener, thus allowing maximum energy transfer to the load.

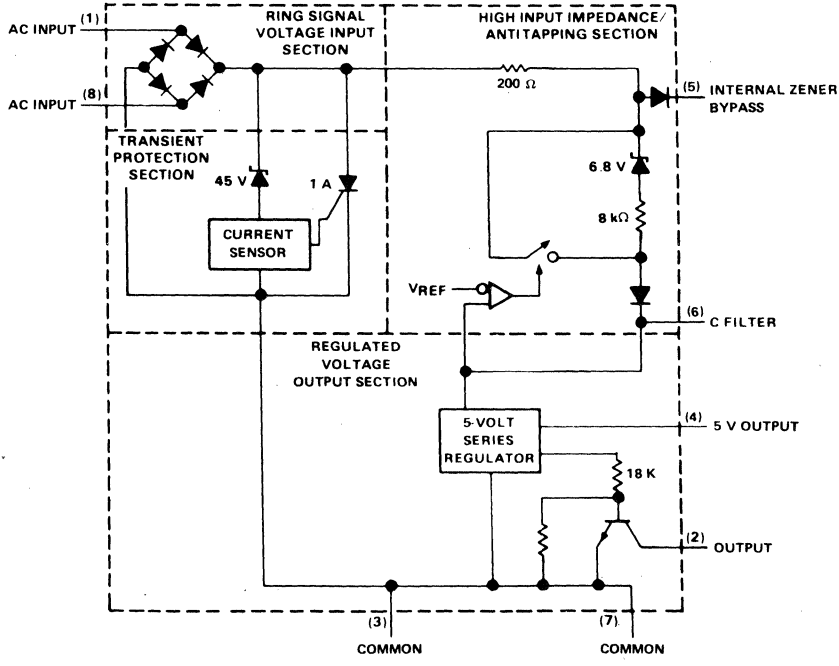
The TCM1501A, TCM1506A, and TCM1512A have built-in 10-V and 40-V regulators. The 10-V regulator drives the CMOS oscillator and the audio generator section, while the 40-V regulator drives the push-pull output.

The TCM1520A ring detector has a 5-V regulator only whose output is brought out to pin 4.

The TCM1501A through TCM1512A series and TCM1520A have a built-in transient protection circuitry which consists of a high current SCR triggered by a sense circuit through a 65-V or 45-V zener. The external 2.2-kΩ resistor is necessary to dissipate the energy when SCR is turned on.



(a) TCM1501A, TCM1506A, TCM1512A



(b) TCM1520A

Figure 2. Functional Block Diagram

Pin Configuration

Pin configurations for this series of monolithic ICs are depicted in Figures 3 and 4. Pin functions are listed in Table 1.

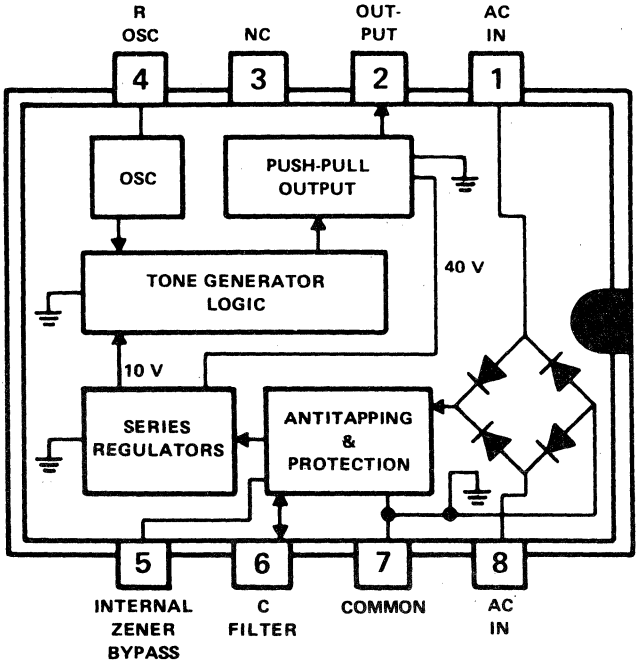


Figure 3. TCM1501A/TCM1506A/TCM1512A Pin Configuration

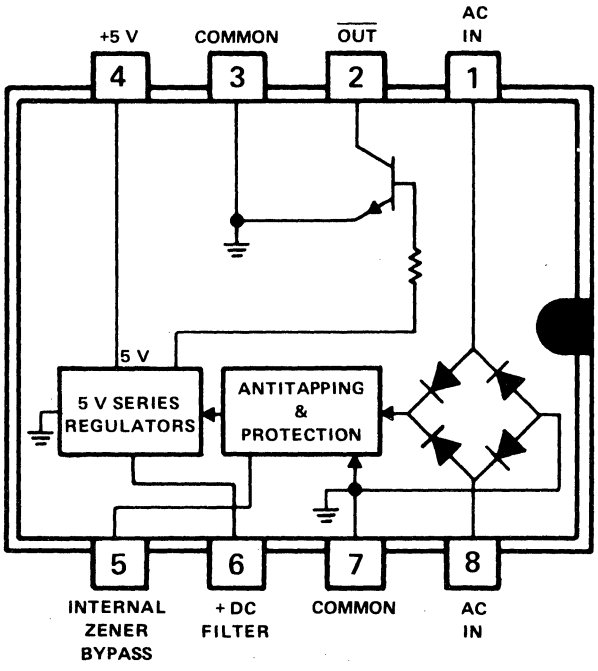


Figure 4. TCM1520A Ring Detector Pin Configuration

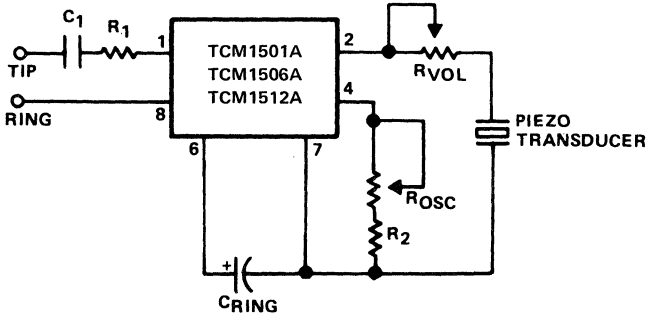


Figure 5. Driving a Piezo Transducer

Table 1. Pin Functions

Pin Number	Function	
1, 8	AC INPUT	Internally limited to 65 V maximum
2	OUTPUT	40 V P-P (TCM1501A, TCM1506A, TCM1512A) Low Active Open Collector (TCM1520)
3	NC COMMON	(TCM1501A, TCM1506A, TCM1512A) (TCM1520A)
4	R_{osc} +5 V	Resistor between this pin and ground will adjust oscillator frequency (TCM1501A, TCM1506A, TCM1512A) Five volt dc output (TCM1520A)
5	Internal Zener Bypass	Normally NC externally — a resistor between this pin and pin 6 will lower threshold voltage of ac input that will generate an output.
6	C FILTER	Capacitor to GND stores charge until voltage threshold is surpassed to generate output.
7	COMMON	

Ringer Output Frequency Options

TCM1501A through TCM1512A devices output a square wave that warbles between two audible frequencies. The warble rate and the center frequency are determined by a mask option at the time of manufacturing. An external resistor selects this center frequency. Table 2 lists the various standard ring detector drivers, the center frequency and warble ratio options.

Table 2. Ringer Output Frequency Options

Part No.	Rectifier Type	Output Type	Nominal Output Center Frequency (Hz)	Warble Ratio	Warble Frequency (Hz)
TCM1501A	Full Wave Bridge	Single Ended	2000	5:4	7.8
TCM1506A	Full Wave Bridge	Single Ended	500	5:4	7.8
TCM1512A	Full Wave Bridge	Single Ended	1250	8:7	9.8
TCM1520A	Full Wave Bridge	TTL/MOS Logic	N/A	N/A	N/A

Types of Transducers

All of these devices will drive either a piezoelectric transducer or a speaker except the TCM1520A whose output is a MOS/TTL compatible level.

Maximum energy is delivered to the transducer if the driver output impedance of 4 kΩ is matched to the transducer. For a speaker, an audio transformer is generally required. The choice of piezo device is complicated by the fact that the impedance changes with frequency. Further information on transducer selection may be found in the section on "Ringer Equivalency Number" and Appendixes A and B.

Telephone Applications

Driving a Piezo Transducer

The most obvious application for this device is to detect the ring signal and drive the ringer in an electronic telephone. Figure 5 is the schematic diagram for such an application.

The function and value of each component in Figure 5 is as follows:

C_1 This is a dc blocking capacitor in series with the telephone line. It must pass the ring signal which can be up to 150 V rms (212 V_{PK}). The value of this capacitor should be as small as possible and still pass enough energy to properly drive the ringer. A common choice for this capacitor would be 0.47 μF, 250 V.

R_1 This resistor is required to dissipate power resulting from a high voltage transient. During a voltage transient (up to 1500 V for 200 μs) the ring detector driver becomes a virtual short, thus shunting the surge of current to ground. This surge of current can be as high as 0.9 A provided the voltage is dropped across R_1. The value should be 2.2 kΩ, ¼ W.

C_{RING} This capacitor is used to store energy from the ring signal and when pin 1 and 8 input of about 17 V is reached, the circuit will issue the ring signal. The lower limit of the capacitor value is determined by the time constant required to ignore bell-tapping, while an upper limit is set by the ring turn-on time. After the capacitor reaches its threshold, it continues to charge to approximately 65 V (45 V on TCM1520A). A suitable value for this capacitor is 10 μF, 100 V. This capacitor will also determine the turn-on and turn-off time of the ringer. Should a sharper cut-off of the ring signal be desired, a suggested circuit is shown in Figure 6.

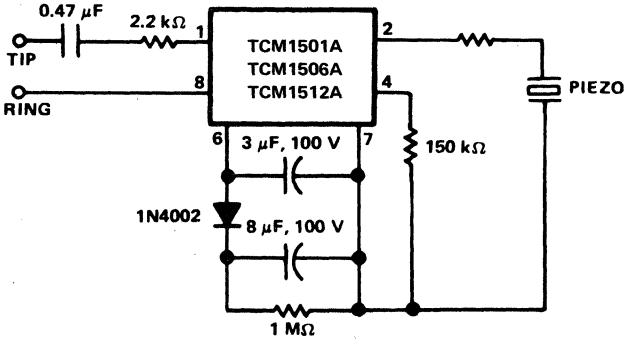


Figure 6. Optional Circuit (for Sharp Cut-Off Ring Signal)

R_{OSC} This potentiometer allows adjustment of the frequency of the ring signal at pin 2. To allow adjustment over the entire frequency range, a good value is 100 kΩ (assuming R_2 = 100 kΩ).

R_2 This resistor is present to limit the minimum resistance between pin 4 and ground. A good choice is 100 kΩ.

R_{VOL} This potentiometer allows volume adjustment. A 250-kΩ potentiometer will allow adjustment from full loud to barely audible. If volume adjustment is not required, instead of potentiometer, a fixed resistor of 0.5 kΩ to 2 kΩ may be used.

PIEZO For a telephone application such as this, the impedance of the transducer must be approximately 4 kΩ to best match the output of the detector/driver. One choice that meets this requirement is a Kyocera KBS-27DB-3A. (See further discussion in section on Ringer Equivalency Number.)

Driving a Speaker

The circuit in Figure 7 will also drive a speaker. The only difference is, that a speaker which is normally 8 Ω should be matched to the 4-kΩ output with a transformer. Figure 8 shows how the speaker should be connected.

The values and functions of each component in Figure 8 is as follows:

R_{VOL} This potentiometer provides volume control

C_2 This capacitor blocks dc and should have a low impedance to the detector driver output frequencies. A suitable value is 0.1 μF, 40 V.

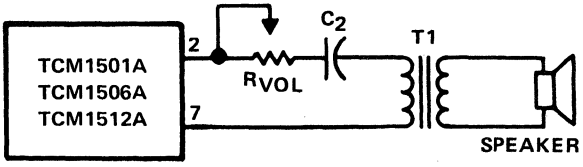


Figure 7. Driving a Speaker

Output Characteristics

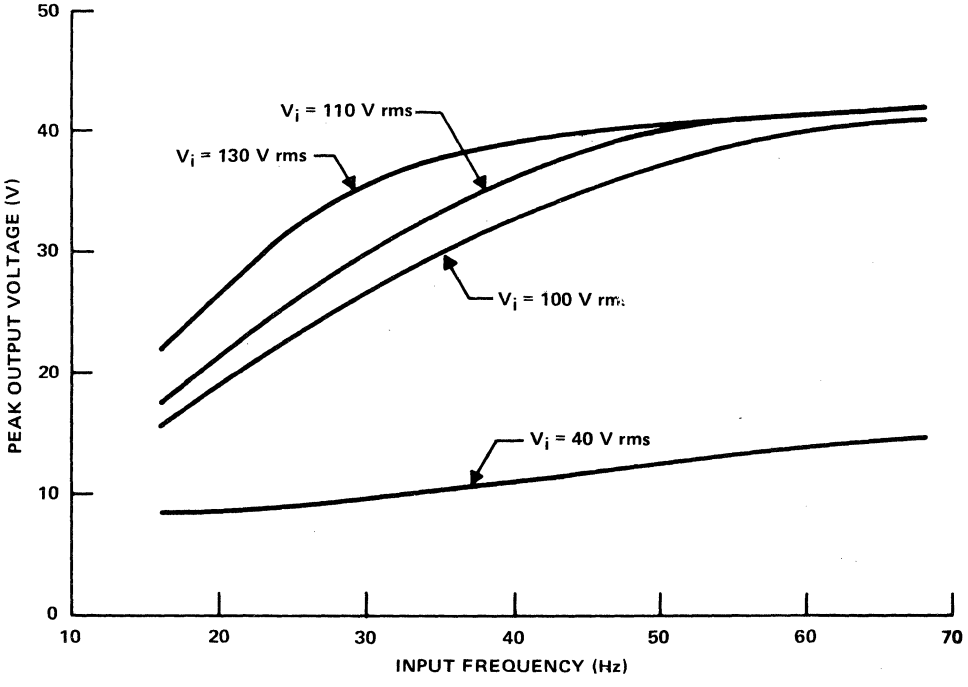
The output voltage and the output power curves of TCM1501A ringer as a function of input frequency at various input voltages are shown in Figures 8 (a) and (b), respectively. The device is capable of putting out well over 80 mW into a 4-kΩ load at input signal greater than 110 V and frequency of 60 Hz.

Ringer Equivalency Number (REN)

The REN of a ringer circuit is a number that reflects the minimum amount of impedance that is presented to the telephone line during ringing. A standard ringer is defined to be 8000 Ω and have a REN of 1. The following equation may be used to calculate the REN of a nonstandard ringer:

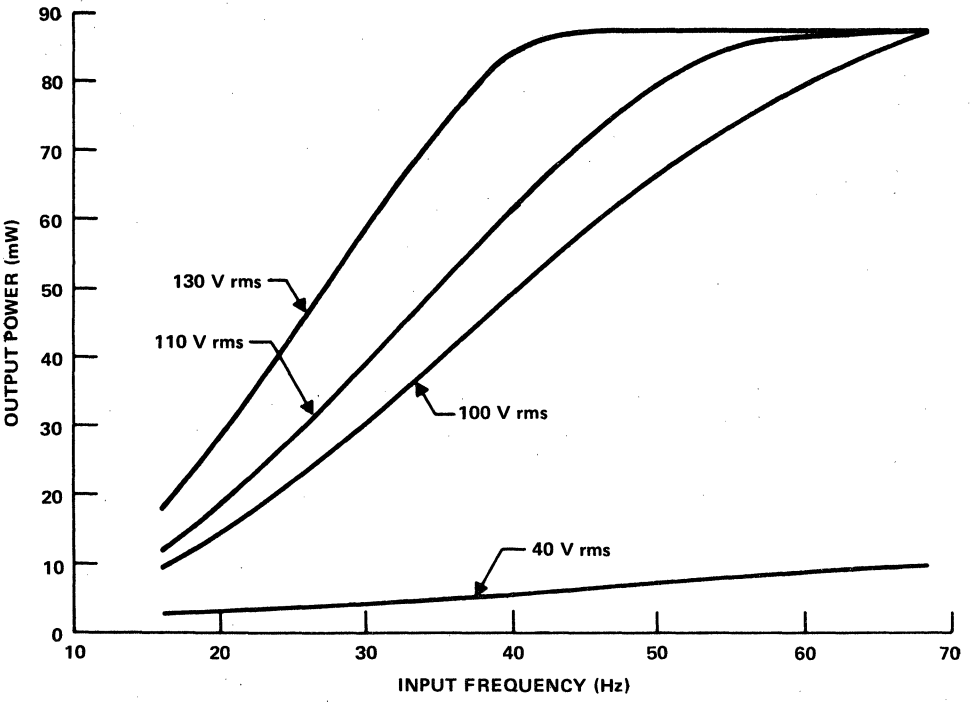
$$\text{REN} = \frac{8000}{|Z|}$$

where $|Z|$ is the magnitude of the impedance of the ringer circuit.



(a) Voltage Out with 4-kΩ Fixed Output Load

Figure 8. TCM1501A Output Characteristics



(b) Output Energy with 4-kΩ Fixed Output Load

Figure 8. TCM1501A Output Characteristics

To estimate the REN of ringer circuits utilizing one of the TCM1500 family ICs, the circuit in Figure 9 may be used. For purposes of simplifying the analysis of this circuit,

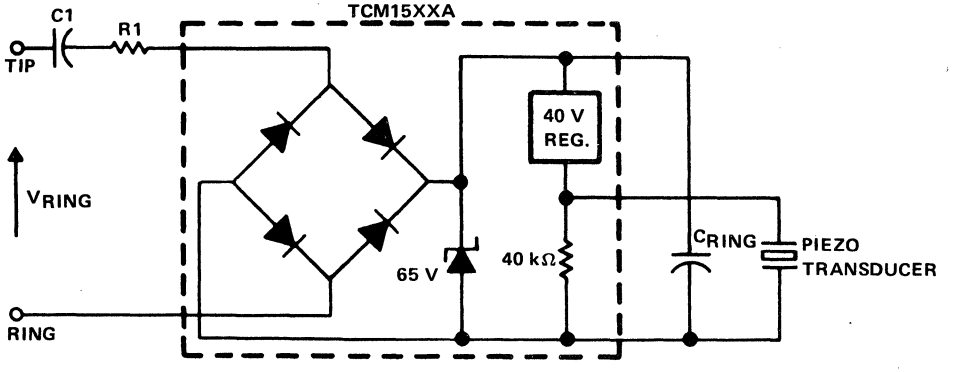


Figure 9. Equivalent Circuit for REN Analysis

the diodes in the bridge as well as the 65-V zener may be assumed ideal. Also, once C_{RING} is charged up, it is effectively out of the circuit as far as REN is concerned. The fact that the 65-V zener is parallel with the 40-kΩ resistance complicates things when the ringing voltage tries to exceed 65 V. The 40-kΩ resistance represents the power used by the CMOS logic circuitry and is so large compared to the impedance of the parallel load that it may be ignored. A further simplification of the equivalent circuit may be drawn as indicated in Figure 10. Notice that the load appears as a resistive impedance even though the piezo device is basically a capacitive device. This is due to the voltage regulators that supply the output drivers that drive the piezo device.

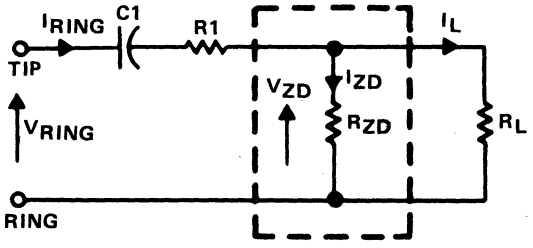


Figure 10. Simplified Ringer Equivalent Circuit

The REN analysis is as follows:

1. Assuming worst case values of Ringer Voltage (V_{RING}) and frequency (f_{ring}),
   let $V_{RING} = 150\ V_{rms}$ (so that zener is clamping)
   let $f_{ring} = 68$ Hz (Class B ringer per FCC part 68)
2. Known values are:
   $C_1 = 0.47\ \mu F$ $\quad R_1 = 2.2\ k\Omega$
   $R_L = 6\ k\Omega$ (from Kyocera impedance graph)
3. Calculate R_{ZD} (equivalent resistance of zener diode)

$$R_{ZD} = \frac{V_{ZD}}{I_{ZD}}$$

where $V_{ZD} = 65$ volts
and $I_{ZD} = I_{RING} - I_L$

$$\text{where } I_L = \frac{V_L}{R_L} = \frac{65}{6000} = 10.8\ (10^{-3})\ A$$

$$\text{and } I_{RING} = \frac{V_{C1} + V_{R1}}{Z_{C1} + Z_{R1}}$$

$$Z_{C1} = \frac{1}{j2\pi\ f_{RING}\ C} = -j4980\ \Omega$$

$$Z_{R1} = R_1 = 2200\ \Omega$$

$$V_{C1} + V_{R1} = 150 - 65 = 85 \text{ volts}$$

$$I_{RING} = \frac{85}{2200 - j4980} = \frac{85}{5444\ \angle -66.16^\circ}$$

$$= 15.6\ (10^{-3})\ \angle 66.16^\circ\ A$$

$$I_{ZD} = 15.6\ (10^{-3})\ \angle 66.16^\circ - 10.8\ (10^{-3})$$
$$= (6.30 + j\ 14.26 - 10.8)\ (10^{-3})$$
$$= (-4.5 + j\ 14.26)\ (10^{-3})$$
$$= 14.95\ (10^{-3})\ -\ \angle 72.48^\circ\ A$$

now since V_{ZD} and I_{ZD} are in phase (resistive), the angle may be dropped

$$R_{ZD} = \frac{65}{14.95\ (10^{-3})}$$

$$R_{ZD} = 4348\ \Omega$$

4. Calculate parallel equivalent for R_{ZD} and R_L

$$R_{ZD} \,||\, R_L = \frac{R_{ZD}\, R_L}{R_{ZD} + R_L} = \frac{(4348)(6000)}{4348 + 6000}$$
$$= 2521\ \Omega$$

5. Calculate overall equivalent impedance Z

$$Z = Z_{C1} + Z_{R1} + R_{ZD} \,||\, R_L$$
$$= -j4980 + 2200 + 2521$$
$$= -j4980 + 4721 = 6862\ \underline{/-46.71^\circ}\ \Omega$$

6. Calculate REN:

$$REN = \frac{8000}{|Z|} = \frac{8000}{6862}$$

$$REN = 1.165$$

It is important to note that only in the absolute worst case situation of 150 V rms, 68-Hz ring signal would the REN be as high as 1.165. If the ring signal is more tightly controlled, as in the case with most PBXs, the REN would typically be less than 0.5.

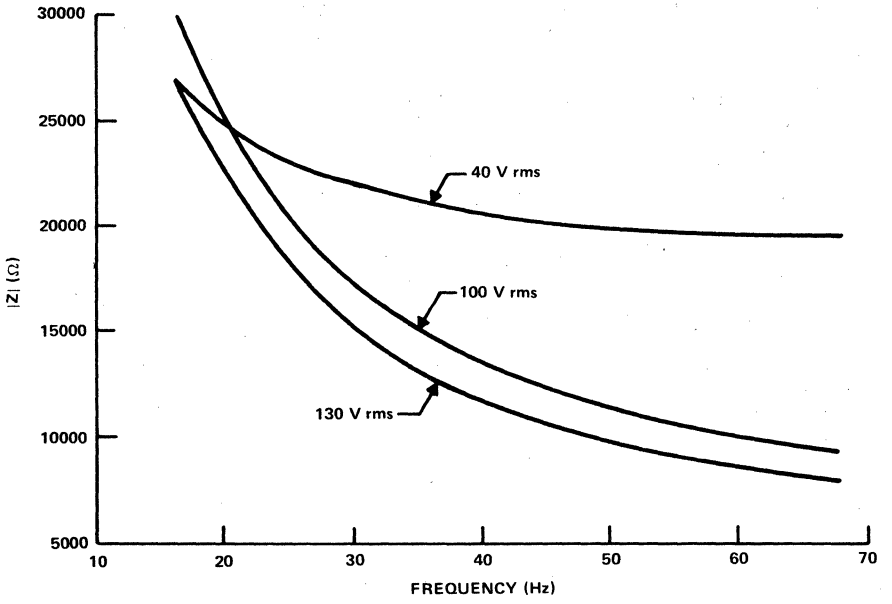
Figures 11(a) through 11(c) show respectively, the typical laboratory measurements for impedance vs frequency for the TCM1501A ringer with output open, output shorted and with Kyocera KBS-27D8 piezo transducer, taken at different voltages. Figure 11(d) shows the impedance variation of Kyocera Piezo KBS-27D8-3A with frequency. As is obvious, the impedance of TCM1501A ranges approximately from 8 kΩ to 30 kΩ and is fairly independent of the load connected to its output.

Tighter Frequency Control

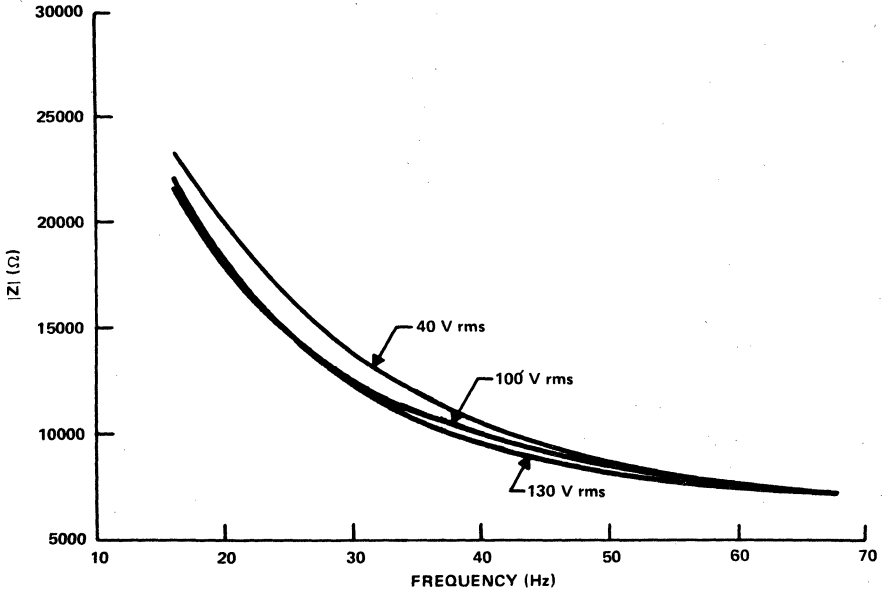
Due to normal process variations from one lot to another, the oscillator frequency can vary somewhat from the nominal values listed in Table 2. To obtain these center frequencies, the designer may either use a potentiometer as in the application in Figure 5, or use the applicable binned (standard) 1% resistor value as indicated in Table 3. The binned resistor will cause it to oscillate within ±5% of the nominal frequency. At a slight premium, TI will label the bin values if the user so chooses. If a fixed resistor is used to set frequency, it takes the place of both the R_{OSC} potentiometer and R_2.

Table 3. Binned (Standard) Resistor Values

Part No.	Binned Resistor Values (kΩ)
TCM1501A TCM1506A TCM1512A	130, 140, 150, 158, 165

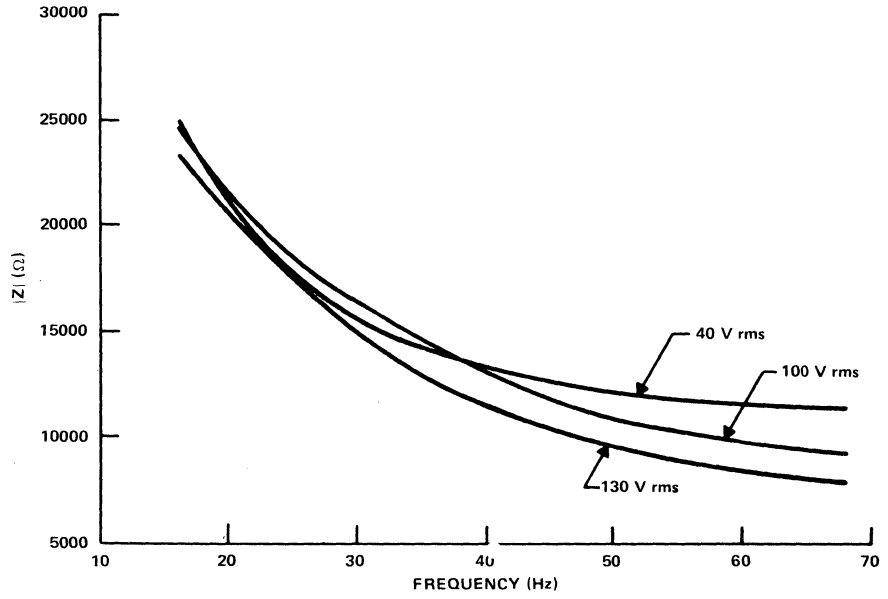


(a) Output Open

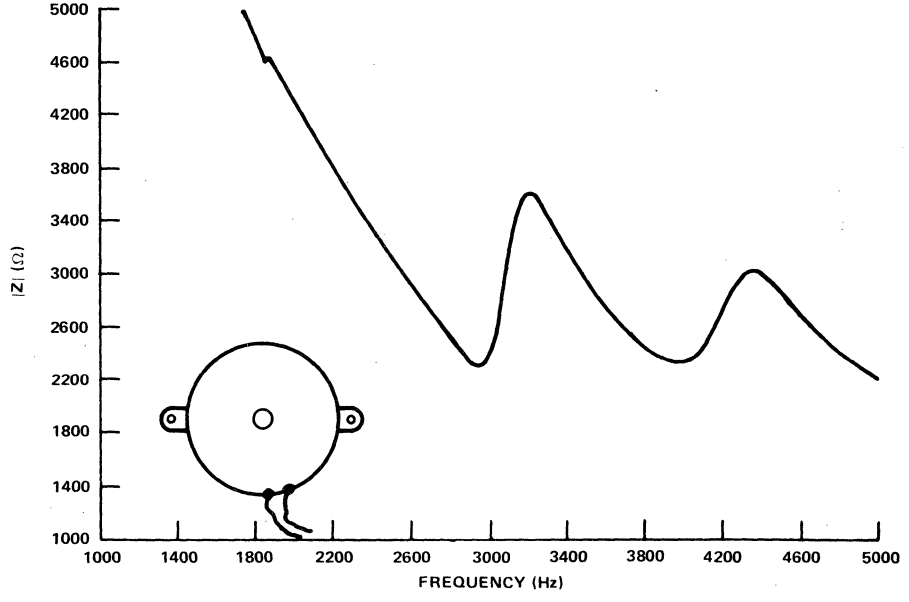


(b) Output Shorted

Figure 11. TCM1501A Laboratory Measurements — Impedance vs Frequency



(c) With Kyocera KBS-27-DB-3A Piezo



(d) Kyocera Piezo KBS-27DB-3A in Standalone Mode

Figure 11. (Cont'd.) Laboratory Measurements — Impedance vs Frequency

Additional Applications

Turning Ringer Circuit ON/OFF with a TTL Output

Figure 12 shows how an open-collector output of a TTL or STTL device may be used to disable the ring output of the TCM1512A. When the open-collector input goes low, the opto-isolator switches ON, placing a voltage on pin 4 that is sufficient to swamp-out the internal oscillator. While there are other means of shutting off the ringer, this is a low-voltage high-impedance method that provides isolation.

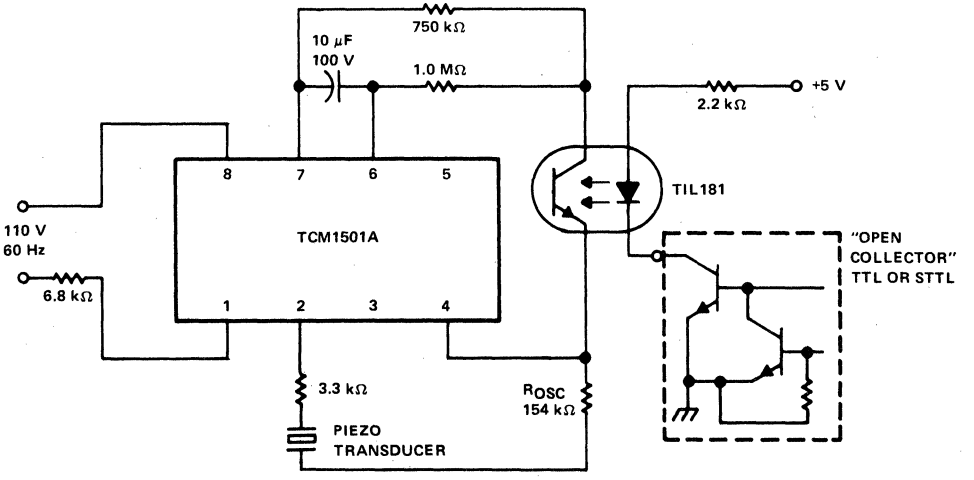


Figure 12. Controlling Ringer with a TTL Output

3 Interfacing the TCM1520A Ring Detector

The TCM1520A may be interfaced to allow either isolated or nonisolated supplies. Figure 13 shows a typical telephone application which uses an optocoupler to keep the phone lines isolated. When a ring signal is applied, the 10-μF capacitor charges until pin 1 and 8 passes the 17-V threshold, at which time pin 4 outputs + 5 V turning the optocoupler on. This causes the transisitor portion of the optocoupler to saturate, providing a low signal to the μP or logic block.

The drive capability of the TCM1520A is a function of the input Tip Ring voltage and frequency. Figure 14(a) shows the typical output voltage vs load curves at different input ring signals. Figure 14(b) shows the typical impedance vs frequency curves of TCM1520A at different input voltages.

Figure 15 illustrates one example of how to interface to the TCM1520A when isolation is not required. The 10-kΩ resistor is required only if the opposite sense of the output signal is desired.

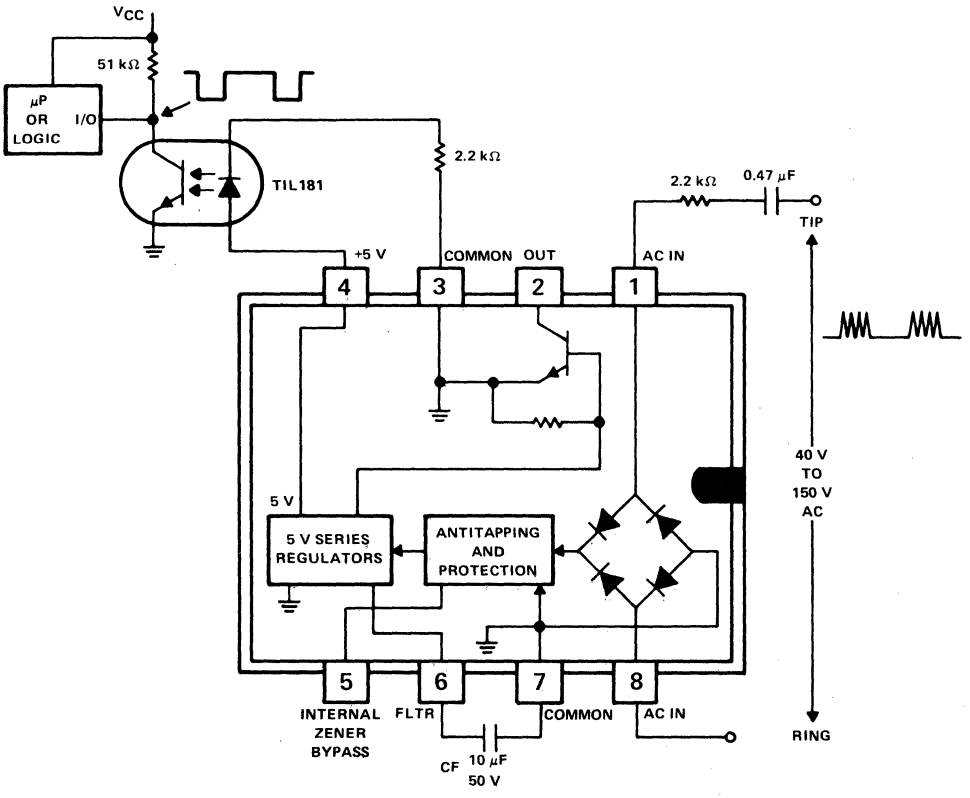
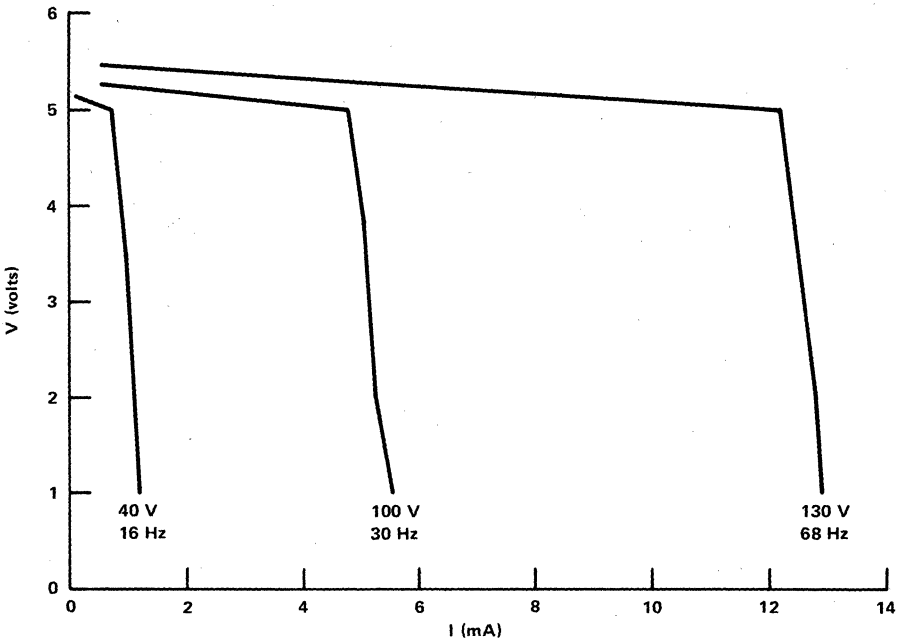


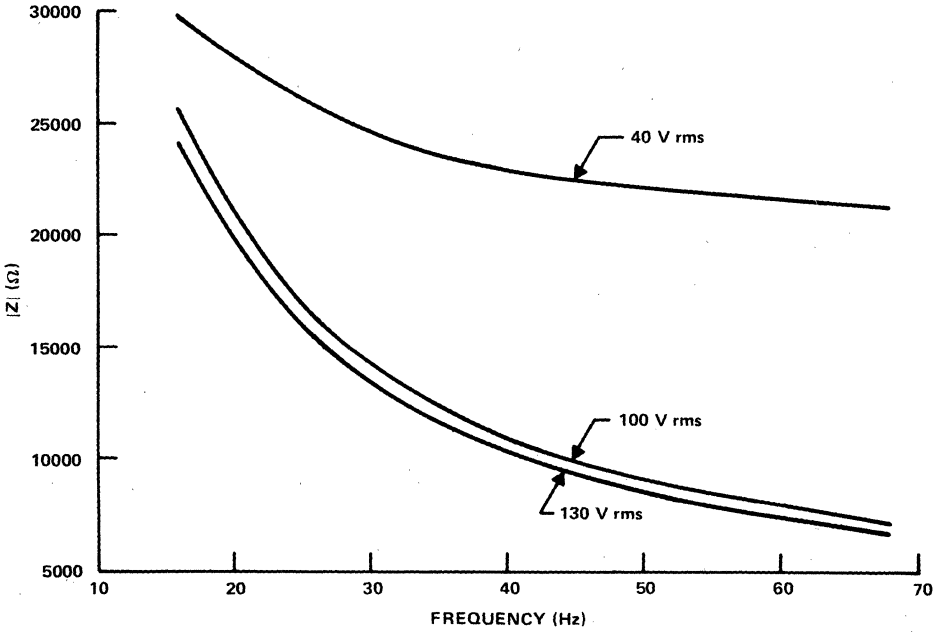
Figure 13. TCM1520A with Isolated Supply

Autoanswer MODEM

Figure 16 shows how TCM1520A may be used to design an autoanswer MODEM. The incoming ring signal is detected by the TCM1520A which drives an optoisolator to give a MOS/TTL compatible signal to the μP. The μP on recognizing a valid ring signal gives an off-hook (OH) signal to DAA (Direct Access Arrangement), thus answering the "phone." The transmitting device can now send the carrier and start data transmission. The TCM1520A goes in the standby mode offering a better than 1-MΩ impedance to signals below 5 V rms, thus offering no signal degradation to transmit or receive audio signals.



(a) Output Voltage vs Load



(b) Output Open

Figure 14. TCM1520A Drive Capability

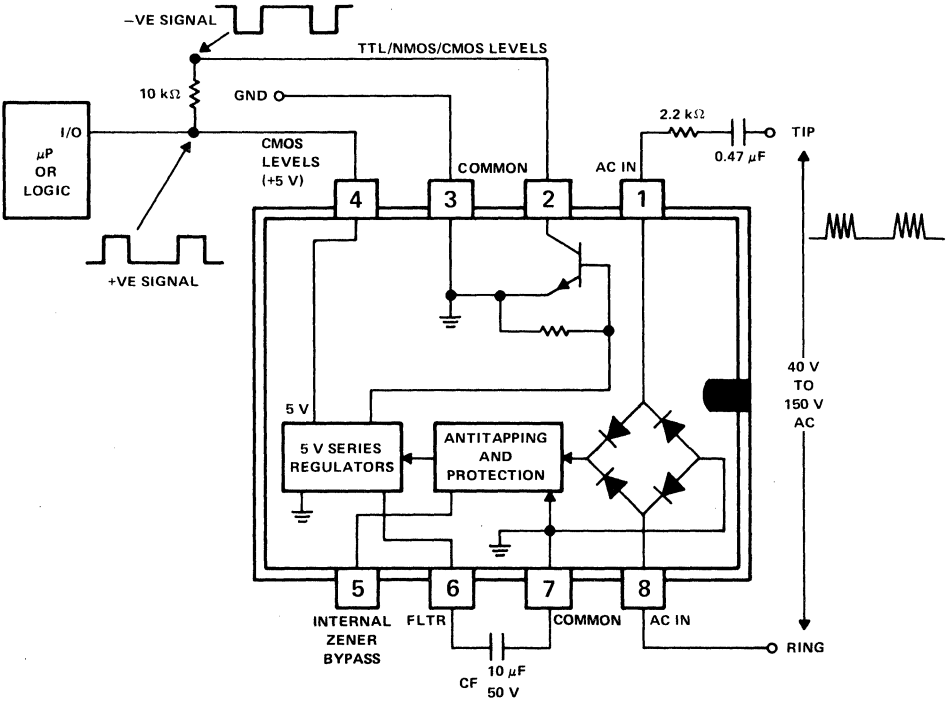


Figure 15. TCM1520A with Nonisolated Supply

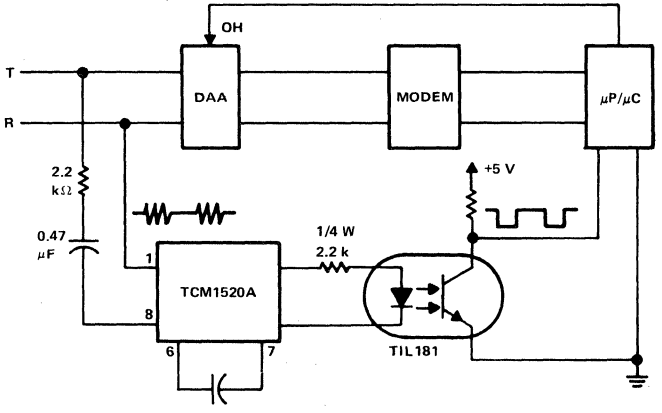


Figure 16. Autoanswer Modem Applications

TCM1520A as a Low Current Power Supply

The TCM1520A may also be used as an inexpensive 5 V power supply as shown in Figure 17. This circuit may be plugged directly into a standard 110 V, 60 Hz wall outlet and a regulated 5 V is available at pin 4. The current drive capability in this configuration is dependent upon the series limiting resistor. With a 6.8-kΩ resistor as shown, the drive capability is about 7 mA.

μC Control of Ringer

Figure 18 shows how a TCM1512A and TCM1520A may be used to detect a ring signal and then let a microcomputer decide whether to ring the ringer or not. The TCM1520A is used to detect the presence of a ring signal. The TCM1512A is used to drive the piezo transducer. The ringer disable switch could be used to tell the microprocessor whether to ring the ringer or start the tape recorder.

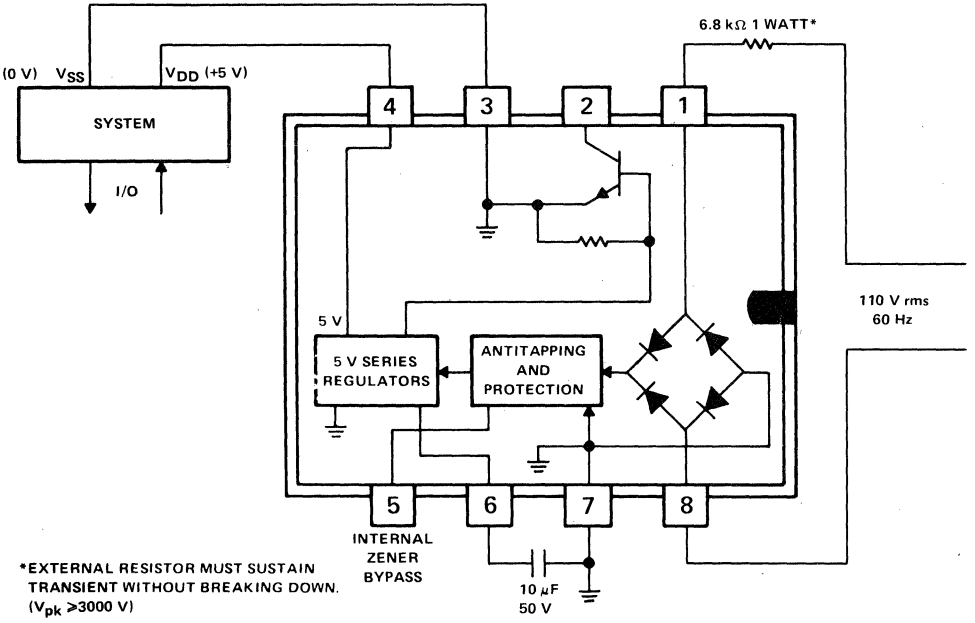


Figure 17. Small Current Power Supply

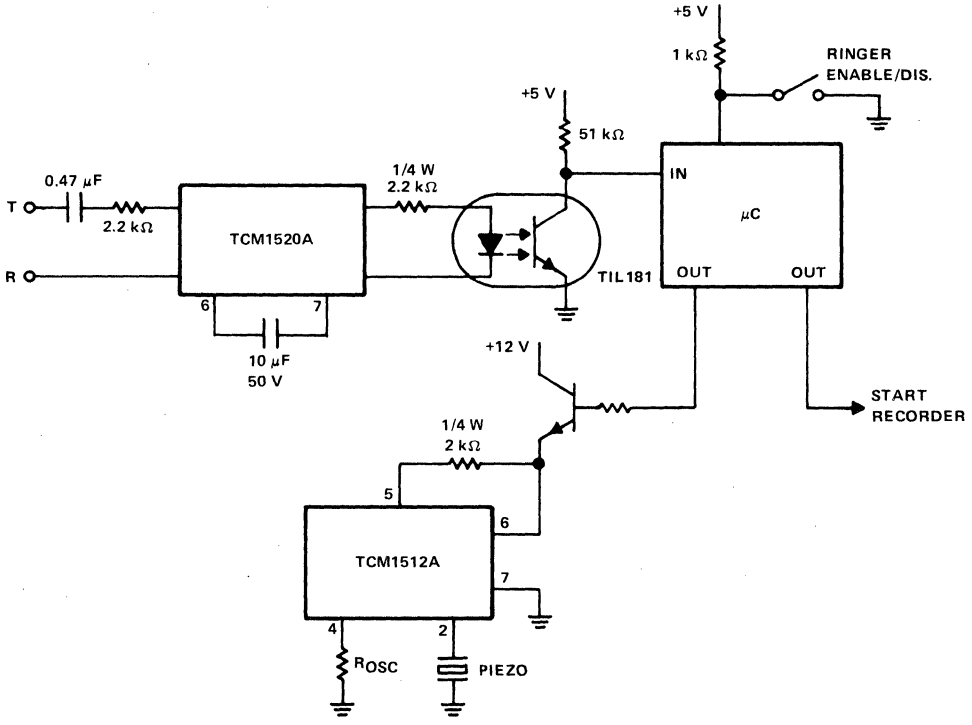
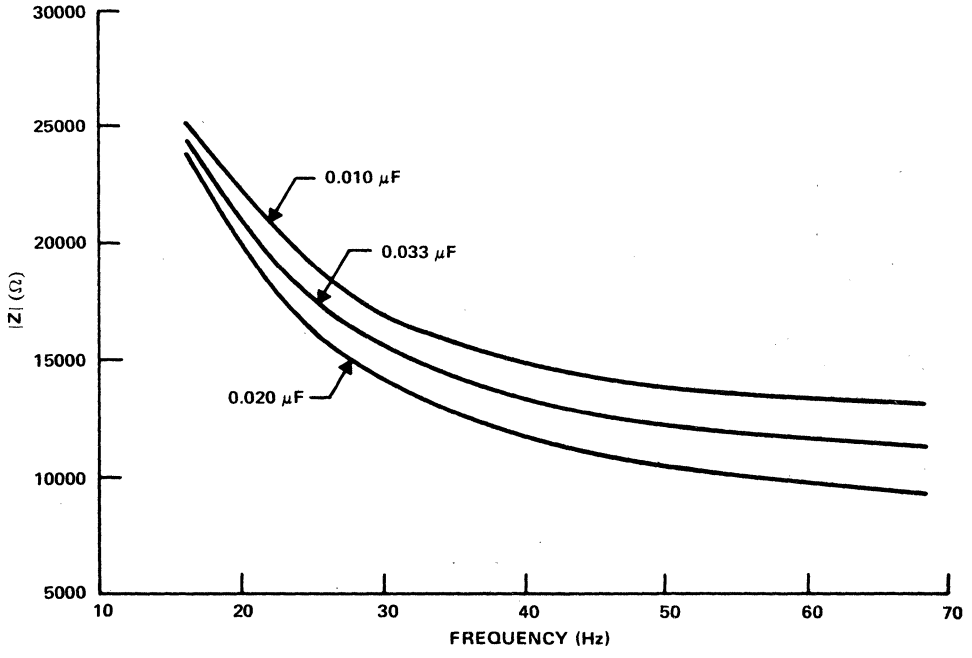


Figure 18. Using TCM1520A to Detect Ring Signal and μc to Drive TCM1512A

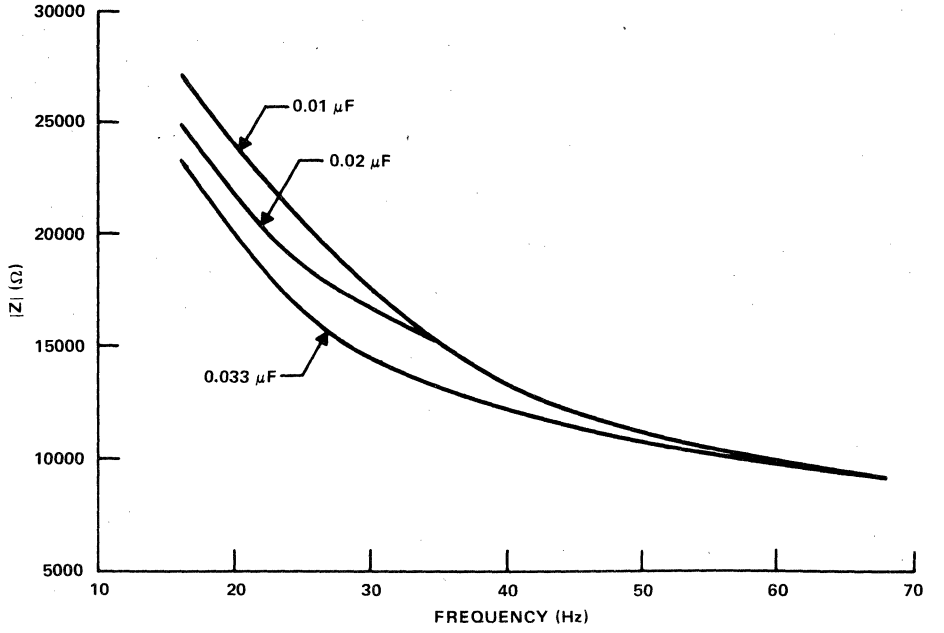
APPENDIX A

IMPEDANCE VS FREQUENCY CURVES FOR VARIOUS VALUES OF CAPACITORS TO SIMULATE PIEZO PERFORMANCE

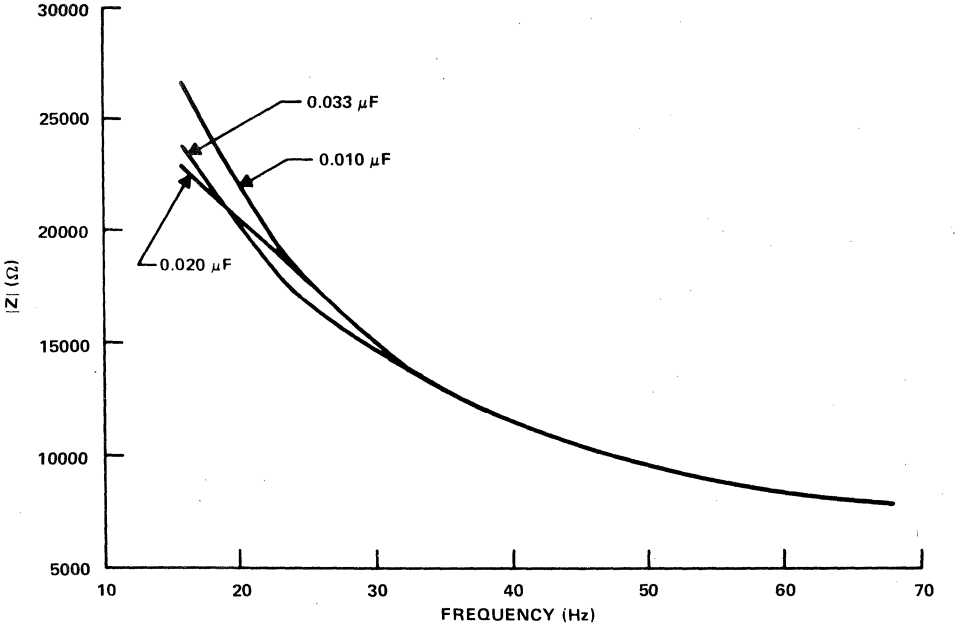


(a) V_{IN} = 40 V rms

Figure A-1. TCM1501A Using Capacitors to Simulate Piezo Performance



(b) V_{IN} = 100 V rms



(c) V_{IN} = 130 V rms

APPENDIX B

KYOCERA PIEZOELECTRIC ACOUSTIC GENERATOR SPECIFICATIONS.

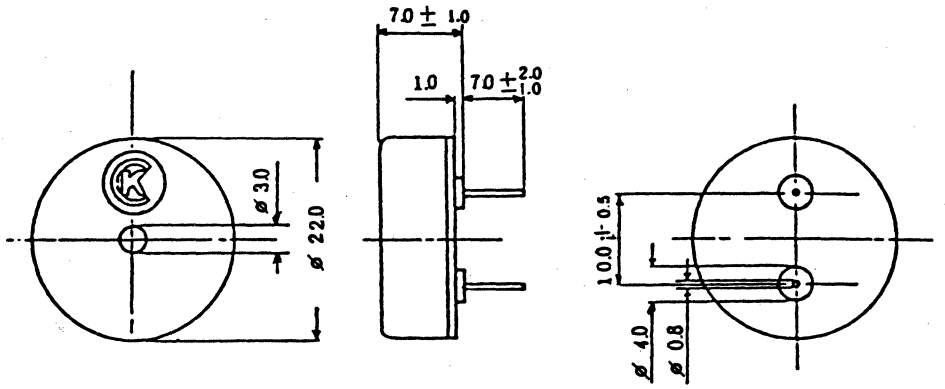
Contact your local Kyocera International, Inc., representative for further details on their devices.

Headquarters: Kyocera International, Inc.
8611 Balboa Avenue
San Diego, CA 92123
(619) 279-8310

Texas: Kyocera International, Inc.
13771 N. Central Expressway
Suite 733
Dallas, Texas 75243
(214) 234-2408

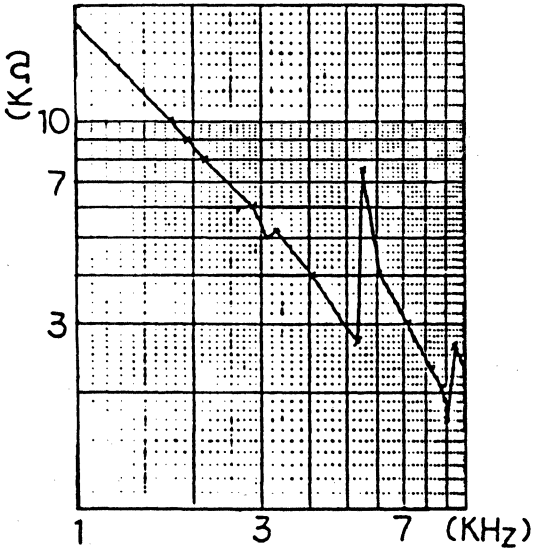
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-20DB-3P



UNIT : mm

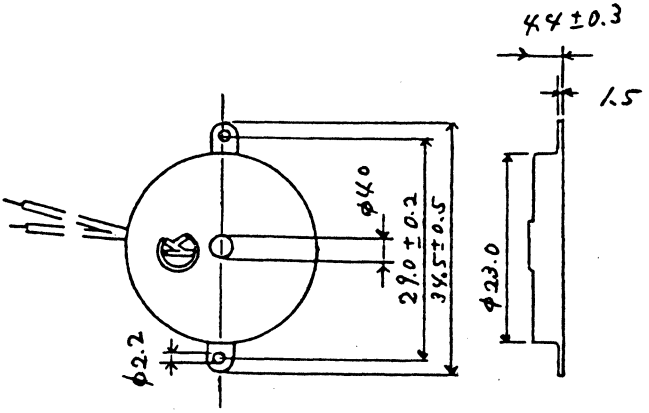
1) Working Temperature : -20°C ~ +60°C
2) Resonant Frequency : 3.5 ± 0.5 KHz
3) Resonant Impedance : 7,500 Ω MAX
4) Capacitance : 10,000 pF ± 30 %
5) Applied Voltage (nominal): 10 V_{p-p}
   Applied Voltage (maximam): 50 V_{p-p}



Impedance-Frequency Characteristic

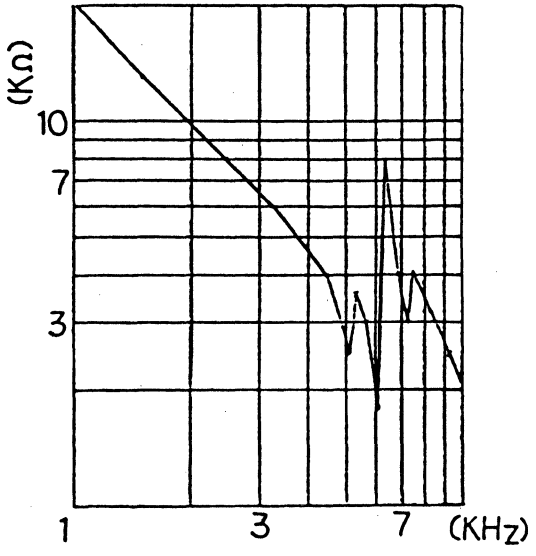
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-20DB-5A



UNIT : mm

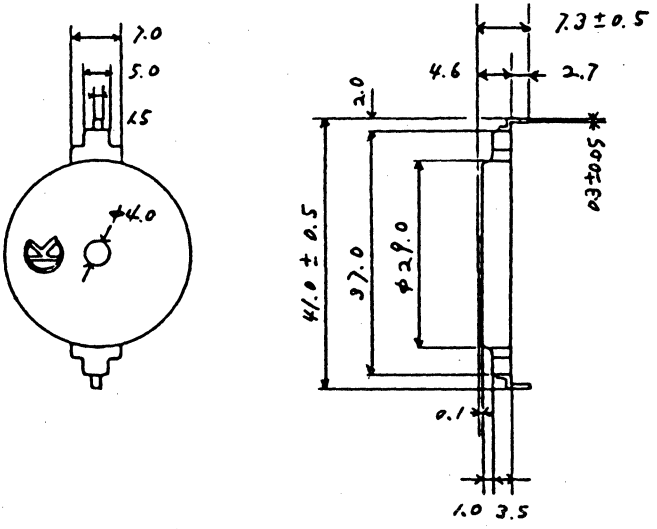
1) Working Temperature	:	-20° C ~ +60° C
2) Resonant Frequency	:	6.0 ± 2.0 KHz
3) Resonant Impedance	:	3,000 Ω MAX
4) Capacitance	:	10,000 pF ± 30 %
5) Applied Voltage (nominal):		10 V_{p-p}
Applied Voltage (maximam):		50 V_{p-p}



Impedance-Frequency Characteristic

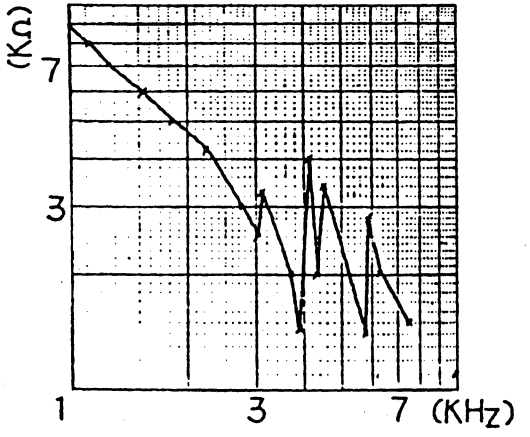
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-2708-3T



UNIT : mm

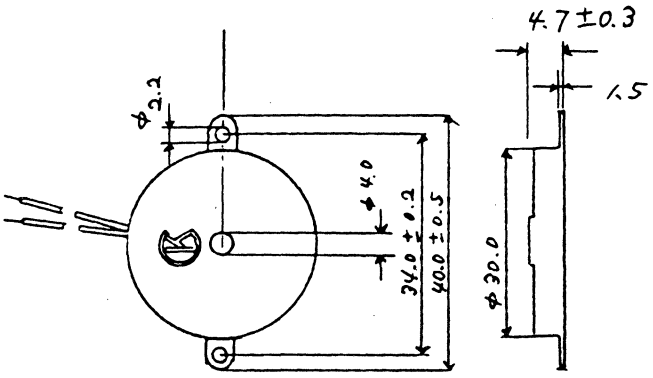
1) Working Temperature : -20°C ~ +60°C
2) Resonant Frequency : 3.8 ± 1.0 KHz
3) Resonant Impedance : 3000 Ω MAX
4) Capacitance : 20000 pF ± 30 %
5) Applied Voltage (nominal): 10 V_{p-p}
   Applied Voltage (maximam): 50 V_{p-p}



Impedance-Frequency Characteristic

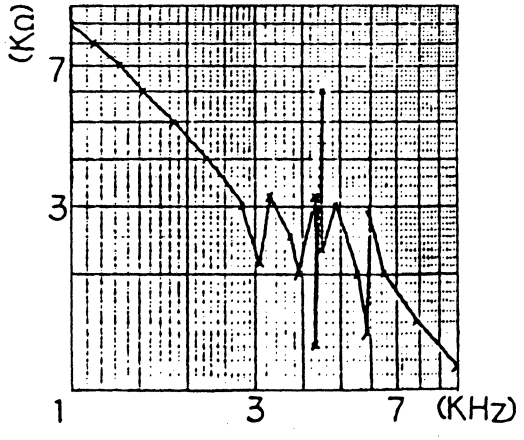
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-27DB-3A



UNIT : mm

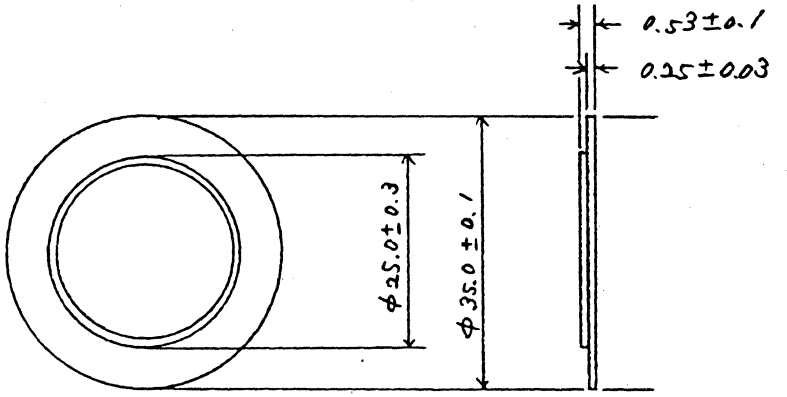
1) Working Temperature	:	-20°C ~ +60°C
2) Resonant Frequency	:	3.8 ± 1.0 KHz
3) Resonant Impedance	:	2.500 MAX
4) Capacitance	:	20.000 pF ± 30 %
5) Applied Voltage (nominal)	:	10 V_{p-p}
Applied Voltage (maximam)	:	50 V_{p-p}



Impedance-Frequency Characteristic

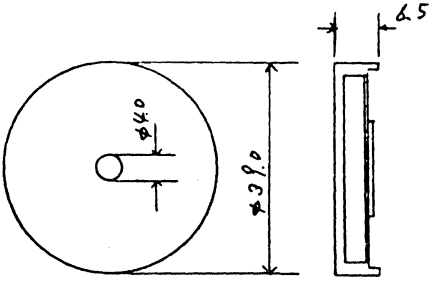
SPECIFICATIONS

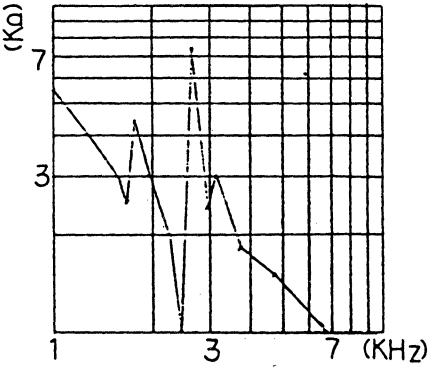
PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-35 DA-3A



UNIT : mm

1) Working Temperature : -20°C +60°C
2) Resonant Frequency : 2.9 ± 0.5 KHz
3) Resonant Impedance : 200 Ω MAX
4) Capacitance : 30000 pF ± 30 %
5) Applied Voltage (nominal): 10 V_{p-p}
   Applied Voltage (maximam): 50 V_{p-p}

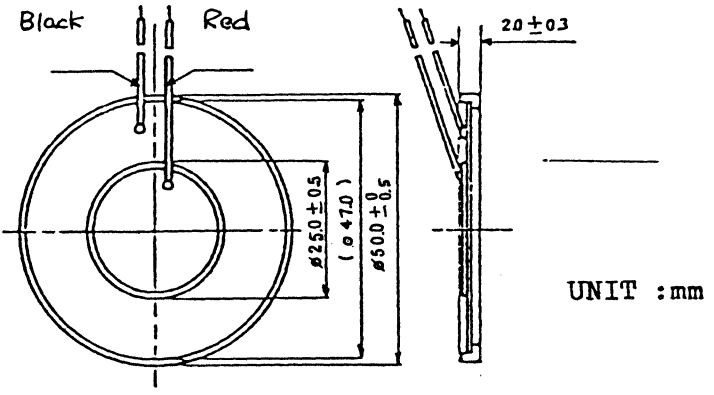




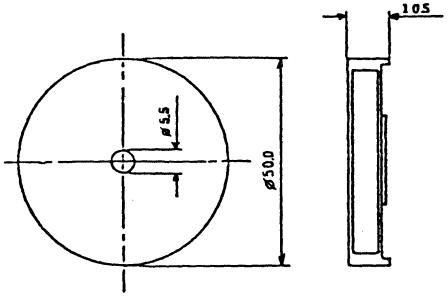
Impedance-Frequency Characteristic

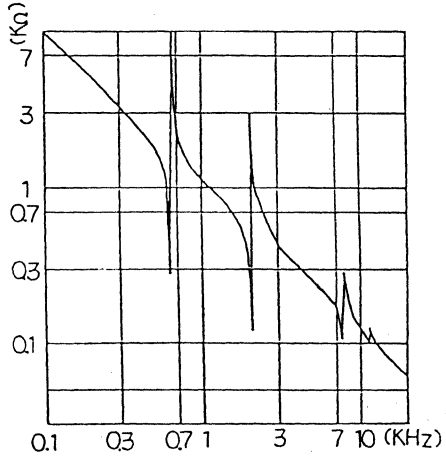
SPECIFICATIONS

PIEZOELECTRIC ACOUSTIC GENERATOR ELEMENT KBS-50DL-05C



1) Working Temperature : -20° C ~+60° C
2) Resonant Frequency : 0.55± 0.25 KHz
3) Resonant Impedance : 700 Ω MAX
4) Capacitance : 120,000 pF ± 30 %
5) Applied Voltage (nominal): 10 V_{p-p}
   Applied Voltage (maximam): 50 V_{p-p}





Impedance-Frequency Characteristic

ESD Considerations

Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies

SCOPE

This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded people's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

The part types for which these requirements are applicable include, but are not limited to, those listed:

1) All metal-oxide semiconductor (MOS) devices, e.g., CMOS, PMOS, etc.
2) Junction field-effect transistors (JFET)
3) Bipolar digital and linear circuits
4) Op Amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
5) Hybrid microcircuits and assemblies containing any of the types of devices listed
6) Printed circuit boards and any other type of assembly containing static-sensitive devices.

Definitions

1. Antistatic material: ESD protective material having a surface resistivity between 10^9 and 10^{14} Ω/square.
2. Static dissipative material: ESD protective material having surface resistivity between 10^5 and 10^9 Ω/square.
3. Conductive material: ESD protective material having a surface resistivity of 10^5 Ω/square maximum.
4. Electrostatic discharge (ESD): A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.
5. Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the dimension of Ω/square.
6. Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).
7. Ionizer: A blower that generates positive and negative ions, either by electrostatic means or by means of a radioactive energy source, in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.
8. Close proximity: For the purpose of this specification, is 6 inches or less.

Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883

Devices are categorized according to their susceptibility to damage resulting from electrostatic discharge (ESD), and the type packaging required to adequately protect them.

1) Device electrostatic sensitivity:

Category	ESD Sensitivity (V)	Minimum Protective Packaging
A	20-2000	Antistatic Magazine & Conductive Bag/Box
B	> 2000	Antistatic Magazine & Antistatic Bag

2) Devices are to be categorized by their sensitivity
3) Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test and shipment of completed equipment.

APPLICABLE REFERENCE DOCUMENTS

The following reference documents (of latest issue) can provide additional information on ESD controls.

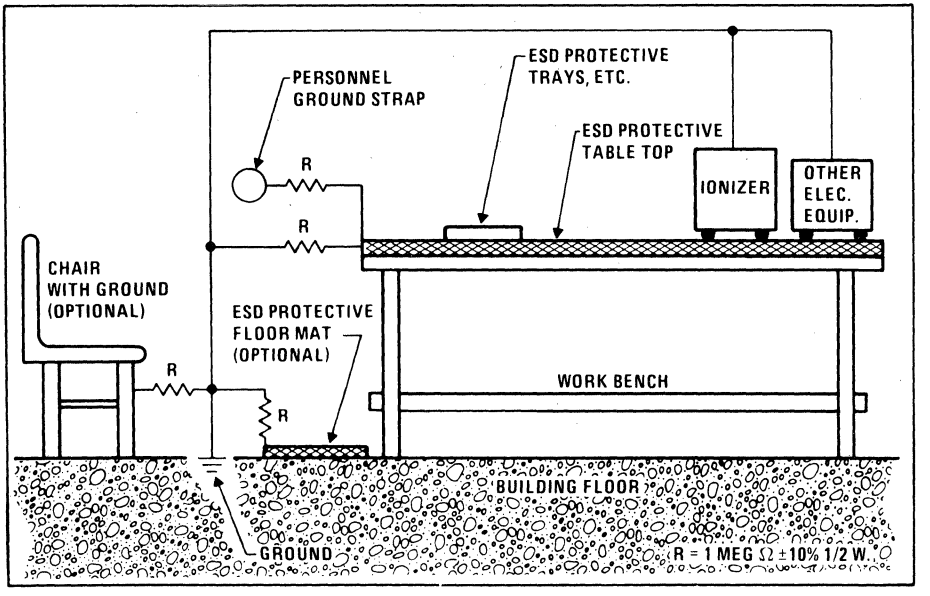
1) MIL-M-38510 Microcircuits, General Specification
2) MIL-STD-883 Test Methods and Procedures for Microelectronics
3) MIL-S-19491 Semiconductor Devices, Packaging of
4) MIL-M-55565 Microcircuits, Packaging of
5) DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
6) DOD-STD-1686 Electrostatic Discharge Control Program
7) NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual

FACILITIES FOR STATIC-FREE WORK STATION

The minimum acceptable static-free work station shall consist of the work surface covered with an ESD protective material attached to ground through a 1 MΩ ±10% resistor, an attached grounding wrist strap with integral 1 MΩ ±10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap shall be connected to the ESD protective material. Ground shall utilize the standard building earth ground, refer to Figure 42. Conductive floor tile along with conductive shoes may be used in lieu of the conductive wrist straps. The Site Safety Engineer must review and approve all electrical connections at the static-free work station prior to its implementation.

Air ionizers shall be positioned so that the devices at the static-free work stations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

General grounding requirements are to be in accordance with Table 5.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the conductive table top.

NOTE: Earth ground is not computer ground or RF ground or any other limited type ground.

Figure 42. Static-Free Work Station

Table 5. General Grounding Requirements

	TREATED WITH ANTISTATIC SOLUTION OR MADE OF CONDUCTIVE MATERIAL	GROUNDED TO COMMON POINT
Handling Equipment/Handtools	X	
Metal Parts of Fixtures and Tools/Storage Racks		X
Handling Trays/Tubes	X	
Soldering Irons/Bath		X
Table Tops/Floor Mats	X	X
Personnel		X Using Wrist Strap*

*With 1 MΩ ± 10% resistor

Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

The application of any antistatic chemical in a clean room of class 10,000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

1. Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.
2. Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

The need for initial application and frequency of reapplication can only be established through routine electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

1) Soft surfaces (carpet, fabric seats, foam padding, etc.): each 6 months or after cleaning, by spraying.
2) Hard abused surfaces (floors, table tops, tools, etc.): each week (or day for heavy use) and after cleaning, by wiping or mopping.
3) Hard unabused surfaces (cabinets, walls, fixtures, etc.): each 6 months or annually and after cleaning, by wiping or spraying.
4) Company-furnished and maintained clothing and smocks: after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the Area Supervisor where antistatic chemicals are used.

ESD Labels and Signs in Work Areas

ESD caution signs at work stations and labels on static-sensitive parts and containers shall be consistent in color, symbols, class, and voltage sensitivity identification, and appropriate instructions. Signs shall be posted at all work stations performing any handling operations with static-sensitive items. These signs shall contain the following information.

CAUTION

STATIC CAN DAMAGE COMPONENTS

Do not handle ESDS items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESDS items.

Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling. Use only QC accepted and approved signs and labels to identify static-sensitive products and work areas. The use of ESD signs and labels, and their information content shall be the responsibility of the Area Supervisor to assure consistency and compatibility throughout the static-sensitive routing.

Relative Humidity Control

Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the following relative humidity ranges: incoming/assembly/test/storage 50%-65% (ref. Ashrae, 55—74), within ±5% to avoid static voltage monitor variations.

PREPARATION FOR WORKING AT STATIC-FREE WORK STATION

A work station with a conductive work surface connected to ground through a 1 MΩ ±10% resistor, a grounding wrist strap with the ground wire connected to the conductive work surface, and an ionizer constitute a static-free work station (Figure 42). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free work station. The operator should first touch the grounded bench top before handling static-sensitive items. This precaution should be observed in addition to wearing the grouding wrist strap. If possible, operators should avoid touching leads or contacts even though grounded.

CAUTION

Personnel shall never be attached to ground without the presence of the 1 MΩ ±10% series resistor in the ground wire.

An operator's clothing should never make contact or come in close proximity with static sensitive items. They must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist which shall "cage" the sleeve at least as far up as the elbow. Only antistatic finger cots may be used when handling static-sensitive items.

Any person not properly prepared, while at or near the work station, shall not touch or come in close proximity with any static-sensitive items. It is the responsibility of the operator and the Area Supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and parts carriers must be those approved for use at the static-free work station.

GENERAL HANDLING PROCEDURES AND REQUIREMENTS

1. All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at static-free work station. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.
2. Each packing (outermost) container and package (internal or intermediate) shall have a bright yellow warning label attached, stating the following information or equivalent:

   The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.
3. Static-sensitive items are to remain in their protective containers except when actually in work at the static-free station.
4. Before removing the items from their protective container, the operator should place the container on the conductive grounded bench top and make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, then touch hands to the conductive bench top.
5. All operations on the items should be performed with the items in contact with the grounded bench top as much as possible. Do not allow conductive magazine to touch hard grounded test gear on bench top.

6. Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.
7. In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats.
8. When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
9. The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station.
10. "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than ± 100 volts).
11. Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

PACKAGING REQUIREMENTS

Packaging of static-sensitive items is to be in accordance with Device Sensitivity, item 1). The use of tape and plain plastic bags is prohibited. All outer and inner containers are to be marked as outlined in GENERAL HANDLING PROCEDURES AND REQUIREMENTS, item 2, and conductive magazines/boxes may be used in lieu of conductive bags.

SPECIFIC HANDLING PROCEDURES FOR STATIC-SENSITIVE ITEMS

Stockroom Operations

1. Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.
2. Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in FACILITIES FOR and PREPARATION FOR WORKING AT STATIC-FREE WORK STATION.
3. All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a Customer. In that case, the QC Engineer should contact the Customer and negotiate an appropriate disposition.
4. It is the responsibility of the Stockroom Supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

Module and Subassembly Operations

1. Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static sensitive.
2. All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.
3. Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.
4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

Soldering and Lead-Forming Operations

1. All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above the ground potential.

2. All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.
3. All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.
4. All stations shall be identified by posting signs as outlined in **ESD Labels and Signs in Work Areas.**
5. Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.
6. Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.
7. All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-sensitive items. Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.
8. It is the responsibility of the Area Spervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

Electrical Testing Operations

1. All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.
2. Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.
3. Devices should be in an antistatic/conductive environment except at the moment when actually under test.
4. Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.
5. All unused input leads should be biased if possible.
6. Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.
7. Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free work station as discussed in **PREPARATION FOR WORKING AT A STATIC-FREE WORK STATION**. The units must be returned to the containers before leaving the station.
8. All such items shall be shipped with an ESD warning label affixed as listed.
9. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

Packing Operations

1. Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.
2. A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with **GENERAL HANDLING PROCEDURES AND REQUIREMENTS,** item 2.
3. Any void-fillers shall be made of an approved antistatic material.

Burn-In Operations

1. Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.
2. Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connector shall be taken off just prior to plugging the board into the oven connector. The clip/connector shall be installed immediately upon removal of the board from the oven connector. Installation and removal of the clip/connector shall be done by a properly grounded operator.
3. All automatic or semiautomatic loading and unloading equipment shall be properly electrically grounded.

4. It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

CUSTOMER RETURNED ITEM HANDLING PROCEDURE

Receipt of ESDS-labeled items is to be done at a static-free work station and handled in accordance with applicable sections within this guideline.

QUALITY CONTROL PROVISIONS

Sampling

Each manufacturing, stockroom, and testing operation handling ESDS devices will be audited a minimum of once each quarter for compliance with all terms of this specification by the responsible process control or QRA organization. Ground continuity and the presence of uncontrolled static voltages are considered critical and shall be checked more frequently as specified below.

Ground Continuity (minimum of once a week).

Ground connections (grounding wrist strap, ground wires on cords, etc.) shall be checked for electrical continuity. The presence of a 1 MΩ ± 10% resistor in the ground connections between both the operator wrist straps to the work surface and the work surface to ground connector must be verified.

Grounded Conditions (minimum of once a week).

A visual inspection shall be made to determine full compliance with this specification at static-free work stations during handling of static-sensitive items, including operator being grounded as required, static-sensitive items not being handled in unprotected or unauthorized areas, and no static-generating materials at the grounded work station.

Sleeve Protectors (minimum of once a week).

A visual check shall be made to determine that each operator wearing loose-fitting or long-sleeved clothing either has sleeves properly rolled or covered with sleeve protectors properly grounded to the bare skin at the wrist.

Static Voltage Levels (minimum of once a week).

In addition to the visual inspections, a sample inspection using an electrostatic voltmeter will be used to check for uncontrolled electrostatic voltages at or near electrostatic-controlled work stations.

Conductive Floor Tiles (minimum of once a month).

Conductive floors must have a resistance of not less than 25 kΩ from any point on the tile to earth ground. Also, resistance from any point-to-point on the tile floor 3 feet apart shall be not less than 25 kΩ. The test methods to be used are ASTM-F-150-72 and NFPA 56.

Records

Written records must be kept of all these QC audits.

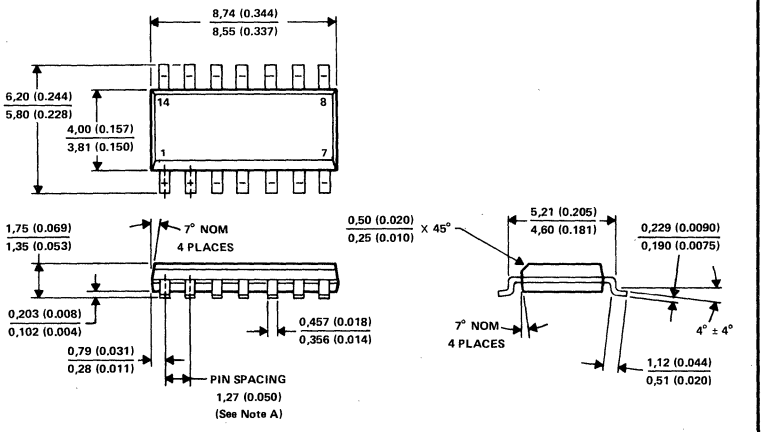
TRAINING

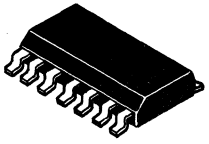
Training is applicable for all areas where individuals come in contact with ESDS (category A) devices. It is the responsibility of each Area Supervisor to make sure that his/her people receive ESD training initially and every 12 months thereafter to maintain proficiency. Training should include static fundamentals, a review of applicable parts of this specification, and actual applications in the work area.

D plastic "small-outline" package

This "small-outline" package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

14-pin D package





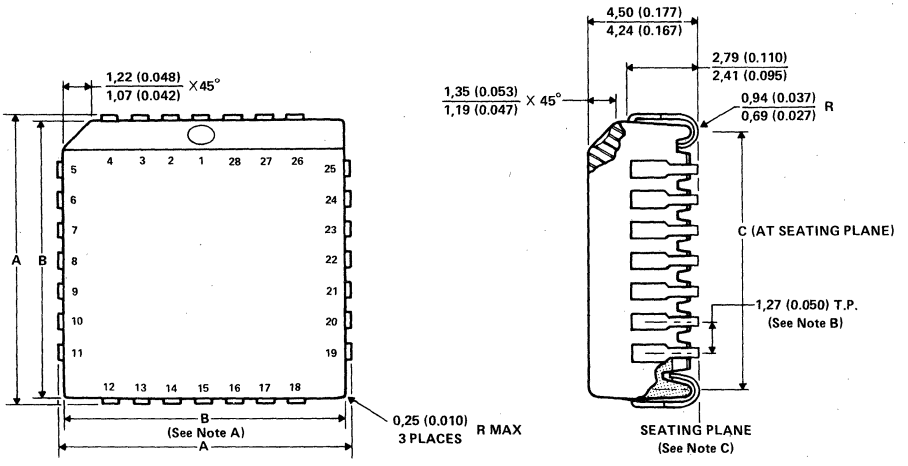
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

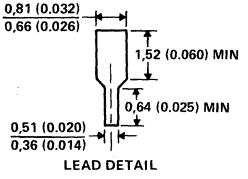
FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. the compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package used for illustration)



JEDEC OUTLINE	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO-047AA	20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
MO-047AB	28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10.41 (0.410)	10.92 (0.430)
MO-047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
MO-047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)



All dimensions and notes for the specified JEDEC outline apply.

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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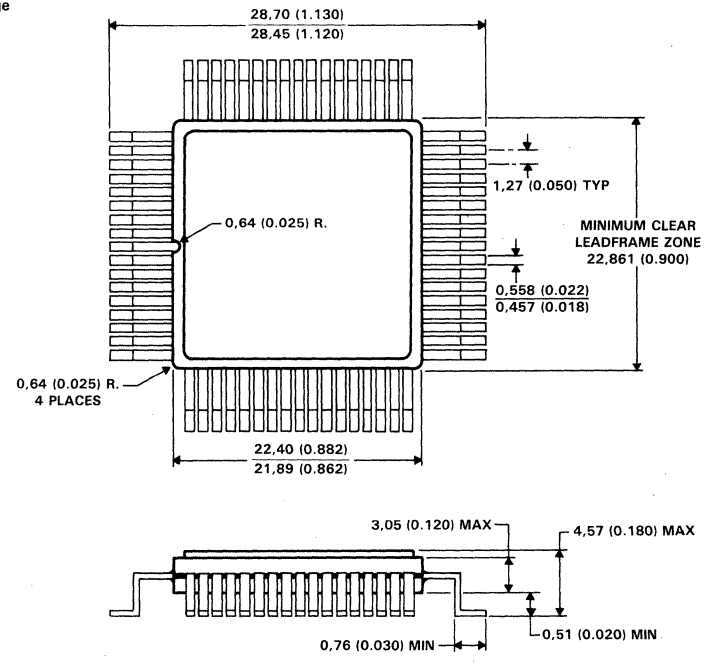
68-pin HA package

The 68-pin HA is housed in a quadriform ceramic chip carrier (CERQUAD) and has gull-wing bent leads for surface-mount technology.

68-pin HA package



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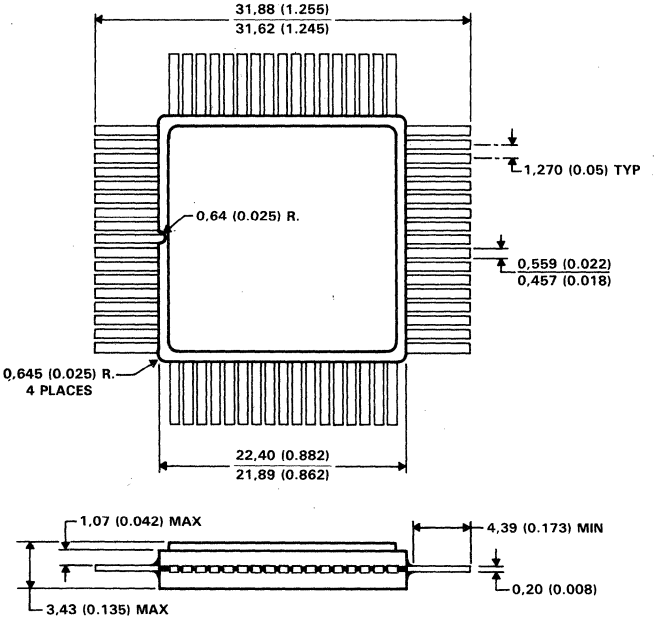
68-pin HB package

The 68-pin HB package is housed in a quadriform ceramic chip carrier (CERQUAD) and has straight leads for surface-mount technology. The straight leads are for use with low-profile sockets.

68-pin HB package



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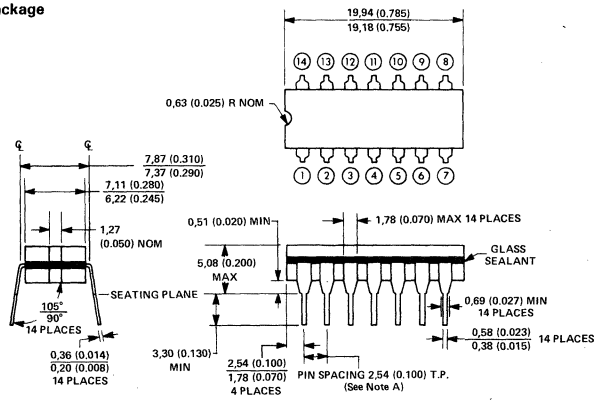
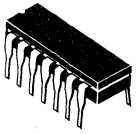
J ceramic dual-in-line package

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldering assembly.

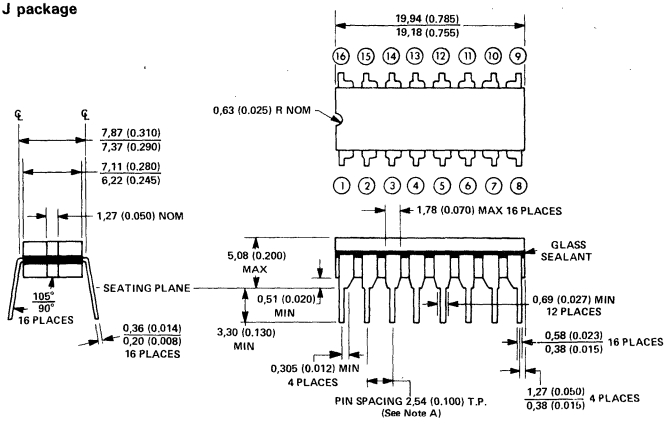
14-pin J package

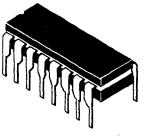




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

16-pin J package



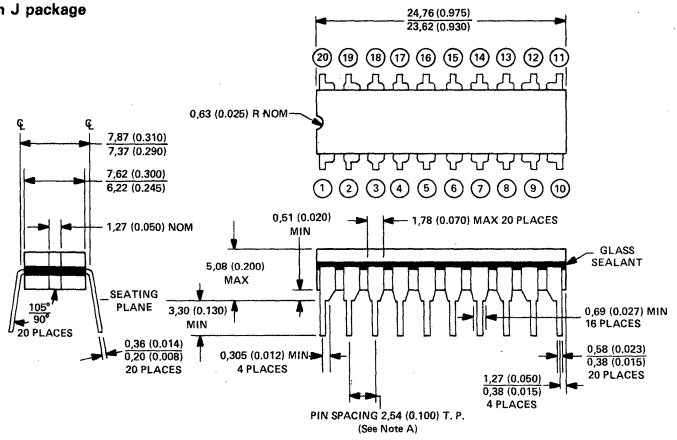


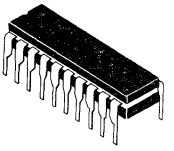
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

J ceramic dual-in-line package (continued)

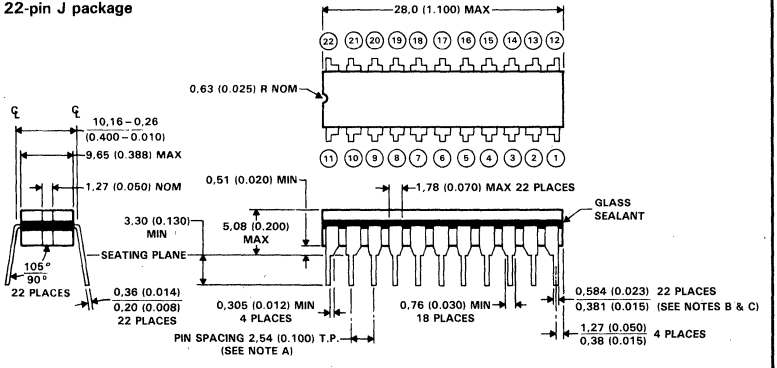
20-pin J package

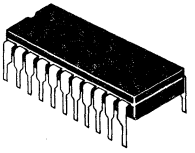




ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

22-pin J package





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,26 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,50 (0.020) above the seating plane.

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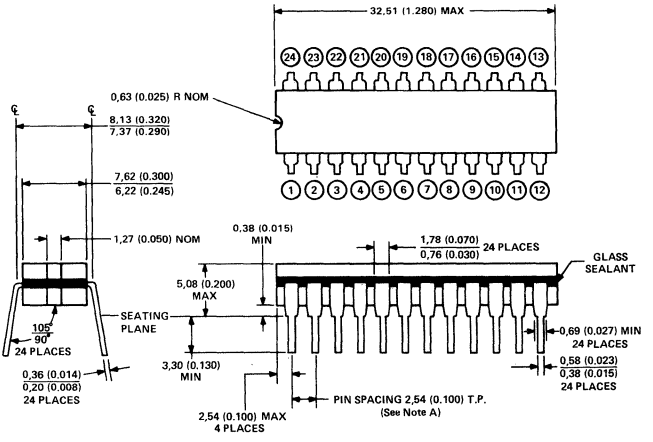
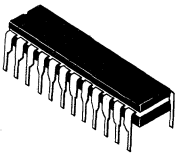
J ceramic dual-in-line package (concluded)

24-pin JT package, 0.300-inch row spacing





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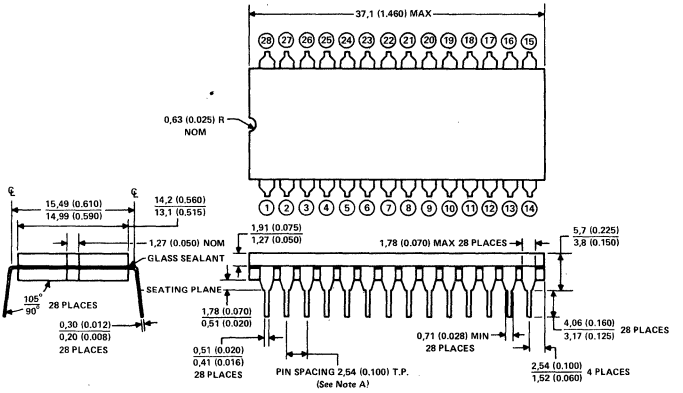
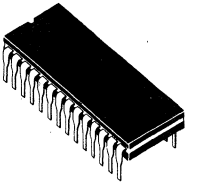
28-pin J package, 0.600-inch row spacing





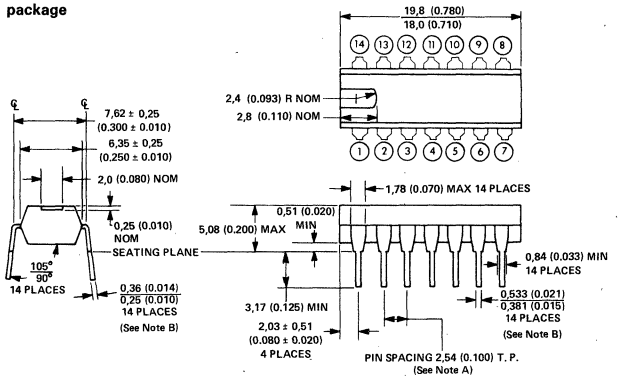
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

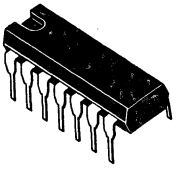
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N plastic dual-in-line package

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) or 15,24 (0.600) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-pin N package





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

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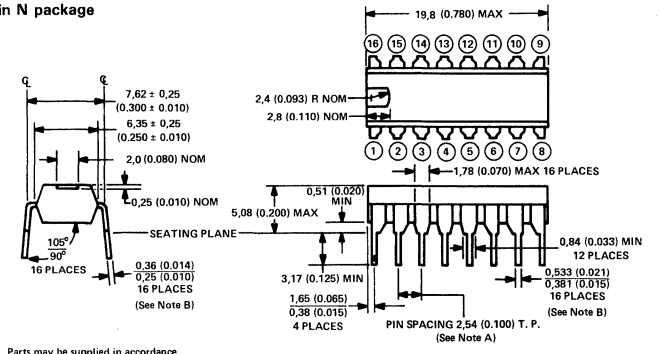
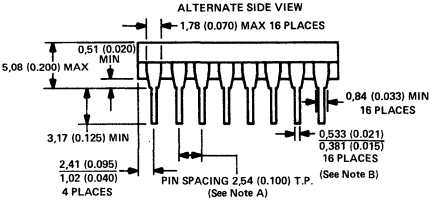
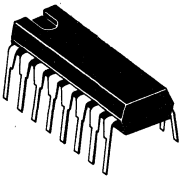
N plastic dual-in-line package (continued)

16-pin N package



Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

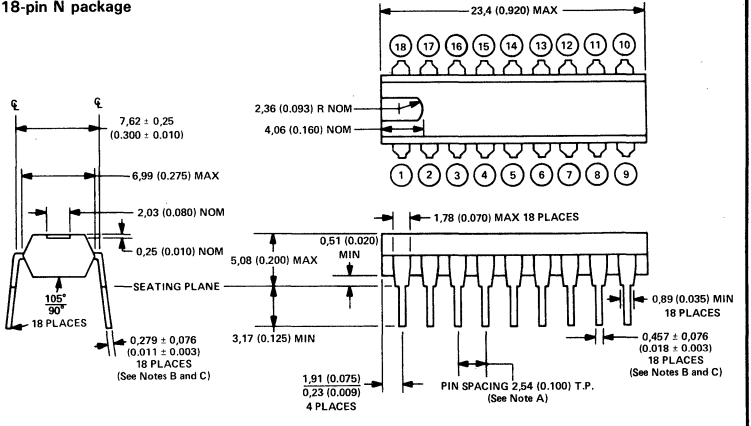


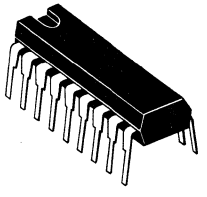


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. For solder-dipped leads, this dimension applies from the lead tip to the standoff.

18-pin N package





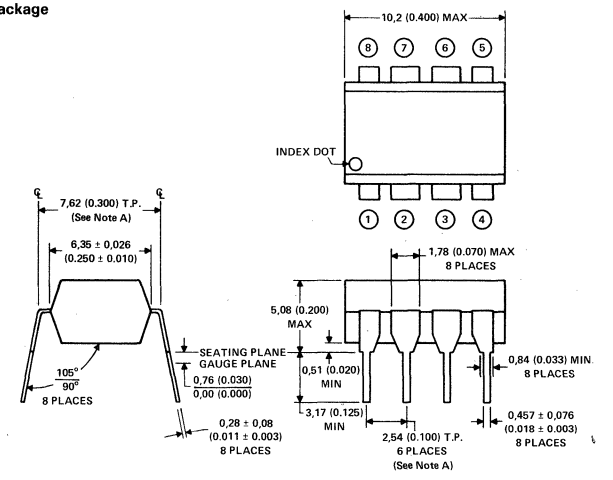
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located with 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

P dual-in-line plastic package

this dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics remain stable when operated under high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldering assembly.

8-pin P package



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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