HEWLETT® PACKARD

Technical Reference Manual HP Vectra Technology

This manual is a technical reference document for engineers and technicians providing system level support. It is assumed that the reader possesses a detailed understanding of AT-compatible microprocessor functions and digital addressing techniques.

Technical information that is readily available from other sources, such as manufacturer's proprietary publications, has not been reproduced.

This manual contains summary information only. For additional reference material, refer to the bibliography inside this document.

HP Vectra VEi 7, VEi 8, VLi 8, VLi 8 SF and VL600 PCs

Contents

Bibliography

Data sheets can be obtained at:

- *Matrox Millennium G200, G250 and G400 AGP graphics controllers*
  www.matrox.com/mga/products/home.htm
- *Intel Chipsets*
  www.intel.com/design/chipsets/datashts
- *SiS Chipsets. SiS620 and SiS5595 PCI/ISA Bridge Chip (includes information on the integrated super AGP graphics controller)*
  www.sis.com.tw/
- *Celeron, Pentium II & Pentium III Processors*
  www.intel.com/design/celeron/datashts
  www.intel.com/design/pentiumII/datashts
  www.intel.com/design/pentiumIII/datashts
- *PC Data Sheets*
  www.hp.com/vectra
- *Crystal Audio*
  www.cirrus.com/products/overviews/cs4280.html
  www.cirrus.com/products/overviews/cs4297.html
- *Intel LAN card*
  www.intel.com/network/products/pro100mgmt.htm

Hewlett-Packard white papers are available on a variety of subjects including AGP graphics, SDRAM memory and the Ultra ATA/33 protocol at:

- **www.hp.com/desktops/vectra/library.html**

Core Components and Technologies

This chapter describes core components of the PCs such as processors, chip sets, mass storage devices, graphics controllers, audio controllers, network features and input devices.

Processors

Intel Celeron (Socket 370)

The Socket 370 Intel® Celeron™ processor has the following features:

- 128K on-die L2 cache
- Intel MMX™ technology, which gives higher performance for media, communications and 3D applications.

Socket 370 is a conversion of Slot 1 (used by the Pentium® II and Pentium III) to a socket. The Socket 370 Celeron shares the same P6 microarchitecture as the Pentium II. The reduction in size achieved by the Socket 370 Celeron is due to the integration of the L2 cache on the processor die.

The heatsink is supplied separately from the processor. The processor is locked in place in the plastic pin grid array (PPGA) by a lever. Thermal efficiency is further enhanced by a heat interface gum supplied with the heatsink.

Intel Pentium II

The Pentium II processor connects to the motherboard via a single edge 242-contact slot (Slot 1) connector. It comes in either a SECC or a SECC 2 package (see “Pentium Processor Packages” below).

The Pentium II processor has several performance-enhancing features:

- Dual Independent Bus architecture, which combines a dedicated 64-bit L2 cache bus (supporting level cache sizes of 512K), plus a 64-bit system bus with non-ECC that enables multiple simultaneous transactions.
- Intel MMX technology, which improves video compression/decompression, image manipulation, encryption and I/O processing.
- Dynamic execution to speed up software performance.

Intel Pentium III

The Pentium III processor uses the same basic core and L2 cache as the Pentium II. In addition to this, however, it uses 70 new multimedia-oriented instructions known as SSE (streaming SIMD extensions). These SIMD (single instruction multiple data) instructions enable the CPU to perform simultaneous floating point calculations on multiple data. This brings substantial improvements to 3D graphics, video encoding and decoding and other floating point-intensive operations that operate on large sets of data such as voice recognition. Like the Pentium II, the Pentium III processor connects to the motherboard by a Slot 1 connector. It comes in a SECC 2 package only (see "Pentium Processor Packages" below).

- The Katmai processor cartridge includes processor core chip, ctag and data sram for L2 cache (512K) and GTL bus termination.
- The Coppermine processor cartridge includes processor core chip and GTL bus termination. The L2 cache (256K) is integrated into the core chip.
- The bus frequency (100 or 133Mhz) and the processor voltage is set automatically.

GTL+ Technology

The Processor-Local (PL) bus of Socket 370 Celeron, Pentium II and Pentium III processors, also referred to as their FSB (Front Side Bus), is implemented in GTL+ technology. This technology features open-drain signal drivers that are pulled-up to 1. 5V through five 6ohm resistors on the bus, acting as bus terminators.

The supported operating frequencies of the GTL+ bus are 66, 100 or 133 MHz. The width of the data bus is 64 bits, the width of the address is 32 bits.

The control signals of the PL bus allows the implementation of a *"split -transaction"* bus protocol. This allows the processor to send its request (such as asking for the contents of a given memory address) and then to release the bus, rather than waiting for the result, thereby allowing the bus to accept another request. The target device (PCI AGP controller chip) then requests the bus again when it is ready to respond, and sends the requested data packet. Up to four transactions can be outstanding at any given time.

Pentium Processor Packages

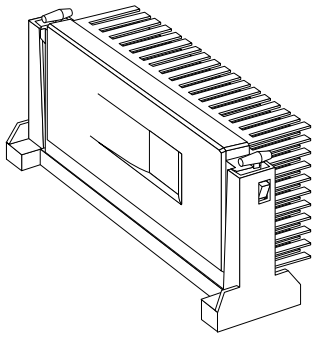
The processor and level-2 cache memory are packaged in a self-contained, pre-sealed module, installed in a Slot 1 socket on the system board.

The heat sink is supplied with the processor, and is bolted to it by the manufacturer. The processor is held in place by a retention mechanism.

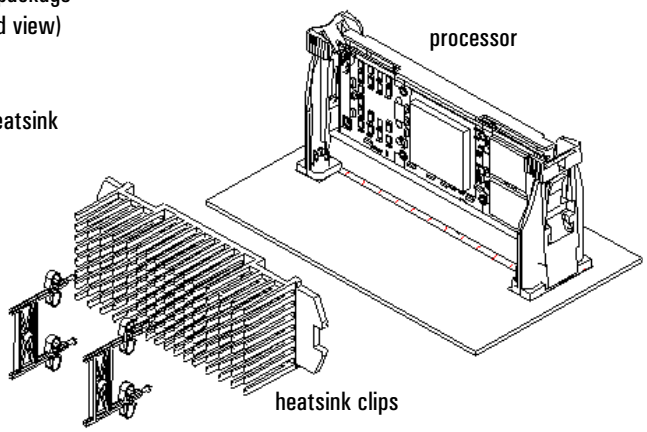
Pentium II processors use either a Single Edge Contact Cartridge (SECC) or a Single Edge Contact Cartridge 2 (SECC 2) packaging technology. These packages allow the L2 cache to be tightly coupled to the processor, while enabling the use of high volume commercial SRAM components. The Pentium III comes in the SECC2 package only.

Pentium Processor Packaging		
	SECC (Single Edge Contact Cartridge)	**SECC2 (Single Edge Contact Cartridge 2)**
Heat Sink	ATXV2	SECC2 Heat Sink
Weight	237 g	130 g
Dissipation	40 W	36 W
Attach Locations	Interfaces with thermal plate	Substrate holes
Connector	SC242	SC242
Heat Sink Clip	Riv screws	SECC2 H/S clip

SECC package



SECC 2 package
(exploded view)



Chip Sets

Intel 440ZX AGPset (VEi 8, VLi 8 and VLi 8SF PCs)

The Intel 440ZX AGPset is used in conjunction with either a Socket 370 Celeron, a Pentium II or a Pentium III processor depending on the model of PC. For information on the various configurations available, refer to the *Technical Reference Manual - Product Line Overview*.

The 440ZX chip set is derived from and has the same benchmarks as the 440BX. The only differences in features are:

- 512MB of RAM supported instead of 1GB on the 440BX
- One less PCI master
- No ECC memory support.

The Intel 440ZX AGPset is comprised of two chips: the 440ZX PAC (PCI AGP Controller) chip and the PIIX4E chip.

- The PAC chip (440ZX) is the bridge between four buses: the Processor Local Bus (GTL+, also referred to as the Host, or Front Side Bus), the main memory bus, the PCI bus and the AGP (graphics) bus.
- The PIIX4E chip is the bridge between three buses: the PCI bus, the SM bus and the ISA bus. In addition, it contains the *IDE controller*, *USB controller and Power Management logic*.

The Intel 440ZX AGPset is contained in a Ball Grid Array (BGA) package, giving a smaller footprint and higher reliability.

The two chips that make up the Intel 440ZX AGPset are explained below:

Intel 440ZX PAC Chip

The 440ZX PAC chip integrates a Host-to-PCI bridge, optimized DRAM controller and data path, and an Accelerated Graphics Port (AGP) interface. AGP is a high performance, component level interconnect, targeted at 3D graphics applications.

Features of the Intel 440ZX Chip

Processor Local Bus Interface

The 440ZX chip monitors each cycle that is initiated by the processor, and forwards those to the PCI bus that are not targeted at the local memory. It translates Processor Local (PL) bus cycles into PCI bus cycles.

The chip can support one processor at up to 100MHz Front Side Bus clock frequency.

PCI Bus Interface

The 82443ZX PCI interface is 3.3V (5V tolerant), 33 MHz and is PCI 2.1 compliant.
The maximum PCI burst transfer rate is 132 MB/s. The chip supports advanced snooping for PCI master bursting, and provides a pre-fetch mechanism dedicated for IDE read.
The PCI arbiter supports PCI bus arbitration for up to six masters using a rotating priority mechanism. Its hidden arbitration scheme minimizes arbitration overhead.

AGP Bus Interface

A controller for the AGP (Accelerated Graphics Port) slot is integrated in the 440ZX PAC chip. The PAC chip supports only a synchronous AGP interface, coupling to the host bus frequency. The AGP characteristics are described in detail in "Matrox Millennium G200 AGP Graphics (VEi 8, VLi 8 and VLi 8SF PCs)" on page 35.

Main Memory Controller

The main memory controller in the 440ZX chip supports two DIMM slots. Each slot can host a 168-pin unbuffered SDRAM module, running at 100MHz, for a total of up to 51 2MB of dynamic random access memory (non-ECC SDRAM).

The memory bus is 72-bits wide, comprised of 64 bits of data and 8 bits of ECC. However, the 440ZX chip does not support ECC operation.

Read/Write Buffers

The 440ZX chip defines a data buffering scheme to support the required level of concurrent operations and provide adequate sustained bandwidth between the DRAM subsystem and all other system interfaces (Host, AGP and PCI).

System Clocking

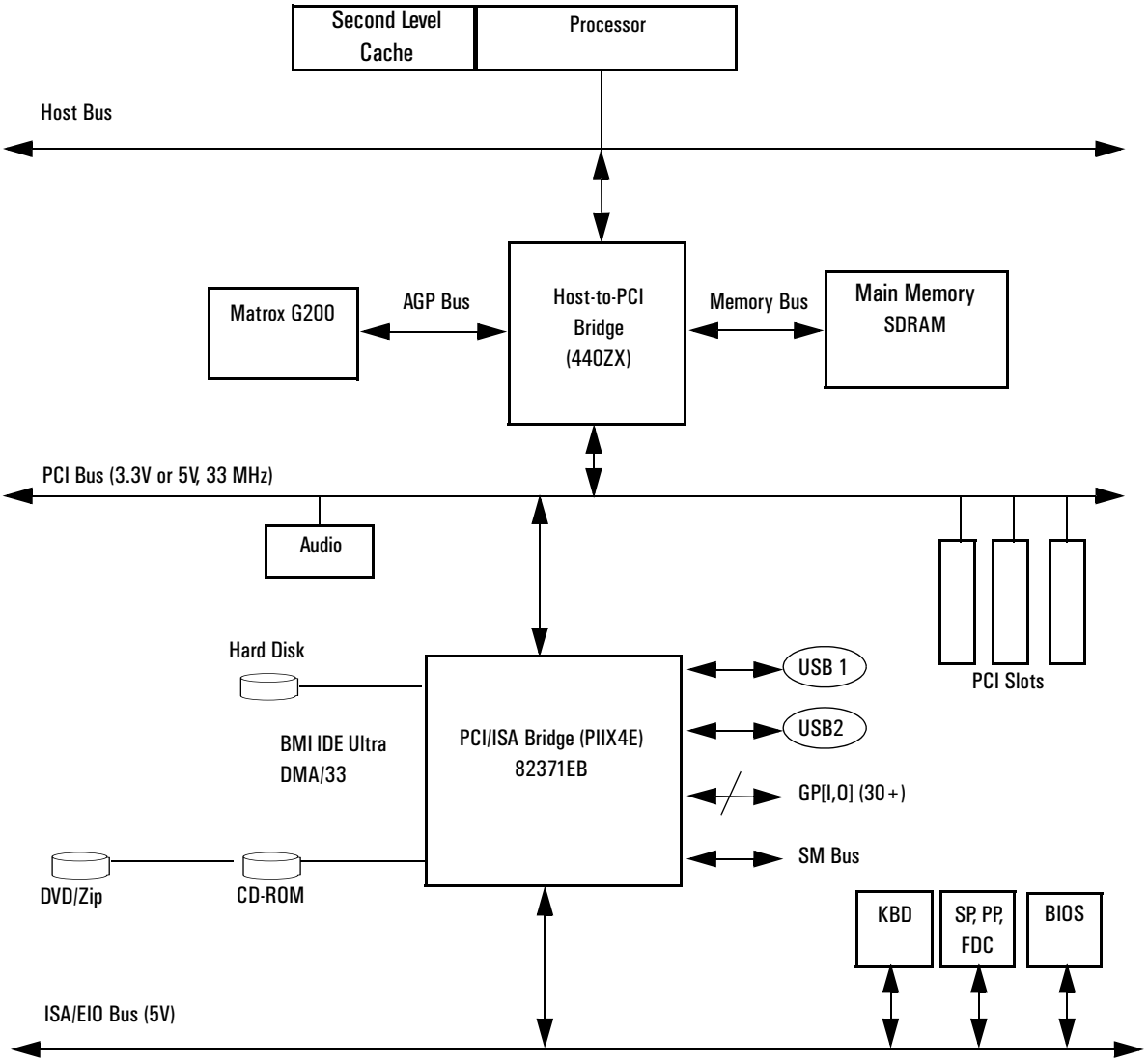
The 440ZX chip operates the host interface at 100MHz, the SDRAM/core at 100MHz, PCI at 33 MHz and AGP at 66 MHz. Coupling between all interfaces and internal logic is done in a synchronous manner. The clocking scheme uses an external clock synthesizer (which produces reference clocks for the host and PCI interfaces).

The PIIX4E PCI/ISA Bridge Chip (82371EB)

The universal host controller interface (UHCI) chip, known as PIIX4E, is encapsulated in a Ball Grid Array (BGA) package.

The PIIX4E chip is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Bus host/hub function, and an Enhanced Power Management function.

Intel PIIX4E PCI-ISA Bridge Chip Block Diagram



Features of the Intel PXII4E PCI-ISA Bridge Chip

PCI Bus Interface

This part of the chip is responsible for transferring data between the PCI bus and the ISA expansion bus. It performs PCI-to-ISA, and ISA-to-PCI bus cycle translation. It supports the Plug-and-Play mechanism. Data buffers are provided, to isolate the PCI and ISA buses.

ISA Bus Interface

As well as accepting cycles from the PCI bus interface, and translating them for the ISA bus, the ISA bus interface also requests the PCI master bridge to generate PCI cycles on behalf of a DMA or ISA master. The ISA bus interface contains a standard ISA bus controller and data buffering logic. It can directly support six ISA slots without external data or address buffering.

SMBus Controller

The System Management (SM) bus is a two-wire serial bus provided by the PIIX4E controller. It runs at a maximum of 16 kHz. The bus monitors some of the hardware functions of the main board, both during boot-up and run-time. All access to the SM bus is handled by the main processor, via the PIIX4E SM bus registers.

IDE Controller

The PCI master/slave IDE controller supports four devices, two on each of two channels.

USB Controller

The PCI USB (Universal Serial Bus) controller, supports two stacked USB connectors on the back panel. These ports are built into the PIIX4E controller as standard USB ports.

Ultra DMA Controller

The seven channel DMA controller incorporates the functionality of two 82C37 DMA controllers. Channels 0 to 3 are for 8-bit DMA devices, while channels 5 to 7 are for 16-bit devices. The channels can be programmed for any of the four transfer modes: the three active modes (single, demand and block), can perform three different types of transfer: read, write and verify. The address generation circuitry supports 24-bit addresses for DMA devices.

Interrupt Controller

The interrupt controller incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded, supporting 15 interrupts (edge/level triggered).

Counter / Timer

The chip contains a three-channel 82C54 counter/timer. The counters use a division of the 14.318 MHz OSC input as the clock source.

For tips on where to find more information on the Intel 440ZX AGPset, refer to the bibliography at the beginning of this document.

Intel i820 Chipset (VL600 PCs)

Intel 82820 Memory Controller Hub (MCH)

Host Interface

- Pentium III processor on Slot 1
- Processor support for 100 or 133MHz front side bus
- 32-bit host bus addressing
- 6 deep in-order queue.

Direct RDRAM Memory Interface

- Single Direct RDRAM Channel
- Supports PC600, PC700 and PC800 Rambus DRAM memory modules
- 300 or 400MHz RDRAM operation (with 100MHz front side bus); 256, 356 or 400MHz operation (with 133MHz front side bus)
- 64M**B**, 128MB, 256MB or 512MB DRAM Technology
- 256MB, 512MB, 1GB max memory array size (end of Year)
- Maximum of 8 Simultaneous Open Pages
- Active Power Management of RDRAM Devices (for ACPI Suspend to RAM)
- Configurable ECC Operation
- Single bit error detection and correction (ECC) and scrubbing
- Double bit error detection (EC)

AGP 2.0 Interface

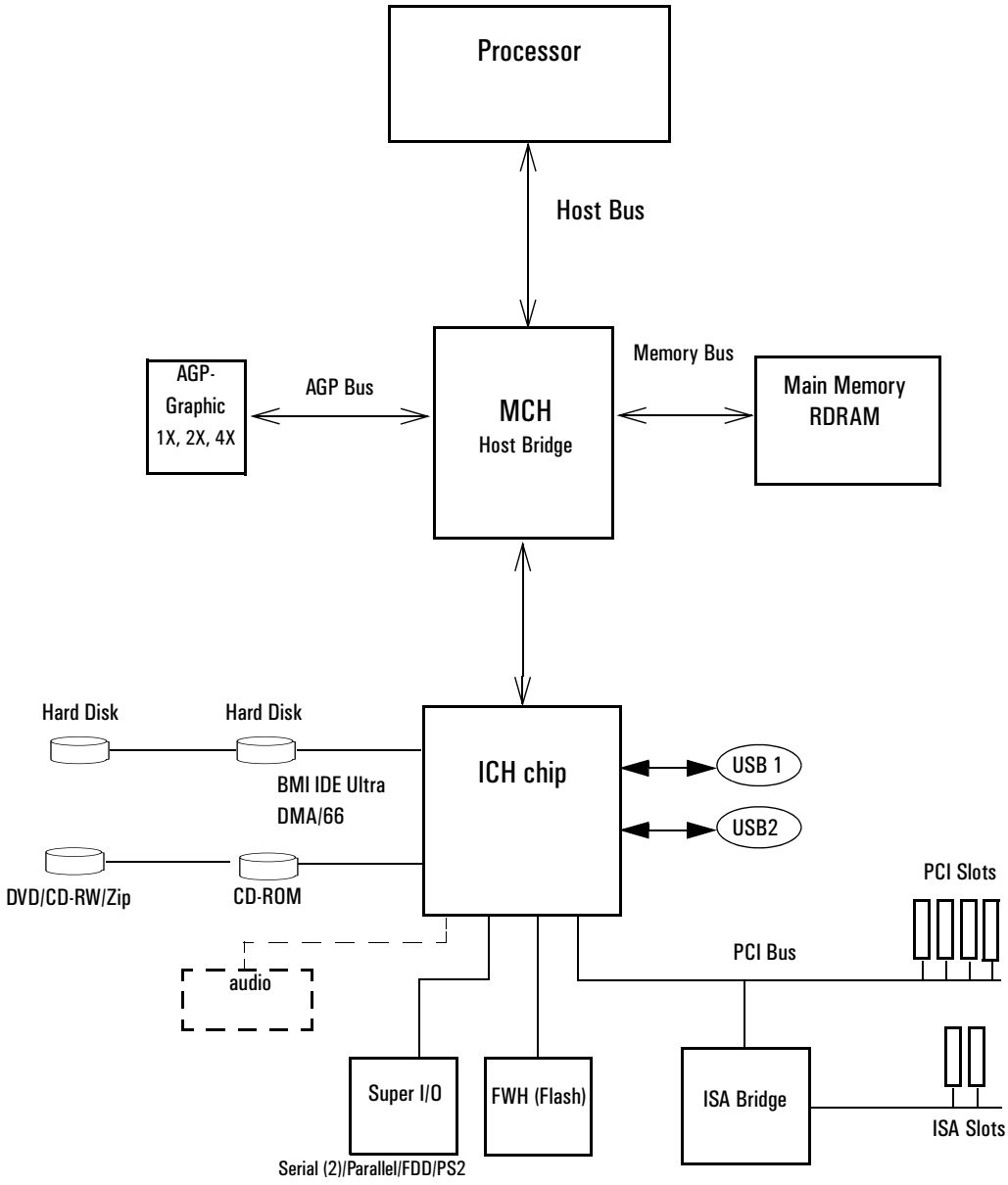
- Support for a Single AGP Device
- AGP 4X Data Transfers
- 1 Gbyte/sec Data Transfer Rate
- Differential Strobes for More Accurate Timings
- AGP 2X and 4X Fast Writes
- Fast Transfers from Processor to AGP
- Use with USWC cycles to raise Driver Performance
- 1.5v and 3.3v Power Supply Support
- AGP Universal Connector Supported
- Dual Mode Buffers allow use of AGP 1.0 and AGP 2.0 Compliant Devices

I/O Controller Hub (ICH)

PCI Bus Interface	• Master PCI Device Support: up to 6 • Supports PCI at 33 MHz • Supports PCI Rev 2.2 specification • 133 MByte/sec maximum throughput.
Integrated IDE Controller	• ICH Support of Ultra ATA/66 Mode (66 MB/s) • Independent Timing of Up to 4 Drives • Supports Ultra ATA/33 Mode (33 Mbytes/sec) • PIO Mode 4 Transfers up to 14 Mbytes/s • Separate IDE Connections for Primary and Secondary Cables • Implements Write Ping-Pong Buffer for faster write performance
USB	• UHCI Implementation with 2 Ports • Supports Wake-up from sleeping states S1-S4 • Supports Legacy Keyboard/Mouse Software • USB Revision 1.1 Complaint
Interrupt Controller	• Two Cascaded 82C59 • Integrated I/O APIC Capability • 15 Interrupts Support in 8259 Mode, 24
Power Management Logic	• ACPI 1.0 Compliant • Support for APM-Based Legacy Power Management for Non-ACPI Implementations • ACPI Defined Power States (S1, S3, S4, S5) • ACPI Power Management Timer • SMI# Generation • All Registers Readable/Restorable for Proper Resume from 0 V Suspend States.

Enhanced DMA Controller	• Two Cascaded 8237 DMA Controllers • PCI DMA: Supports PC/PCI - Includes Two PC/PCI REQ#/GNT# Pairs • Supports LPC DMA • Supports DMA Collection Buffer to Provide Type-F DMA Performance for All DMA Channels
SM Bus	• Host Interface Allows Processor to Communicate via SM Bus • Compatible With Most 2-Wire Components that are Also I 2 C compatible
Other Features	• Timers Based on 82C54 • RTC with Year 2000 support • System Timer, Refresh Request, Speaker Tone Output

Intel i820 PCI-ISA Bridge Chip Block Diagram



SiS 620/5595 Chip Set (VEi 7 PCs)

The SiS 620/5595 chip set is used in conjunction with a Socket 370 Celeron processor. The SiS 620/5595 chip set is comprised of two chips: the SiS 620 host chip and the SiS 5595 PCI/ISA bridge chip.

- The SiS 620 is the bridge between three buses: the Processor Local Bus (GTL+, also referred to as the Host, or Front Side Bus), the main memory bus, and the PCI bus.
- The SiS 5595 chip is the bridge between three buses: the PCI bus, the SM bus and the ISA bus. In addition, it contains the USB controller and Power Management logic.

The SiS 620 Chip

The SiS620 integrates the host bus interface, the DRAM controller, the IDE controller, the PCI interface, 2D/3D Graphics accelerator and video playback accelerator. The SiS 620 is contained in a Ball Grid Array (BGA) package, giving a smaller footprint and higher reliability.

Features of the SiS 620 chip

PL Bus Interface

The SiS 620 chip monitors each cycle that is initiated by the processor, and forwards to the PCI bus those that are not targeted at the local memory. It translates PL (Processor Local) bus cycles into PCI bus cycles.

The chip can support one Celeron processor at a Front Side Bus clock frequency of 66 MHz.

PCI Bus Interface

The PCI interface is PCI2.2 compliant and supports up to 4 PCI masters. The built-in PCI arbiter uses a rotating priority arbitration scheme with guaranteed minimum access time for PCI masters, providing fair access and low latency for each PCI master.

DRAM (Main Memory) Controller

The DRAM controller supports two DIMM slots. The maximum system memory size supported is 512MB. The memory clock frequency can be operated at up to 100MHz and can be in synchronous or asynchronous modes with respect to host bus frequency. The host/DRAM clock scheme is 66/66MHz.

IDE Controller

The PCI master/slave IDE controller supports four devices, two on each of two channels.

Read/Write Buffers

The SiS 620 chip defines a data buffering scheme to support the required level of concurrent operations and provide adequate sustained bandwidth between the DRAM subsystem and all other system interfaces (Host, AGP and PCI).

System Clocking

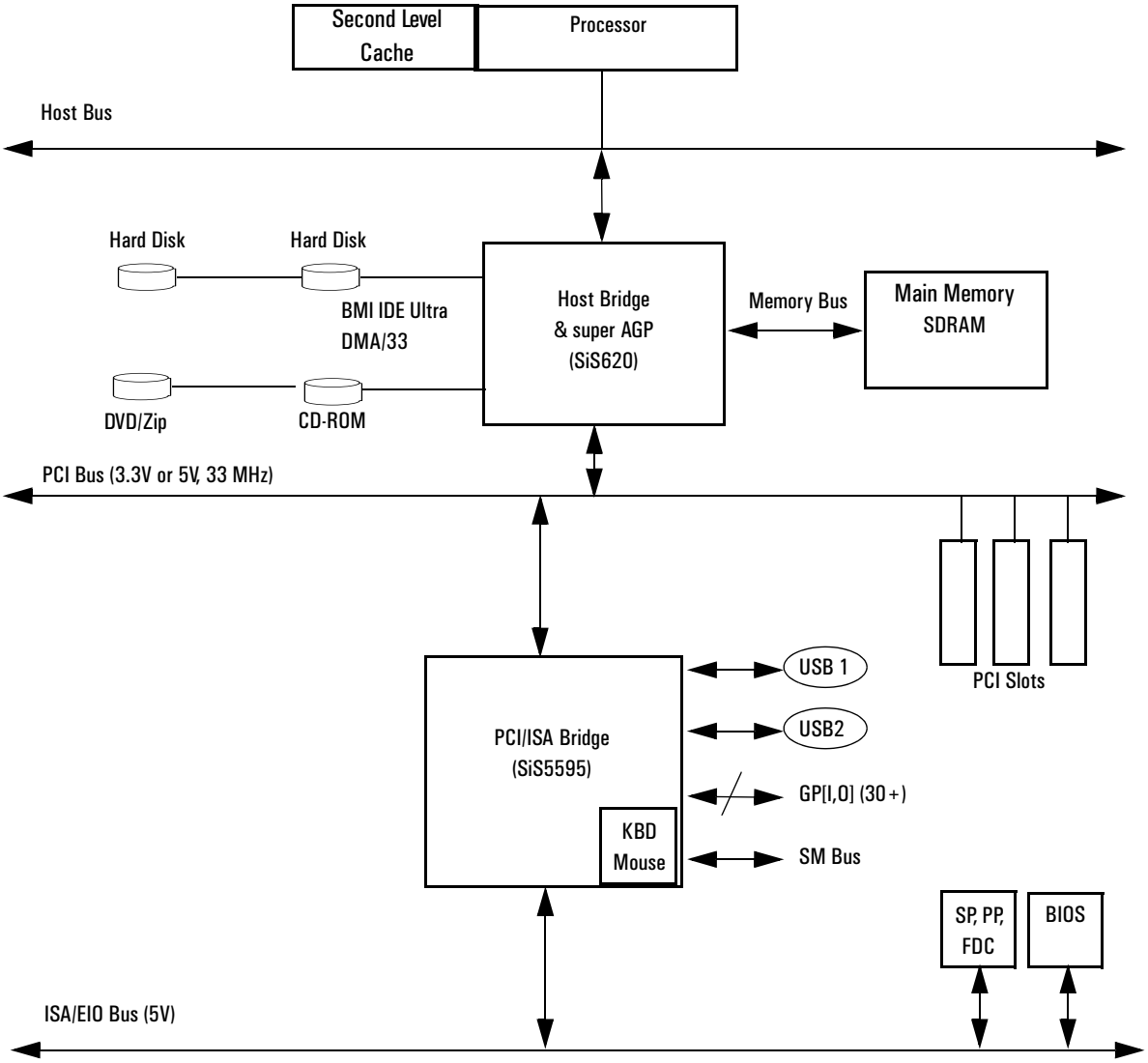
The SiS 620 chip operates the host interface at 66 MHz, the SDRAM/core at 66 MHz, PCI at 33 MHz and AGP at 66 MHz. Coupling between all interfaces and internal logic is done in a synchronous manner. The clocking scheme uses an external clock synthesizer (which produces reference clocks for the host and PCI interfaces).

The SiS 5595 PCI/ISA Bridge Chip

The SiS 5595 chip is a multi-function PCI device implementing a PCI-to-ISA bridge function, a PCI IDE function, a Universal Bus host/hub function, and an Enhanced Power Management function.

The following figure shows an example of the system block diagram using the SiS 5595 chip.

SiS 5595 PCI-ISA Bridge Chip Block Diagram



Features of the SiS 5595 Chip

PCI Bus Interface	This part of the chip is responsible for transferring data between the PCI bus and the ISA expansion bus. It performs PCI-to-ISA, and ISA-to-PCI bus cycle translation. It supports the Plug-and-Play mechanism. Data buffers are provided to isolate the PCI and ISA buses.
ISA Bus Interface	As well as accepting cycles from the PCI bus interface, and translating them for the ISA bus, the ISA bus interface also requests the PCI master bridge to generate PCI cycles on behalf of a DMA or ISA master. The ISA bus interface contains a standard ISA bus controller and data buffering logic. It can directly support six ISA slots without external data or address buffering.
SMBus Controller	The System Management (SM) bus is a two-wire serial bus provided by the SiS 5595 controller. It runs at a maximum of 16 kHz. The bus monitors some of the hardware functions of the main board, both during boot-up and run-time. All access to the SM bus is handled by the main processor, via the SiS 5595 SM bus registers.
USB Controller	The PCI USB (Universal Serial Bus) controller, supports two stacked USB connectors on the back panel. These ports are built into the SiS5595 controller as standard USB ports.
Ultra DMA Controller	The seven channel DMA controller incorporates the functionality of two 82C37 DMA controllers. Channels 0 to 3 are for 8-bit DMA devices, while channels 5 to 7 are for 16-bit devices. The channels can be programmed for any of the four transfer modes: the three active modes (single, demand and block), can perform three different types of transfer: read, write and verify. The address generation circuitry supports 24-bit addresses for DMA devices.
Interrupt Controller	The interrupt controller incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded, supporting 15 interrupts (edge/level triggered).

Counter / Timer

The chip contains a three-channel 82C54 counter/timer. The counters use a division of the 14.318 MHz OSC input as the clock source.

For tips on where to find more information on the SiS 620/5595 chip set, refer to the bibliography at the beginning of this document.

Mass-Storage Devices

Ultra-ATA Hard Disk Drives

ATA (AT Attachment) is a disk drive implementation designed to integrate the controller into the drive itself, thereby reducing interface costs. Ultra-ATA has two high performance mode: DMA/33 with 33MB/s bandwidth, twice that of DMA mode 2, and DMA/66 with 66MB/s bandwidth.

Ultra ATA/33

Ultra-ATA 33 provides higher levels of disk throughput (with a burst transfer rate of 33 megabytes per second) yet also enhancing data integrity. A checksum is added to the data sent over the ATA interface. That way, data corruption can be detected and the data retransmitted.

Ultra-ATA 33 improves timing margins by eliminating propagation and data turnaround delays. During a read under Fast ATA, the drive must wait for the strobe from the host (propagation delay) before taking some time to respond by putting data on the bus (data turnaround delay) - for which the host must then wait (more propagation delay). All these events must occur with a fixed time window between the falling edge of the strobe and the rising edge, when data is latched in the host.

The Ultra-ATA protocol eliminates these delays by having the drive be the source of both the strobe and the data during a read. Since the strobe and data signal travel in the same direction down the cable simultaneously, propagation delay in the opposite direction is eliminated. And since the drive controls both strobe and data, there is no data turnaround delay. With the time window remaining constant, less delay means improved timing margins during reads.

On top of improved timing margins, the protocol of Ultra-ATA also implements a significant feature new to ATA called Cyclical Redundancy Check (CRC) to provide data protection verification. CRC is calculated on a per-burst basis by both the host and the drive, and is stored in their respective CRC registers. At the termination of each burst, the host sends the contents of its CRC register to the drive, which compares it against its own register's contents.

For even greater integrity, the protocol can be used at speeds slower than its maximum 33MB/s. In these cases, signal and data integrity will still surpass that of Fast ATA and earlier protocols at a given burst transfer rate. In fact, the slower the Ultra-ATA transfer speeds, the greater the integrity margins.

To access HP's white paper on the Ultra ATA/33 protocol, refer to **`www.hp.com/desktop/library/wp.html`**.

Ultra ATA/66

Ultra ATA/66 is an extension of the Ultra ATA/33 hard drive interface that doubles its burst data rate. Also known as Ultra DMA/66 and Fast ATA-2, Ultra ATA/66 allows host computers to send and receive data at 66.6 MB/s, which is twice the data transfer speeds of 33.3 MB/s of Ultra DMA/33. The result is maximum disk performance under PCI local bus environments.

At its fast burst data rates, Ultra ATA/66 will go farther than Ultra ATA/33 in removing bottlenecks associated with data transfers, especially during sequential operations. Ultra ATA/66 also delivers heightened data integrity to the EIDE interface through use of a 40-pin 80-conductor cable, and CRC (Cyclical Redundancy Check) error detection code. The 80-conductor cable reduces crosstalk and improves signal integrity by providing 40 additional ground lines between the 40-pin IDE signal and ground lines. The connector is plug-compatible with existing 40-pin headers, and the incremental cost for the cable should be minimal. As with Ultra ATA/33, CRC ensures the integrity of transferred data.

By having the hard drive as the source of both the strobe and the data during a read, Ultra ATA/33 eliminated both propagation and data turnaround delays. The elimination of these delays improved the timing margins. Ultra ATA/66 retains the same strobe frequency but doubles the burst transfer rate once again.

The progressive advantage of Ultra ATA/66 is to double the transfer rate once again, this time by reducing setup times. Timing signals are made twice as fast. However, a new 80-conductor cable is needed to ensure data integrity. The 40-pin interface cable of the earlier Ultra ATA/33 and multi-word DMA interfaces cannot handle the shorter cycle times for a 44.4 MB/s or 66.6 MB/s burst rate. The 80-conductor cable retains the same connector configuration as the standard 40-pin interface cable but has ground lines interleaved between all signal lines. In other words, the 40 new lines are all ground (which act as shields) and no new signals are transferred.

Ultra ATA/33 introduced CRC, a feature new to IDE that provides data protection verification. Ultra ATA/66 uses the same process. The CRC is calculated on a per-burst basis by both the host and the hard drive, and is stored in their respective CRC registers. At the end of each burst, the host sends the contents of its CRC register to the hard drive, which then compares it against its own register's contents. If the hard drive reports errors to the host, then the host retries the command containing the CRC error.

S.M.A.R.T. Technology

S.M.A.R.T. or Self Monitoring Analysis and Reporting Technology allows the hard disk drive to report certain types of degradation or impending failure. This allows the operating system to take the necessary precautions and warn the user.

The system is comprised of software that resides both on the disk drive and on the host computer. The disk drive software monitors the internal performance of the motors, media, heads, and electronics of the drive, while the host software monitors the overall reliability status of the drive. The reliability status is determined through the analysis of the drive's internal performance level and the comparison of internal performance levels to predetermined threshold limits.

DVD Drives

Digital Versatile Disk (DVD) Technology

Digital Versatile Disc (DVD) is a medium for the distribution of from 4.7 to 17 GB of digital data on a 120-mm (4.75 inch) disc. This huge volume of data (CD-ROMs can store 680 MB) can be used to store up to nine hours of studio quality video and multi-channel surround-sound audio, highly interactive multimedia computer programs, 30 hours of CD-quality audio, or anything else that can be represented as digital data.

A DVD looks like a CD-ROM: it is a silvery disc, 4.75 inches in diameter, with a hole in the center. Like a CD, data is recorded on the disc in a spiral trail of tiny pits, and the discs are read using a laser beam. The DVD's larger capacity is achieved by making the pits smaller and the spiral tighter, and by recording the data in as many as four layers, two on each side of the disc.

To read these tightly packed discs, lasers that produce a shorter wavelength beam of light are required, as are more accurate aiming and focusing mechanisms. In fact, the focusing mechanism is the technology that allows data to be recorded on two layers. To read the second layer, the reader simply focuses the laser a little deeper into the disc, where the second layer of data is recorded.

Not only are two layer discs possible, but so are double-sided discs. The availability of four layers is what gives DVD its 17 gigabyte capacity.

	DVD	CD
Diameter	120mm	120mm
Thickness	0.6 mm	1.2 mm
Track Pitch	0.74 nanometers	1.6 nanometers
Minimum Pit Length	0.40 nanometers	0.834 nanometers
Laser Wavelength	640 nm	780 nm
Data Capacity (per layer)	4.7 GB	0.68 GB
Layers	1,2,4	1

Audio features of DVD-Video

A DVD-Video disc can have up to 8 audio tracks (streams). Each track can be in one of three formats:

- Dolby Digital (Dolby AC-3): 1 to 5.1 channels
- MPEG-2 audio: 1 to 5.1 or 7.1 channels
- LPCM: 1 to 8 channels.

Dolby Digital is multi-channel digital audio, using lossy AC-3 coding technology from original PCM with a sample rate of 48 kHz at up to 24 bits. The bitrate is 64 kbps to 448 kbps, with 384 being the normal rate for 5.1 channels and 192 being the normal rate for stereo (with or without surround encoding).

MPEG audio is multi-channel digital audio, using lossy compression from original PCM format with sample rate of 48 kHz at 16 bits. Both MPEG-1 and MPEG-2 formats are supported. The variable bitrate is 32 kbps to 912 kbps, with 384 being the normal average rate. MPEG-1 is limited to 384 kbps.

Linear PCM is uncompressed (lossless) digital audio, the same format used on CDs and most studio masters. It can be sampled at 48 or 96 kHz with 16, 20, or 24 bits/sample. (Audio CD is limited to 44.1 kHz at 16 bits.) There can be from 1 to 8 channels. The maximum bitrate is 6.144 Mbps.

DVD Region Codes

DVD Regional Locking is a system used to control which DVD movies play on which DVD Players. For example, if the first DVD-Video disc played on a DVD device is from Region 1, the device can subsequently only play DVD-Video discs from that region. The regions are broken down as follows:

Regional Codes	Region
1	USA & Canada
2	Europe & Japan
3	South East Asia
4	Latin America & Australia
5	Russia, Rest of Asia, Africa
6	China

SCSI Adapter Card

Hardware Features

PCI	• Complies with PCI 2.1 • PCI is 32bits, 33MHz • Uses DMA and Bus Mastering • Universal PCI signaling: operates on 3.3V or 5V buses
SCSI	• 16 bit Wide SCSI bus • Multimode SE/LVD SCSI bus
SCSI speed supported:	• Ultra2 80MB/s • Ultra 40MB/s • Fast 20MB/s • Asynchronous 14MB/s
Automatic termination, Multimode LVD/SE with automatic switching to Single-ended.	Yes

Connectivity

Enables both internal and external connection.

Internal Connection

The internal connector is a WideSCSI 68-pin high-density connector. The internal ribbon cable has to be connected to this connector.

External Connection

The external connector is located on the PCI bracket. It is a shielded WideSCSI 68-pin high-density connector. Any cable connected to this connector must be shielded.

When running in LVD mode, the external cable should not exceed 12m.

When running in SE mode, the external cable should not exceed 1,5m.

Cables

Internal SCSI cable

The internal SCSI cable is supplied with an embedded multi-mode terminator at one end of it.

The SCSI cable has two connectors.

LED Activity cable

The LED cable supplies SCSI LED activity to the front panel hard disk LED.

SCSI Controller

The SCSI controller characteristics are as follows:

- PCI 32bits/33MHz chip
- SCSI Multimode LVD/SE
- Max speed: 40MB/s in SE (ultra), 80MB/s in LVD (Ultra2).

PCI connector

- 32 bit universal connector (supports both 5V and 3,3V signaling)
- Configured as a 7,5W board (PRSNT1 and PRSNT2 grounded)
- The card only sink current on the 5V power supplies lines. The 3,3V is supplied by an on-board regulator.

Connectors

- 1 external shielded 68-pin high-density WideSCSI connector
- 1 internal 68-pin high-density WideSCSI connector
- 1 4-pin LED activity connector

Terminators

- 3 multi-mode SE/LVD active, auto-terminating terminators
- Auto-termination: terminators are active when one of the two connectors is used. If both connectors are used at the same time, terminators will automatically switch to high impedance mode.
- The terminator will automatically detect the bus type (LVD or SE) and switch to the right mode.

Flash memory

The flash memory stores the SCSI BIOS.

SEEPROM (also called NVRAM)

- Stores BIOS settings
- Stores the sub-system vendor ID and the sub-system device ID (programmable).

Activity LED

The Activity LED has the same function as the LED on the status panel.

SCSI BIOS

The SCSI BIOS is integrated into the onboard Flash memory. It has a standard PCI expansion ROM format.

AGP Graphics Controllers

AGP technology was developed as a means of accessing system memory as a viable alternative to augmenting the memory of the graphics subsystem needed for high quality 3D graphics applications. All the PCs covered in this manual support an AGP device (Matrox® MGA-G200, 8MB, not upgradeable, or SiS super AGP, 4MB upgradeable to 8MB).

Matrox Millennium G200 AGP Graphics (VEi 8, VLi 8 and VLi 8SF PCs)

The Matrox Millennium G200's 128-bit DualBus architecture uses two independent 64-bit buses to allow faster management of data and process graphics. The G200 graphics chip also provides full AGP 2X optimization based on Symmetrical Rendering Architecture. This enables faster data transfer rates and drawing engine access to both frame buffer and system memory.

The Millennium G200 uses a high-speed 250 MHz RAMDAC to eliminate screen flicker and produce crystal clear displays. Its 250 MHz RAMDAC incorporates ultra-high bandwidth DAC for sharp display images.

128-bit Dual Bus Architecture

The 128-bit DualBus uses two independent 64-bit buses that operate in parallel inside the graphics engine to effectively double the raw performance of almost every operation. In addition, the 128-bit DualBus architecture uses Dual Command Pipelining so that read and write phases of two consecutive commands can be overlapped and executed simultaneously.

This system allows very fast 2D performance even at the most demanding resolutions and color depths. The 64-bit granularity of the 128-bit DualBus means that for frequent copying of small bitmaps and fonts, performance is much higher than with a traditional 128-bit architecture.

Vibrant Color Quality (VCQ) Rendering

Vibrant Color Quality Rendering (VCQ) uses 32-bpp color accuracy throughout the rendering pipeline. VCQ is capable of rendering displayed images in 32-bpp color from source texture maps of up to 32-bpp color. Additionally, VCQ architecture provides high quality analog color output to avoid 'washed out' images. VCQ delivers sharp contrast and highly saturated colors for maximum photo-realism.

Symmetric Rendering Architecture (SRA)

The Millennium G200's Symmetric Rendering Architecture (SRA) treats AGP memory exactly as if it were local video memory. It is able to draw to, render to and read from AGP memory using the high bandwidth of the AGP 2X bus. The G200 also uses the SRA to implement a hierarchical texturing system (HTS) for 3D rendering. With HTS, the G200 offers the storage of surfaces - either textures, bitmaps or video streams - across three levels depending on the frequency of use or the size of the texture in most cases. The first level is the large on-chip cache, the second level is the 8MB of local video memory and the third level is the AGP memory.

Per Pixel Trilinear Filtering

Trilinear filtering is an advanced texture filtering algorithm that provides image quality much higher than bilinear filtering and must be calculated on a per pixel basis. The trilinear filtering algorithm checks texel scale factors[1] on a per pixel basis and uses the scale factor to index into two adjacent MIP maps. It then takes four texels from each MIP, bilinearly filtering each set of four pixels and then averages the results based on scale factor.

Full Resolution Rendering

The highest resolution source texture maps available are always used for rendering unless the application specifically provides lower resolution MIP maps to be used in conjunction with high resolution textures. The fast 3D engine of the G200 provides high performance without needing to downscale textures. Allows high quality rendering without compromising performance and prevents blurry images.

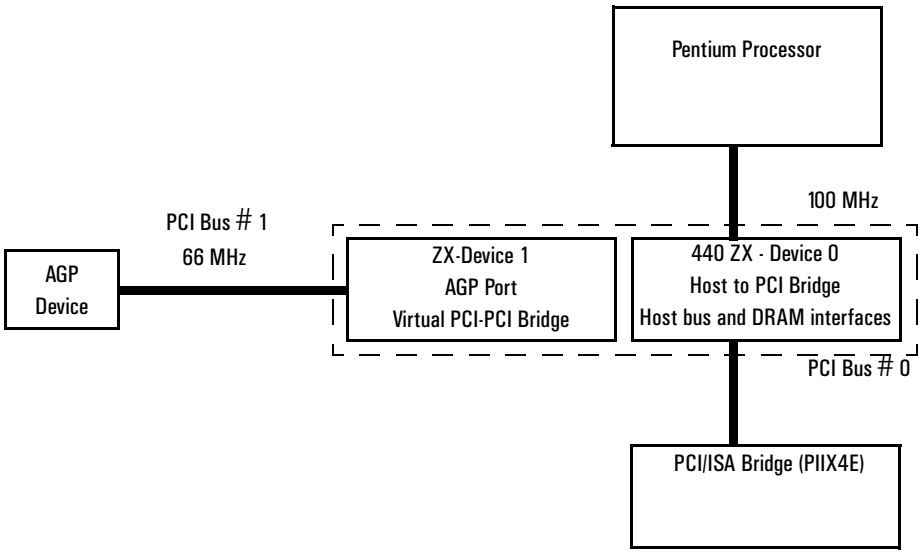
1. The texel scale factor is the ratio between the size of the rendered texture versus the size of the source texture.

Full Scene Anti-aliasing

Full scene anti-aliasing is a technique where all low resolution aliasing artifacts are removed from the image. This is done in an independent manner, meaning that it is application independent. Full scene anti-aliasing removes "jaggies" from rendered scenes so that images in CAD, animation and 3D appear smooth and realistic.

AGP PCI Bus Implementation

In the diagram below, the AGP Bus is viewed as a PCI bus with extra data lines.



Matrox Millennium G250 AGP Graphics (some VL600 PCs)

Powered by the speed-graded Matrox G250 chip, the Millennium G250 offers faster 2D and 3D performance than the Millennium G200, thanks to its 83MHz 2D graphics clock and its 105Mhz 3D graphics clock. This increase in speed offers higher performance in graphics-intensive applications such as Web browsing. An AGP 2X card with 8 MB of SGRAM, the Millennium G250 is equipped with all of the features of the Millennium G200. Performance is further enhanced with the optional 8 MB SGRAM upgrade, which enables 24-bit true color at resolutions up to 1920 x 1200. This upgrade card also runs 3D applications at as much as 1280 x 1024 at 32-bpp double buffered with a 32-bit Z-buffer.

Matrox Millennium G400 AGP Graphics (some VL600 PCs)

The Matrox Millennium G400 is an AGP 4X graphics controller designed to make maximal use of the AGP 4X's 1GB/sec bandwidth. As graphics applications become more demanding, data transfer rates must increase in order to support the growing bandwidth requirements of these applications.

The Matrox G400 acts as a unique multi-threaded AGP 4X bus master that is capable of using Direct Memory Access (DMA) to fetch commands and data from multiple locations in memory. This feature balances the needs of next generation 3D applications to send command data, vertex data and texture data from different areas in memory across the AGP bus to the graphics engine. In addition, the Matrox G400 is able to avoid long latencies in data fetching across the AGP bus. Large buffers inside the Matrox G400 allow it to initiate Extended Burst Transactions on the AGP 4X bus for highly optimized data flow. The combination of these features allows the Matrox G400 to sustain high, effective bandwidth on the AGP bus for high performance in real-life applications. The Matrox G400 also supports AGP texturing, pipelining, side band signaling, and AGP 4X transactions.

256-bit DualBus Architecture

Building on the success of the MGA-G200's 128-bit DualBus architecture, the Matrox G400 doubles the engine bandwidth by moving to a full 256-bit DualBus architecture, composed of two independent unidirectional 128-bit buses working in parallel inside the chip. Coupled with a high-speed 128-bit bus to external memory, the Matrox G400 256-bit DualBus architecture delivers very high 2D performance, surpassing the performance of traditional 128-bit architectures. While the 256-bit DualBus provides the largest direct gain in 2D performance, it is also used to accelerate all other data types, including 3D and video.

One of the benefits of the DualBus architecture is dual command pipelining, a feature that delivers fast and efficient data transfer by preventing empty, or wasted, cycles between commands. Dual command pipelining avoids the latency experienced with the traditional 128-bit bus by allowing the Data In buffer to begin sending the next command to the engine while the Data Out buffer finishes

reading the results from the current command. Since the next piece of data to be processed by the engine is always available in the Data In buffer, it can be sent to the engine right away. This ensures a continuous, uninterrupted flow of instructions/commands to the engine.

Vibrant Color Quality (VCQ) Rendering

The VCQ rendering engine in the Matrox G400 was designed to ensure that multi-textured applications are rendered with the same Vibrant Color Quality achieved with single texturing on the MGA-G200. Multi-texturing requires the combination or blending of many textures onto a single polygon. Without proper care, precision can be lost on each texture pass and the resulting image suffers from cumulative rounding errors and ugly dither patterns. The VCQ engine addresses this issue with increased precision and buffering throughout all of the internal 3D pipelines.

Symmetric Rendering Architecture (SRA)

Similar to the MGA-G200, the Matrox G400 uses a Symmetric Rendering Architecture (SRA) to take advantage of the high bandwidth made available by the AGP 4X bus. Within the SRA, the Matrox G400 treats AGP memory exactly as if it were local video memory, meaning that in a fully bus mastered fashion, the Matrox G400 can draw to, render to and read from AGP memory at AGP 4X transfer rates. By using the SRA as a key component of 3D, 2D and video operations, the Matrox G400 benefits from the 1GB/sec bandwidth provided by the AGP 4X bus in parallel with local video memory to achieve an optimal performance level in all application areas. To alleviate some of the drain on local memory, the SRA uses a hierarchical texturing system which stores textured and bitmapped surfaces across three levels: the large on-chip cache, local video memory of 32MB and AGP memory. Within the hierarchical texturing system, small and frequently used textures are usually mapped from local memory while large and infrequently used textures are mapped using AGP texturing from AGP memory. Supported by the chip's intelligent memory controller and the driver's intelligent memory management and allocation scheme, the hierarchical texturing system ensures that available memory resources are maximized and used with utmost efficiency. In addition, the SRA is designed to take advantage of the local video memory pool of 32MB, meaning that users benefit from high resolution triple buffering and

extra texture storage. Two-dimensional bitmaps benefit from the SRA in the same way that 3D textures do. In addition, the Matrox G400 expands the amount of fast access memory available for bandwidth-intensive video compression and decompression operations by writing to AGP memory at AGP 4X speeds.

DualHead Display

DualHead Display is a new technology in the Matrox G400 which allows a single chip to ouput two physically separate images simultaneously to two different output devices. The DualHead Display is quite versatile in its ability to support simultaneous output either to two RGB monitors, to an RGB monitor and a television set, to an RGB monitor and a Digital Flat Panel or to two analog Flat Panels. DualHead Display takes advantage of a new Windows 98 feature which allows a single board to support a Windows desktop spanning multiple monitors. In addition, DualHead Display offers enhanced performance for DVD viewing, design applications, video editing, and web browsing.

SiS Super AGP Graphics (VEi 7 PCs)

SiS super AGP graphics is an integrated 3D graphics system built in to the SiS 620 chip. Super AGP has the following features:

Integrated 2D Accelerator

The integrated 2D accelerator is a 64-bit BITBLT graphics engine. It supports all 256 raster operations and DirectDraw. The accelerated primitives include: BLT, Transparent BLT, Color expansion, Clipping, Multiple scanline, Polylines, Patterns, Trapezoid Fills. Up to 8MB of frame buffer can be used with linear addressing.

Integrated 3D Accelerator

The integrated 3D graphics accelerator is composed of the triangle setup engine and the rendering engine. The hardware acceleration features can be enabled by the SiS driver under Direct 3D and OpenGL. Supported 3D quality acceleration includes: Gouraud Shading, Z buffer, Alpha buffer, Perspective Correction, MipMapping, Tri-linear Texture Filtering, Specular Lighting and Dithering.

Integrated Graphics Accelerator

The integrated graphics accelerator is compatible with AGP1.0 and PCI 2.2 configurations. Display memory can be up to 8MB of SGRAM.

The super AGP architecture provides a bandwidth of 800MB/s between VGA and the host bus, an increase of 50% compared with AGP 2X mode (532MB/s). The display memory interface bus frequency can also be operated at up to 100MHz, with a 64-bit data path.

Crystal Integrated PCI Audio

The Crystal® integrated PCI audio solution in the PC is a two-chip solution made up of the CrystalClear™ CS4280 PCI audio controller and the CrystalClear CS4297 Audio Codec '97. The audio controller interfaces with the PCI bus and performs all digital operations such as sample rate conversions and synthesis. The CS4297 chip mixes and processes all the analog signals. A typical signal-to-noise ratio is 95 dB, compared with 85 dB at best for ISA audio solutions.

High fidelity audio is achieved through features such as differential CD audio input, which cancels out PC activity noise. In addition, the system's converters use a highly efficient over-sampling scheme to perform 18 bit analog-to-digital and digital-to-analog conversion. Through its use of DirectX, this Crystal audio solution offers high-end audio features such as 3-D localization, surround sound, room effects and Doppler effect.

The Crystal PCI audio solution includes an integrated FM synthesizer, Plug-and-Play interface and power management features. There is an internal connection for CD-ROM and DVD drives, and external stereo in, stereo out and microphone in sockets. Crystal audio is not SoundBlaster compatible.

The Crystal audio solution has been optimized for Windows-based platforms, while supporting the other major operating systems. It is therefore fully compatible with any application written for a Windows environment. Moreover, it is possible to play back virtually any PC audio format using Microsoft's Media Player 6. This player can process new formats through the use of plug-ins and can decode the following formats by default:

File Formats	File Extension
Midi files (music synthesis)	.rmi .mid
MOD tracker files (enhanced music playback)	.mod

File Formats	File Extension
Windows audio files	.wav .asx .asf
RealAudio and RealVideo streams	.ra .ram .rm .rmm
AVI (Audio Visual Interleave) video files	.avi
MPEG video files	.mpg .mpeg .m1v .mp2 .mpa .mpe
QuickTime® audio video files	.qt .aif .aifc .aiff .mov
Sun™ Microsystems and NeXT™ audio files	.au .snd

CS4280 PCI Audio Interface Features

- PCI Version 2.1 Bus Master
- Windows® 95, Windows 98, Windows NT 4.0, Windows NT 5.0 (WDM) Drivers
- PC'97 and PC'98 Compliance
- MPU-401 interface, FM synthesizer, and Game Port
- Full duplex operation
- Advanced Power Management (PPMI)

CS4297 Audio Codec '97 Features

- AC'97 1.03 compatibility
- Sophisticated mixed signal technology
- 18-bit stereo full-duplex Codec with fixed 48kHz sampling rate
- High quality differential CD input
- Mono microphone input
- Two analog line-level stereo inputs for LINE IN and CD (or VIDEO) connection
- Single stereo line level output
- Extensive power management support
- Meets Microsoft's PC'97 and PC'98 audio performance requirements

Network Features

The LAN cards described in this section are qualified for use with your PC. To order one of these products, refer to HP's Web site at: **www.hp.com/go/pcaccessories**.

HP 10/100 3Com 3C905C-TX Network Interface Card - D7522A and D7523A (pack of 10)

This network interface device is integrated on the riser card on some models. To see whether a PC has integrated networking, refer to the *Technical Reference Manual - Vectra Product Line Overview*.

Card Features	
LAN Interface	• 32 bits PCI 10/100 BT • RJ 45 LAN port
Power Management	• RPO (Remote Power-On) and RWU (Remote Wake-Up) for APM Windows 95 and Windows 98 (SR # 1 only), Windows NT 4.0; RWU for ACPI 98SE • On Now 1.0; APM 1.2; ACPI 1.0 • PCI Power Management 1.1, PCI 2.2
Manageability	• DMI 2.0 Component Code • WfM 2.0 Bootrom
Diagnostics	• Production Diag • MAC address DOS report tool • User Diag for MS-DOS, Windows 95, Windows 98 and Windows NT 4.0
Drivers	Windows 95, Windows 98, Windows NT 4.0, Windows 3.11, OS2 (Warp4), MS-DOS, Novell support
Specifications	
Network Interface	• 10 Mbps Ethernet 10BASE-T: Ethernet IEEE 802.3 industry standard for a 10 Mbps baseband CSMA/CD local area network. • 100 Mbps Ethernet 100BASE-TX: Ethernet IEEE 802.3u industry standard for a 100 Mbps baseband CSMA/CD local area network.
Physical Dimensions of the card	• Height: 8.57 cm (3.75 in.) • Length: 12.07 cm (4.75 in.)

HP 10/100 Intel PRO/100+ Management Adapter - D7506A and D7507A (pack of 10)

Card Features	
LAN Interface	• 32 bits PCI 10/100 BT • RJ 45 LAN port
Power Management	• RPO (Remote Power-On) and RWU (Remote Wake-Up) for APM Windows 95 and Windows 98 (SR #1 only); RWU for ACPI 98SE • On Now 1.0; APM 1.2; ACPI 1.0 • PCI Power Management 1.1, PCI 2.2
Manageability	• DMI 2.0 Component Code • WfM 2.0 Bootrom
Diagnostics	• Production Diag • MAC address DOS report tool • User Diags for MS-DOS, Windows 95, Windows 98 and Windows NT 4.0
Drivers	Windows 95, Windows 98, Windows NT 4.0, Windows 3.11, OS2 (Warp4), MS-DOS, Novell support
Specifications	
Network Interface	• 10 Mbps Ethernet 10BASE-T: Ethernet IEEE 802.3 industry standard for a 10 Mbps baseband CSMA/CD local area network. • 100 Mbps Ethernet 100BASE-TX: Ethernet IEEE 802.3u industry standard for a 100 Mbps baseband CSMA/CD local area network.
Physical Dimensions	• Height: 5.1cm (2.01 in.) • Length: 12.1cm (4.76 in.)

HP 10/100 BT PCI Ethernet Adapter - D7508A and D7509A (pack of 10)

Card Features	
LAN Interface	• 32 bits PCI 10/100 BT • RJ 45 LAN port
Power Management	• RPO (Remote Power-On) and RWU (Remote Wake-Up) for APM Windows 95 and Windows 98 (SR #1 only); RWU for ACPI 98SE • On Now 1.0; APM 1.2; ACPI 1.0 • PCI 2.2
Manageability	• DMI 2.0 Component Code • WfM 2.0
Diagnostics	• Production Diag • MAC address DOS report tool • User Diags for Windows 95, Windows 98 and Windows NT 4.0
Drivers	Windows 95, Windows 98, Windows NT 4.0, MS-DOS, Novell support
Specifications	
Network Interface	• 10 Mbps Ethernet 10BASE-T: Ethernet IEEE 802.3 industry standard for a 10 Mbps baseband CSMA/CD local area network. • 100 Mbps Ethernet 100BASE-TX: Ethernet IEEE 802.3u industry standard for a 100 Mbps baseband CSMA/CD local area network.
Physical Dimensions	• Height: 5.3 cm (2.11 in.) • Length: 12 cm (4.72 in.)

LAN Card Ready Program

The HP LAN Card Ready (LCR) Program provides drivers and installation information for LAN cards by third-party manufacturers that have been tested on your PC.

By using the exact configuration tested by HP, you will be able to install the LAN card more quickly and avoid many of the problems that can occur due to resource conflicts and incompatible driver revisions.

Follow the **LAN Card Ready** link from HP's Support Web site at: **www.hp.com/go/vectrasupport** to access LAN information and drivers tested on your PC.

Input Devices

Standard HP Keyboard

The standard HP keyboard has the following features:

- Euro symbol available on selected localizations if supported by the operating system (Windows 98, Windows 2000). See Microsoft's Web site for more details
- 6-pin Mini-Din style Keyboard with Windows keys
- Available in 30 languages
- Power on function from the space bar supported on some PC models
- Includes 12 function keys, numeric keypad and cursor keys

The standard keyboard kit includes 1 keyboard with 104 or 105 keys and a *Working in Comfort* booklet.

Enhanced HP Keyboard

The enhanced HP keyboard has a number of multimedia features not present on a standard keyboard. You can, for example, connect a headset and microphone to the keyboard. In this instance the headset and microphone cables supplied with the keyboard must be connected to the appropriate PC connectors.

You can control and mute the PC's audio volume, put the PC in suspend or lock mode, launch a Web browser or use programmable QuickLaunch keys to launch applications open files or perform other actions.

Scrolling Mouse

The HP Scrolling Mouse provides the following benefits:

- Quicker and smoother scrolling through screens of information
- Immediate zooming on data without having to action scrollbars, menus or buttons
- Full functionality on supporting applications, including Microsoft Office 97

You can easily configure the scrolling wheel to take full advantage of the functionality provided by an increasing number of applications or simply use it as a third button.

The scrolling mouse kit includes 1 scrolling mouse and 2 driver floppies.

Specifications

- PS/2 compatible mouse with rubber scrolling wheel, including mini-DIN connector
- Allows scrolling in Windows 95, 98, NT applications (not only Office 97-compatible applications)
- Allows configuration of the wheel as a 3rd button.

Connectors and Sockets

IDE and Floppy Disk Drive Connectors

IDE Connector			
Pin	Signal	Pin	Signal
1	Reset#	2	Ground
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	Ground 7	20	orientation key
21	DMARQ	22	Ground 2
23	DIOW#	24	Ground 3
25	DIOR#	26	Ground 4
27	IORDY	28	CSEL
29	DMACK#	30	Ground 5
31	INTRQ	32	IOCS16#
33	DA1	34	PDIAG#
35	DA0	36	DA2
37	CS1FX	38	CS3FX
39	DASP#	40	Ground 6

Floppy Disk Drive Data Connector			
Pin	Signal	Pin	Signal
1	Ground	2	LDENSEL#
3	Ground	4	Microfloppy
5	Ground	6	EDENSEL
7	Ground	8	INDX#
9	Ground	10	MTEN1#
11	Ground	12	DRSEL0#
13	Ground	14	DRSEL1#
15	Ground	16	DTEN0#
17	Ground	18	DIR#
19	Ground	20	STP#
21	Ground	22	WRDATA#
23	Ground	24	WREN#
25	Ground	26	TRK0#
27	Ground	28	WRPRDT#
29	Ground	30	RDDATA#
31	Ground	32	HDSEL1#
33	Ground	34	DSKCHG#

Status Panel Connector (where available) and USB Stacked Connector

Status Panel Connector			
Pin	**Signal**	**Pin**	**Signal**
1	Red Led	2	Green Led
3	Reset	4	Lock
5	Ground	6	Power Leds
7	On_Off Button	8	Lan Led
9	Lock Leds	10	IDE/SCSI Led

USB Stacked Connector			
Pin	**Signal**	**Pin**	**Signal**
1	USB0 Power	2	USB0 Neg.
3	USB0 Pos.	4	Chassis Ground
5	USB1 Power	6	USB1 Neg.
7	USB1 Pos.	8	Chassis Ground
9	Chassis Ground	10	Chassis Ground
11	Chassis Ground	12	Chassis Ground

VL600 Status Panel Connector			
Pin	**Signal**	**Pin**	**Signal**
1	N.C.	2	Green Led
3	3.3 V STDBY	4	Key
5	+ 5 V	6	IDE/SCSI Led
7	Ground	8	On_Off Button
9	+ 5 V	10	Lock Leds

Power Supply Connector

14-pin Power Supply Connector for System Board			
Pin	**Signal**	**Pin**	**Signal**
1	PwrGood	2	
3	Remote On	4	Ground
5	Ground	6	Ground
7	+12 Volt supply	8	5V STDBY
9	+5 Volt supply	10	+5 Volt supply
11	+5 Volt supply	12	-12 Volt supply
13	-5 Volt supply	14	Stop Fan Bit

20-pin Power Supply Connector for System Board			
Pin	**Signal**	**Pin**	**Signal**
1	+ 3.3 Volt supply	2	+ 3.3 Volt supply
3	Ground	4	+5 Volt supply
5	Ground	6	+5 Volt supply
7	Ground	8	PwrGood
9	5V STDBY	10	+12 Volt supply
11	+ 3.3 Volt supply	12	-12 Volt supply
13	Ground	14	Remote On
15	Ground	16	Ground
17	Ground	18	N.C.
19	+5 Volt supply	20	+5 Volt supply

Power Supply 3V3 for System and PCI Wakeup Connector (where available)

Power Supply 3V3 for System			
Pin	Signal	Pin	Signal
1	Ground	2	Ground
3	Ground	4	+ 3V3 Volt supply
5	+ 3V3 Volt supply	6	+ 3V3 Volt supply

PCI Wakeup (J25)	
Pin	Signal
1	Ground
2	PCI Wakeup
3	Ground

Power Supply 3V3 and Fan Connector (where available)

Power Supply 3V3 on Backplane (where appropriate)			
Pin	Signal	Pin	Signal
1	+ 3V3 Volt supply	2	+ 3V3 Volt supply
3	Ground	4	Ground

Fan Connector	
Pin	Signal
1	Ground
2	12V Power
3	Control Signal

ExtStart Connector (where available)

ExtStart Connector (J24)			
Pin	Signal	Pin	Signal
1	SCSI Led	2	Ultra SCSI
3	Ring	4	Ground
5	LAN Wake	6	VStandby Modem
7	Enable Remote On	8	LAN Start
9	External Reset	10	LAN Led
11	VStandby	12	
13	Not connected	14	Not connected

VL600 Power Fan Connector	
Pin	Signal
1	Ground
2	Control Signal
3	Fan detection

External Audio Connectors

A Line In jack, Line Out jack and Mic In jack connector are located on the PCs' rear panel. These external jacks are standard connectors.

Internal Speaker Connector and Package Intrusion Connector (where available)

Internal Speaker (J18)	
Pin	**Signal**
1	Speaker Signal
2	Analog Ground

Package Intrusion (J8)	
Pin	**Signal**
1	Open detect
2	Ground

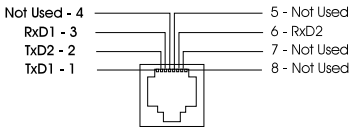
VL600 Package Intrusion	
Pin	**Signal**
1	VCC-RTC
2	Open detect
3	Ground
4	Box ID (MT-DT)

VGA DB15 Connector

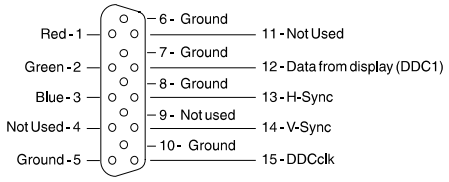
VGA DB Connector Pins		
Pin	**Standard VGA**	**DDC2B**
1	Analog RED	Analog RED
2	Analog GREEN	Analog GREEN
3	Analog BLUE	Analog BLUE
4	Monitor ID2	Monitor ID2
5	n/c	DDC return
6	Analog RED return	Analog RED
7	Analog GREEN return	Analog GREEN
8	Analog BLUE return	Analog BLUE
9	n/c	V_{CC} supply (optional)
10	Digital ground	Digital ground
11	Monitor ID 0	Monitor ID 0
12	Monitor ID 1	Data:SDA
13	HSYNC	HSYNC
14	VSYNC	VSYNC
15	n/c	Clock:SCL

Socket Pin Layouts

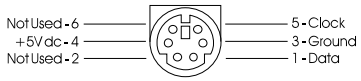
Ethernet UTP Connector



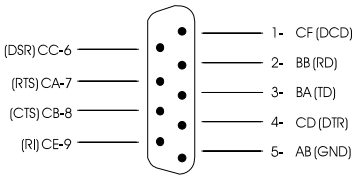
VGA Connector



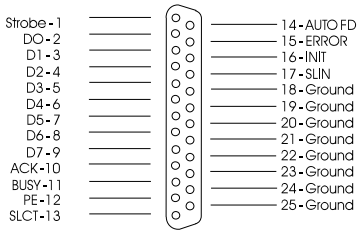
Keyboard and Mouse Connector



Serial Port Connector



Parallel Port Connector



The Technical Reference Manual contains the following documents available on the *HP Information CD-ROM* or downloadable from the Web in PDF format:

- Introduction & HP Vectra Product Line Overview
  Describes how to use the Technical Reference Manual and provides a brief overview of VEi, VL and VLi PCs.
- Product Description
  A separate document exists for VEi 7 models, VEi 8 models, VLi 8/VLi 8SF and VL600 models, providing detailed BIOS information and summary information on the hardware components in the PC.
- HP Vectra Technology
  The document you are reading. A detailed look at the hardware components in all the PCs in the product line. Includes information on processors, chip sets, graphics controllers, network cards, connectors and sockets.