Fuse protection of semiconductor diodes, thyristors, and triacs

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Techniques for matching the characteristics of fuses to the surge current capabilities of diodes, thyristors, and triacs are described. The effects of moderate overload conditions and high-current faults, together with the relationship of fuse arc voltage to peak reverse voltage, are considered. Examples of fuse selection for the BTW92 thyristor, based on energy let-through (I^2t) coordination are given.

INTRODUCTION

The article describes the principles of fuse protection of semiconductor devices. It does not cover every aspect of fusing, because many practical fusing techniques have already been established for many years. The article, therefore, restricts itself to the coordination of the fuse to the semiconductor device, and includes the principles of the short-circuited power line, fuse construction, and fuse characteristics.

Much has been written over the last thirty years on the characteristics and operation of fuses. In particular, the introduction of the so-called 'current-limiting fuse' has allowed the effective protection of electrical apparatus against the effects of a complete short-circuit. Previously, the current-limiting fuse was normally associated with heavy-duty electrical equipment. The introduction of the semiconductor power diode, thyristor, and triac created a new requirement for improved performance in fuse protection from short-circuit faults, because of the low overload capability of semiconductor devices.

The fundamental protection of semiconductor devices against high-current faults is achieved by the limitation of energy let-through I^2t, expressed in A^2s. The let-through of the fuse is compared with the I^2t withstand capability of the device as given in the semiconductor manufacturer's published data. There is evidence to indicate that the peak current let-through of the fuse, the wave-shape, and the time at which the peak occurs after the commencement of the short-circuit should correspond to the peak current and time withstand of the semiconductor device. However, this part of the process of matching a fuse to a semiconductor device is under continuous development.

SHORT-CIRCUITED A.C. POWER LINE

It is clear that a fuse must give reliable protection over a wide variety of overload conditions to satisfactorily protect the circuit and devices. In many examples of circuit protection, fuses are used in conjunction with circuit breakers. In this arrangement, the circuit breaker deals with moderate overloads, and the fuse deals with a high-current fault resulting from a circuit breakdown. For example, curves of surge current I_{FSM}(r.m.s.) against time are shown in Fig.1 for the BYX98 diode protected by an English Electric GSA10 fuse and a mechanical circuit breaker. It can be seen in Fig.1 that the fuse protects the diode and the circuit breaker against high-current surges of less than about 30ms duration, whereas the circuit breaker protects the diode and the fuse against low-current surges of longer duration. Fusing is of

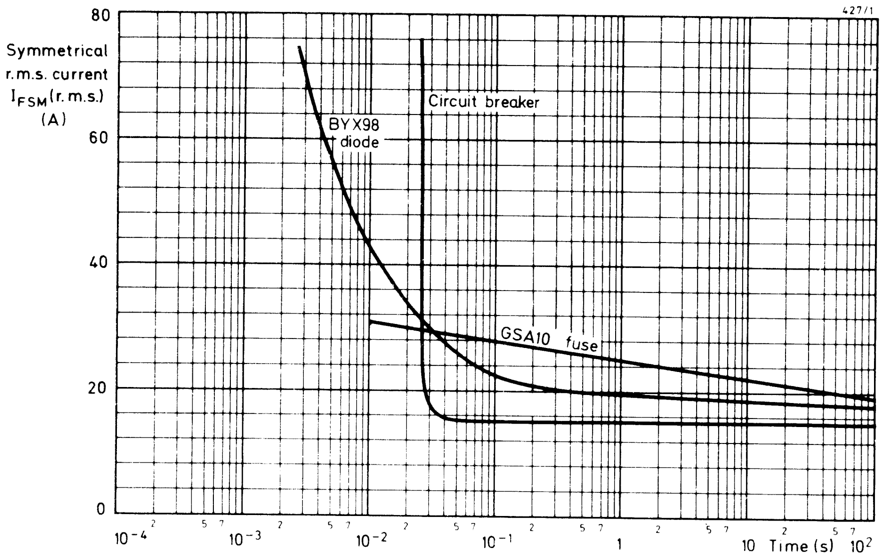


Fig.1 – Curves of surge current I_{FSM} (r.m.s.) against time for BYX98 diode protected by English Electric GSA10 fuse and mechanical circuit breaker

course required for d.c. as well as a.c. supplies, but most manufacturers derate a suitable a.c. fuse for this purpose, as described later.

Fig.2 represents a short-circuit occurring on a single-phase a.c. power line. The inductance L represents the inductive component of the line, including the leakage inductance of the substation transformer. The resistance R represents the resistive component. In high-power installations, the value of R is very low, and a short-circuited line is normally highly inductive. The ratio $\omega L/R$ has been standardised by the American National Electrical Manufacturers Association to a value of 6·66. This standardised value corresponds to a power factor (p.f.) of 0·15 (see Ref.1) for fuse and circuit breaker performance data. Similar standardisations apply in the United Kingdom and in other European countries.

The general equation for the instantaneous current i(t) is given below:

$$i(t) = \frac{E_{pk}}{Z}\left\{\sin(\omega t + \theta - \phi) - e^{-kt}\sin(\theta - \phi)\right\}, \qquad \ldots(1)$$

where: E_{pk} = peak value of the sinewave voltage,

Z = impedance of the line,

θ = angle at which the short-circuit occurs relative to the sinewave voltage zero,

ϕ = $\tan^{-1} \omega L/R$,

k = R/L.

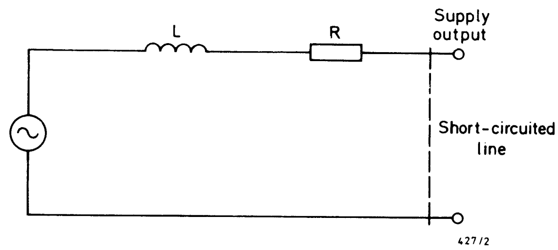


Fig.2 – Occurrence of short-circuit in a single-phase power line

Eq.1 consists of a steady-state term:

$$\frac{E_{pk}}{Z}(\sin \omega t + \theta - \phi),$$

and a transient term:

$$\frac{E_{pk}}{Z}\left\{-e^{-kt}\sin(\theta - \phi)\right\}.$$

When θ is equal to ϕ, that is where a short-circuit occurs at the lag-angle of the line, the transient term is equal to zero. This condition represents the 'steady-state' current-against-voltage relationship of an a.c. supply. The steady-state current i(t) is given by:

$$i(t) = \frac{E_{pk}\sin \omega t}{Z}. \qquad \ldots(2)$$

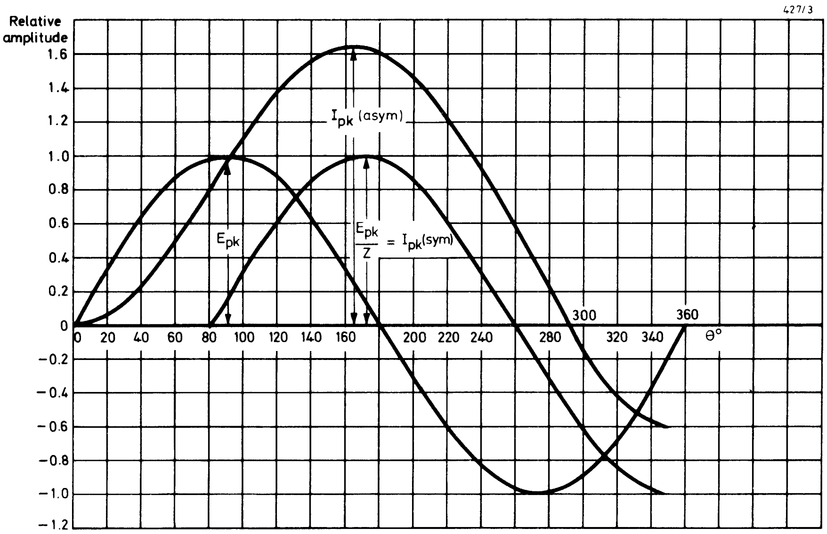


Fig.3 — Asymmetrical current and symmetrical current against supply voltage during one cycle

Fig.3 shows the waveforms of voltage, symmetrical current, and asymmetrical current derived from Eq.1 for a p.f. of 0·15. As indicated in Fig.3:

$$I_{pk}(\text{asym}) \simeq 1{\cdot}6 \times I_{pk}(\text{sym}), \qquad \ldots(3)$$

or

$$I_{pk}(\text{asym}) \simeq \sqrt{2} \times 1{\cdot}6 \times I_{rms}(\text{sym}),$$

$$\simeq 2{\cdot}3 \times I_{rms}(\text{sym}), \qquad \ldots(4)$$

where I_{pk}(asym) is the peak asymmetrical fault current, and I_{pk}(sym) is the peak symmetrical fault current.

As the p.f. increases towards unity, the peak value of the asymmetrical transient current decreases, and the asymmetrical and symmetrical peak currents tend to become in phase with the generated sinewave voltage.

Mains supply source with transient suppression filter

In many instances where thyristors are used in bridge circuit configurations direct from the mains supply, transient suppression filters are required to suppress spikes on the mains voltage waveform. These voltage spikes can cause spurious dV/dt or V_{BO} triggering. An example of a transient suppression filter connected to the supply line is shown in Fig.4, which is reproduced from Ref.2. The R_2, L_2, and C_1 circuit is chosen to be a nearly critically damped system by suitable choice of the three component values. Resistor R_3 is a high-value component which assists in the discharge of capacitor C_1. If a complete short-circuit occurs on the output side of the filter, the inductance L_2 and its associated resistance r_2 becomes part of the power line in terms of the prospective current generated. In high-power installations, the p.f. of the supply line is almost certain to be known, and the values of L_2 and r_2 may be added to the values of L_1 and R_1 for calculation purposes.

In practical terms, the significance of the symmetrical and asymmetrical short-circuit is the way in which the initial rate of rise of current affects the operation of the protective device. Where a fuse is the protective device, Ref.3 shows that there may be a difference in the peak current let-through under short-circuit conditions, depending on whether the current is symmetrical or

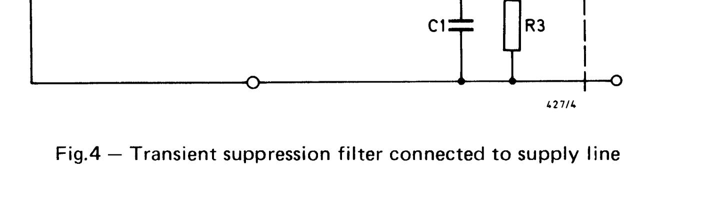


Fig.4 — Transient suppression filter connected to supply line

asymmetrical. Circuit breakers (described in Refs.4 and 5) may have interrupting capabilities which are also dependent on whether the current is symmetrical or asymmetrical.

Short-circuit capability in terms of the percentage of transformer leakage reactance

The percentage of leakage reactance is defined as:

$$X\% = \frac{100X_L}{R_L},$$

where X% is the percentage of leakage reactance of the total reactance X_L of the secondary winding, and R_L is the load resistance.

Usually the leakage reactance percentage is small (typically 2%) and only becomes significant under short-circuited load conditions.

The nominal volt-amp rating VA_{nom} of the transformer is given by:

$$VA_{nom} = E_{rms} I_{L(rms)},$$

$$= E^2_{rms}/R_L. \qquad \ldots(5)$$

The short-circuit VA rating VA_{sc} is given by:

$$VA_{sc} = E^2_{rms}/X_L. \qquad \ldots(6)$$

From Eq.6:

$$VA_{sc} = \frac{VA_{nom} \times 100}{X\%}, \qquad \ldots(7)$$

or

$$I_{(rms)sc} = \frac{I_{L(rms)} \times 100}{X\%}. \qquad \ldots(8)$$

The p.f. of the source is expressed as:

$$\text{p.f.} = R_1 \Big/ \left[\omega^2 L_1{}^2 + R_1{}^2\right]^{1/2}. \qquad \ldots(9)$$

If the p.f. is 0·15, then the values given in Eq.4 apply for I_{rms} and I_{pk}(asym).

FUSE CURVES

It will be appreciated from the foregoing section on the short-circuited a.c. power line that a great variety of short-circuit conditions can apply, depending on the p.f. of the line and at what point on the voltage waveform the short-circuit is initiated. Generally, the fuse performance curves given in the fuse manufacturer's published data are derived from worst-case conditions (see Ref.1). It follows that the conditions under which a fuse clears in a particular situation will probably produce less stress in the device or equipment to be protected than is indicated by the fuse performance curves.

It has been normal practice to present fuse performance in three principal sets of curves:

1) fusing current as a function of time (time-current curves),
2) fuse peak let-through current as a function of prospective current,
3) variation of total I^2t let-through as a function of prospective current.

An example of each of these sets of curves is shown in Figs.5, 6, 7a, and 7c.

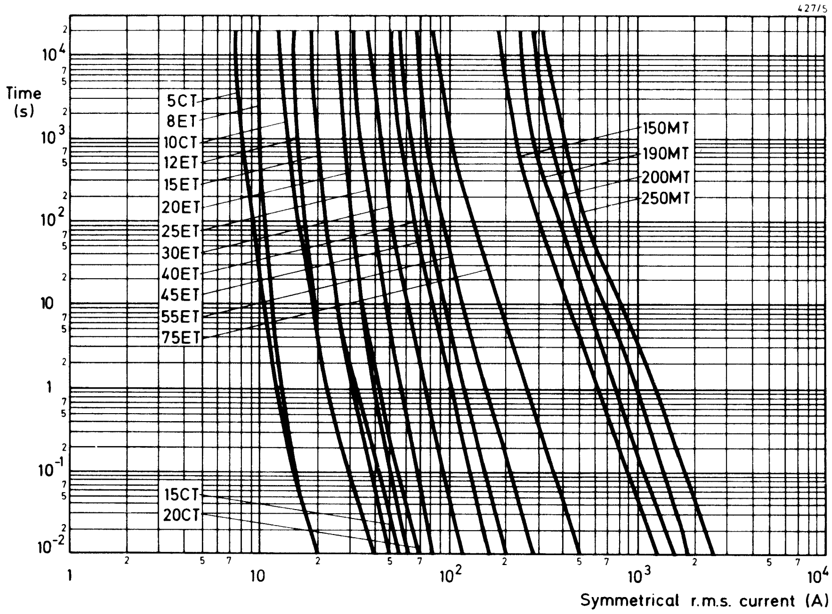


Fig.5 – Time-current curves for Brush type ET and type MT fuses

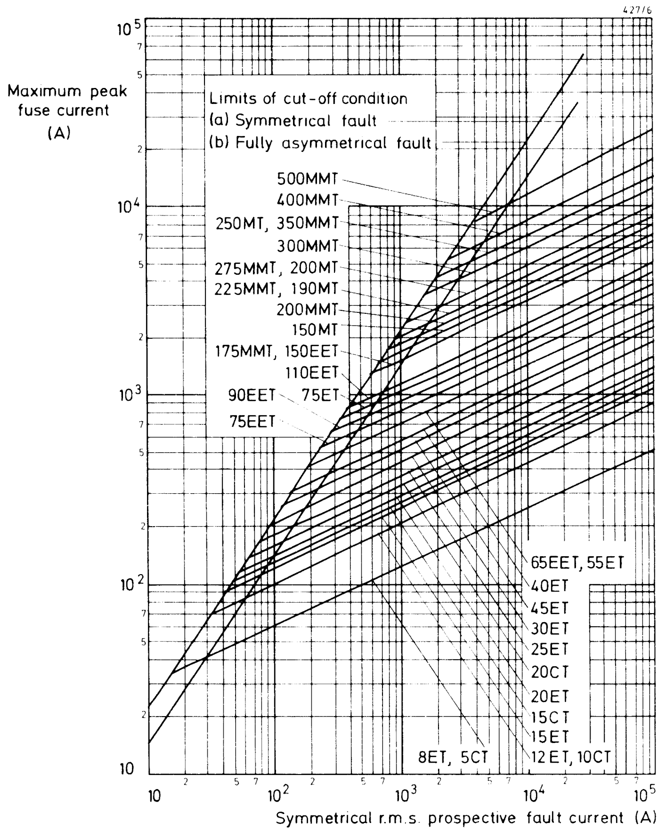
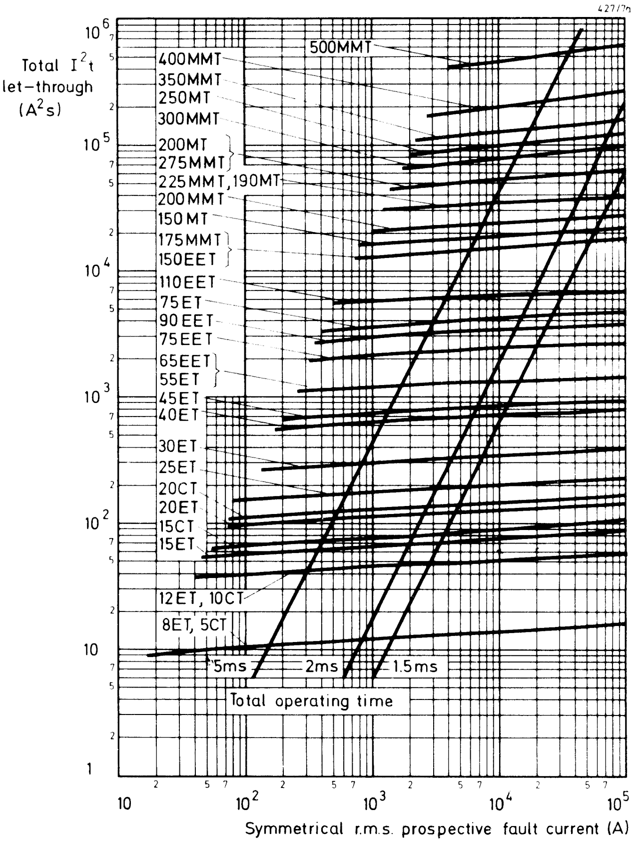
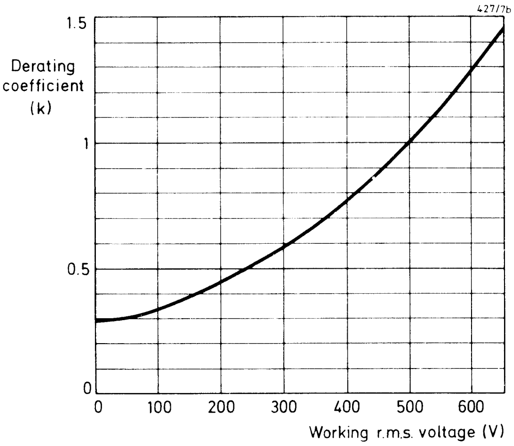


Fig.6 — Curves of fuse maximum peak current as a function of prospective fault current for Brush type ET and type MT fuses (cut-off characteristics at 457V r.m.s.)

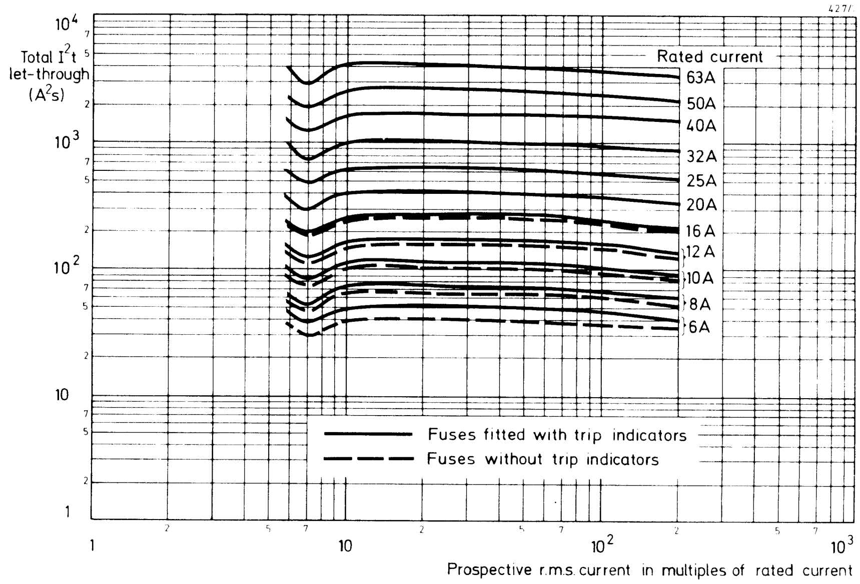
Fig.7 — Fuse performance curves.
Brush type ET and type MT fuses:
(a) total I^2t let-through as a function of prospective fault current at 457V r.m.s.
Ferraz 600V, type RE fuses:
(b) derating coefficient k to be applied to the total I^2t given in Fig.7c to obtain the I^2t as a function of the r.m.s. working voltage
(c) curves indicating maxima total I^2t as a function of prospective current. The curves are expressed in multiples of the rated current for operation under 500V at 50Hz


427/7a
Total I²t let-through (A²s)
500MMT
400MMT
350MMT
250MT
300MMT
200MT
275MMT
225MMT, 190MT
200MMT
150MT
175MMT
150EET
110EET
75ET
90EET
75EET
65EET
55ET
45ET
40ET
30ET
25ET
20CT
20ET
15CT
15ET
12ET, 10CT
8ET, 5CT
5ms
2ms
1.5ms
Total operating time
Symmetrical r.m.s. prospective fault current (A)

(a)


427/7b
Derating coefficient (k)
Working r.m.s. voltage (V)

(b)


427/
Total I²t let-through (A²s)
Rated current
63A
50A
40A
32A
25A
20A
16A
12A
10A
8A
6A
Fuses fitted with trip indicators
Fuses without trip indicators
Prospective r.m.s. current in multiples of rated current

(c)

Time-current curves

The time-current curves shown in Fig.5 are a function of the heating effect of the r.m.s. current through the fuse; that is, an i^2R function, where R is the resistance of the fuse. Over long periods, fuses have an inherent overload capability, defined by the term 'fusing factor'. This factor is the ratio of minimum fusing current to the rated current (see Ref.6). The minimum fusing current is defined as the current which would cause the fuse to operate in a four-hour period.

The time-current curves do not usually extend below 10ms. For times less than 10ms, the energy let-through depends considerably on the point on the voltage waveform at which the fault occurs, and the p.f. of the line. Consequently, in the 'sub-cycle' region, the curves are based on energy let-through, or I^2t values expressed in A^2s.

Peak let-through current

The fuse peak let-through is usually plotted from two boundary ordinates, signifying a symmetrical fault and a fully-asymmetrical fault, as shown in Fig.6. The maximum peak current characteristic for a rated fuse is derived from a multiplicity of circuit conditions (Ref.1). The peak current passed by a fuse is somewhat influenced by the fuse arc voltage characteristic and the system voltage, as indicated in Figs.8a and 8b. The relative arc voltage of the fuse against the relative system voltage is shown in Fig.8c. Therefore, the fuse melting time and the current flow in the pre-arcing interval do not accurately indicate the maximum peak let-through. In addition, a secondary effect concerning low-current fuses (Ref.7) is the modification of pre-arcing current to a lower rate of rise of fault current. This modification is due to the increased resistance in the line, caused by the high-temperature

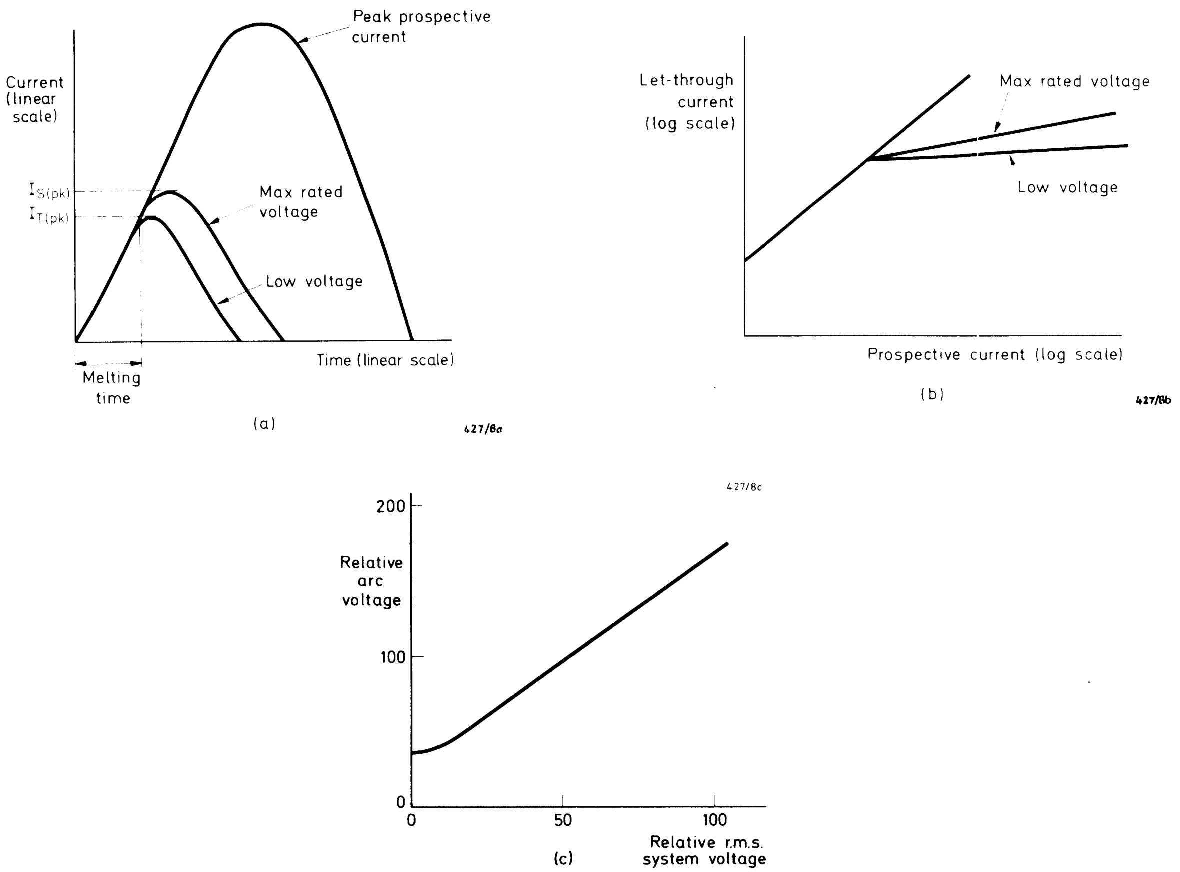


Fig.8 – Principal fuse parameters:
(a) peak prospective current at low voltage and maximum rated voltage,
(b) peak let-through against prospective current for low voltage and maximum rated voltage,
(c) relative arc voltage against relative system voltage

fuse element immediately before the melting point of the silver element is reached at 960°C.

I^2t let-through curves

Performance curves are shown in Fig.7a for Brush type ET and type MT fuses, and in Figs.7b and 7c for Ferraz 600V type RE fuses. The curves indicate maximum I^2t values for a given supply voltage and a low-p.f. circuit. As described later, the I^2t let-through curves represent the sum of the melting I^2t and the arcing I^2t of a particular fuse. The arcing I^2t is particularly dependent on the supply voltage, and fuse manufacturers include voltage derating graphs in their published data. An example of such a derating graph is shown in Fig.7b, subsidiary to the main graph of I^2t let-through against prospective fault current (see Fig.7c). The subsidiary graph is used to derate the total I^2t let-through of the fuse by a fractional factor (k in Fig.7b) as the supply voltage decreases from the maximum-rated value of the fuse. Other manufacturers give I^2t curves for specific test voltages (for example, see Fig.7a). The starting point of an I^2t let-through curve usually corresponds to the onset of current limiting action of the fuse. It is here that the total I^2t let-through has a minimum value (see Fig.7c). As the prospective fault current decreases, the I^2t let-through rises again until it approaches an infinite value for the rated current of the fuse.

Another set of curves which fuse manufacturers have made available in recent years is the fuse clearance times as a function of prospective current. These curves represent an important contribution to the effective protection of semiconductor devices. The value of I^2t withstand for times of 10ms or less may not be a constant value for many types of diode, thyristor, and triac. Information correlating I^2t let-through and fuse clearing time for a given prospective current against I^2t withstand as a function of time for the semiconductor device is of great assistance in assessing fuse protection. An example of the method of presenting fuse clearance time as a function of prospective current is shown in Fig.9 for Ferraz 600V, type RE fuses. Fuse operating times are also given in the Brush I^2t let-through curves shown in Fig.7a. It can be seen from Figs.7a and 9 that fuse clearance can be achieved in very short periods, typically considerably less than 10ms (half-sinewave period at 50Hz).

Fuse standardisation

The general properties, rating, and testing of fuses are now embodied in IEC Recommendations (Ref.8). Publication 269-4, Part 4: 'Supplementary requirements for fuse-links for the protection of semiconductor devices' deals specifically with fuses intended for semiconductor device protection.

FUSE CONSTRUCTION AND OPERATION

The construction of a typical fuse designed for current limiting, and in particular for semiconductor device protection, is shown in Fig.10 (see also Ref.9). The fusing element is usually made of silver to ensure very low ohmic resistance. Typical shapes of fuse elements are shown in Figs.11a and 11b. V-shaped notches are made in the element to produce a number of constrictions, and the fusing action takes place at one or more of

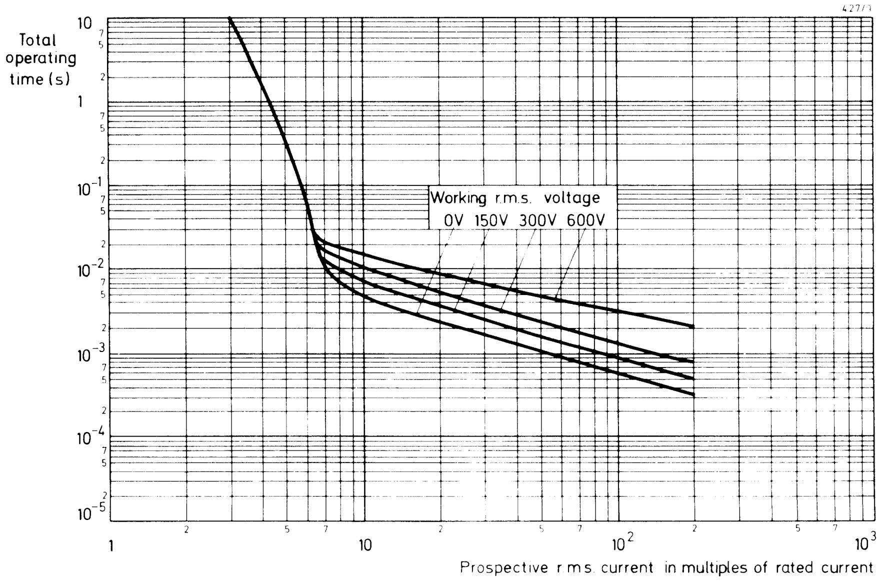


Fig.9 — Total operating time as a function of the prospective current, in multiples of the rated current, and for different r.m.s. working voltages for Ferraz 600V, type RE fuses. The 0V curve relates to pre-arcing time

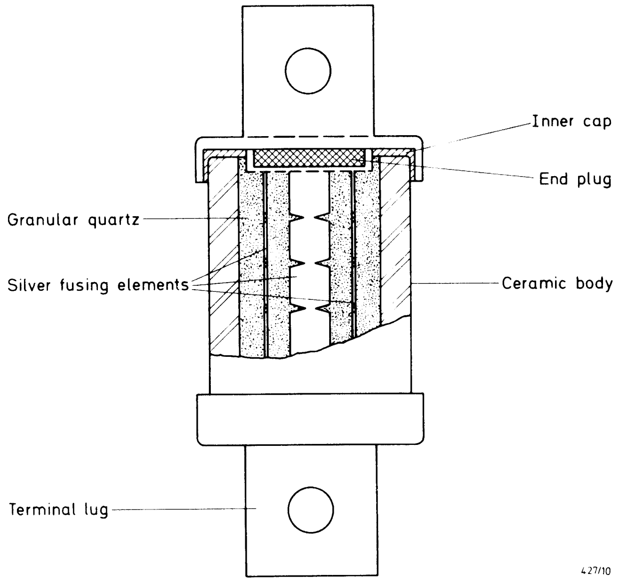


Fig.10 – Cut-away drawing of typical fuse for semiconductor protection

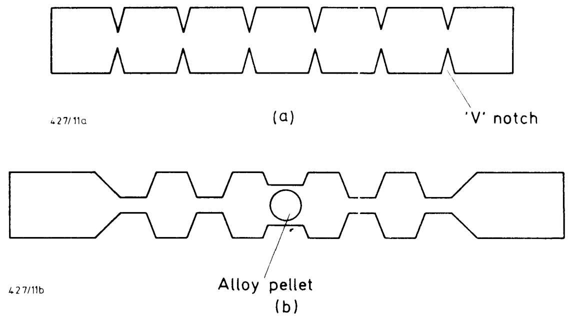


Fig.11 – Typical shapes of elements used in fuses for:
(a) semiconductor protection,
(b) industrial use

these constrictions. The v-shaped notch is chosen instead of rectangular- or semicircular-shaped notches for two principal reasons. First, it combines minimum heat generation with maximum heat dissipation at the minimum cross-section. Consequently, the v-shaped section can carry the greatest overload current. Second, elements with v-shaped notches show a considerably reduced I^2t (arcing) tendency than elements with notches of other shapes. The element shown in Fig.11a is used primarily for the short-circuit protection of semiconductor devices. The element in Fig.11b is intended for industrial use and may have one or more alloy pellets mounted on its surface. On moderate overload current (see Ref.7) the pellets become alloyed to the silver, resulting in a lower melting point. This effect causes a marked shift in the time-current curves for moderate overloads. Short-circuit interruption capability is unaffected. Improvement in performance and economy of size for a given amp-rating is obtained by using parallel-mounted elements in the same housing as shown in Fig.10.

Contained in the body of the fuse is a granular quartz filler for extinguishing the resultant arc which forms as the element breaks at a constriction. The quartz filler enables the heat generated by the arc to be conducted axially and radially to the body of the fuse casing. The resultant silver vapour formed during the arcing combines with the quartz filler to form a non-conducting material called fulgurite.

The material used for the tag and cap of the fuse is usually brass or copper, and the body is usually a ceramic-based material which will withstand high thermal shock.

At sufficiently high short-circuit currents, the element melts. The theoretical energy required to melt the element at one of the constrictions formed by a notch is given by:

$$E_j \text{ (joules)} = \int_0^{t_1} i^2 R \, dt, \qquad \ldots (10)$$

where R is the mean fuse resistance, and t_1 is the melting time limit (see Ref.2). E_j and R in Eq.10 are combined in one constant K given by:

$$K = E_j/R.$$

Therefore:

$$K = \int_0^{t_1} i^2 \, dt, \qquad \ldots (11)$$

where K is expressed in A^2s.

During the arcing period, the arc voltage can be considerably higher than the mains supply voltage, depending on the element design. The additional voltage is supplied by the trapped inductive energy of the circuit. The magnitude of the arc voltage is instrumental in forcing down the magnitude of the fault current, but the value of the arc voltage is carefully controlled to avoid stressing of associated equipment. For example, the fuse arc voltage should not exceed the peak reverse voltage of the diode, thyristor, or triac in the circuit, and for this reason the ratio of maximum arc voltage to system voltage is supplied by the fuse manufacturer.

Fuse testing system

A typical system which is used for short-circuit testing of fuses is shown in Fig.12. A high VA capacity alternator is operated into step-down transformer T_1. Connected between the alternator and the transformer is a network comprising potentiometer R_1 and air-cored variable inductor L_1. The network is adjusted to set up a known value of p.f. Control switch S_1 enables the circuit to be completed at any point on the voltage sinewave. By controlling the p.f., supply voltage, and switching point, a wide range of fusing conditions can be simulated, from which worst-case conditions can be evaluated for fuse curves.

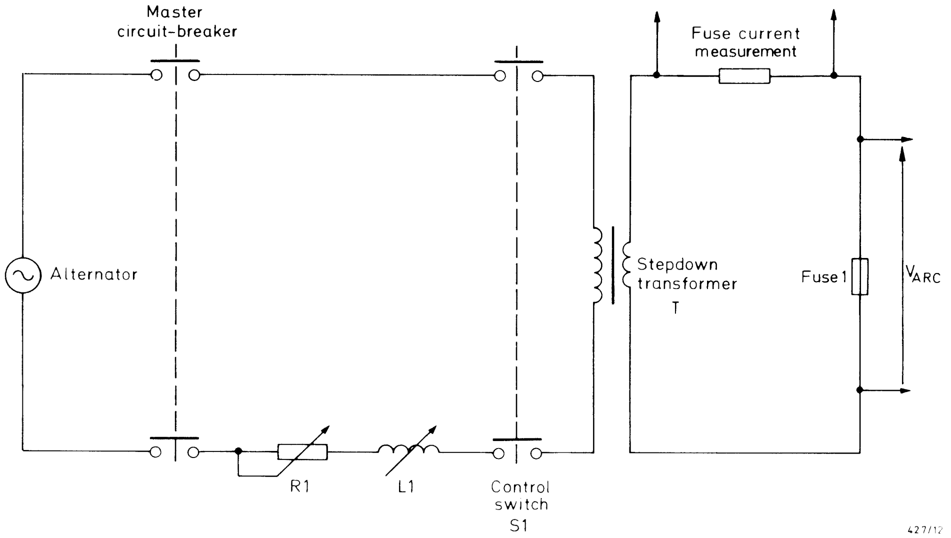


Fig.12 — Typical system used for short-circuit testing of fuses

D.C. OPERATION OF FUSES

Discussion has centred so far on fuses operating on a.c. supplies, and it is in this situation where most fuses are used. Under d.c. conditions there is an absence of voltage zero points, but for high-current fault conditions in d.c. circuits having a low time-constant, fuse clearing times can be similar to those for a.c. circuits. However, for d.c. circuits with lower fault currents and larger time-constants, voltage derating of the fuse will be necessary. Consequently, there is no direct relationship between a.c. and d.c. fusing systems (see Refs.10 and 11).

A specialised d.c. application of fuses intended for semiconductor device protection is in inverter circuits using thyristors. In these circuits, commutation failure due to excessive load current can occur. This type of failure can result in two conducting devices being placed across the d.c. line. Individual fuse protection of each device can be used in a similar manner to branch fusing.

For d.c. circuits with typical time-constants, the peak let-through current of the fuse is less than the peak let-through current for worst-case conditions in a.c. operation. The curve shown in Fig.13 gives an indication of the ratio of d.c. peak let-through current to a.c. peak let-through current as a function of the circuit d.c. time-constant.

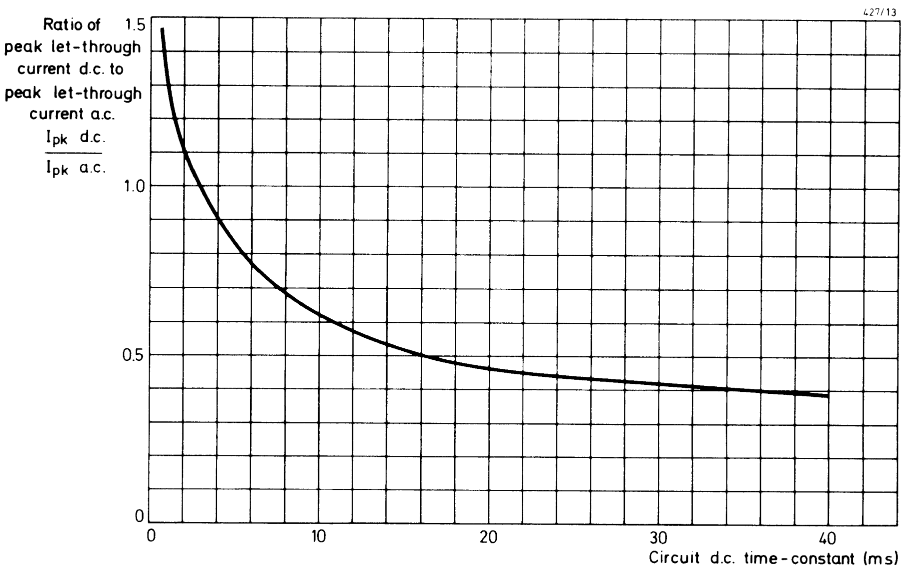


Fig.13 — Ratio of peak let-through current d.c. to peak let-through current a.c. against circuit d.c. time-constant

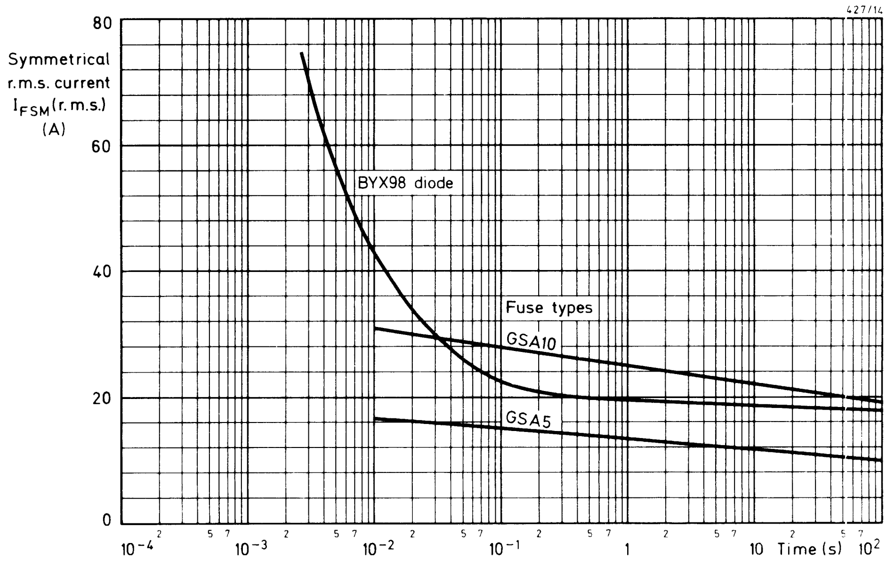


Fig.14 – Curves of surge current I_{FSM} (r.m.s.) against time for BYX98 diode protected by English Electric GSA5 and GSA10 fuses

MATCHING OF SEMICONDUCTOR DEVICES TO FUSE OPERATION

Some of the problems associated with matching semiconductor devices to fuses are considered in this section.

Overload conditions

In practical terms, the protection of diodes, thyristors, and triacs can take two principal forms:

1) Protection throughout an entire overload range up to full short-circuit conditions by means of a fuse alone;
2) Protection by means of a circuit breaker down to its minimum operating time, and for shorter periods, up to full short-circuit conditions by means of a suitable fuse.

In the second form of protection, the fuse is called upon to protect the circuit breaker and the semiconductor device. Hence the let-through current provided by the fuse should not exceed the maximum-rated interrupting capability of the circuit breaker (see Ref.12).

The fuse-only protection method is usually employed in low-power low-cost circuits. Surge current against time curves are shown in Figs.14 and 15 for semiconductor devices with fuse protection under short-circuit conditions. Fig.14 shows surge current I_{FSM} against time curves for the BYX98 diode (9A r.m.s. rating) protected by English Electric GSA5 and GSA10 fuses. Fig.15 shows surge current against time curves for the BTW24 thyristor (55A r.m.s. rating) protected by Brush 30ET, 40ET, and 55ET fuses. It will be seen from Fig.15 that the fuses have lower ratings than the device to give reasonable tracking in the overload region above one second. The problem of the low surge capability of devices to r.m.s. current in the 1s region can result in fuse-to-semiconductor-device coordination difficulties. Because of these difficulties, some restrictions may be placed on the maximum steady-state current operation of devices where fuse-only protection is used.

A more satisfactory system is to use the protection of the circuit breaker in the 1s region (see Fig.1). The circuit breaker provides 'constant current' interruption for this time region, and allows fuses of higher current rating to be used while adequate protection of the devices under short-circuit conditions is maintained.

High-current fault conditions

Semiconductor device protection in circuits where the fault current causing operation of the fuse is high enough to produce current-limiting action and complete fuse clearance in the subcycle region is now considered. As previously mentioned, the time-current curves for fuses usually terminate at 10ms, because for operating times less than 10ms the instant of fault occurrence has considerable influence on the melting time.

Conventional method of protection

Fuse clearance is usually specified solely in terms of energy let-through, or $\int i^2 dt$, rationalised to I^2t. Earlier papers (Refs.14 and 15) suggest that the forward current capability of rectifier diodes assumes a constant I^2t characteristic in the subcycle region (less than 10ms). The current-limiting fuse can be designed to have a constant I^2t let-through as a function of prospective current. The I^2t data given for fuses (see under 'Fuse curves') applies to worst-case conditions. Therefore, for most fault conditions, the I^2t let-through should be less

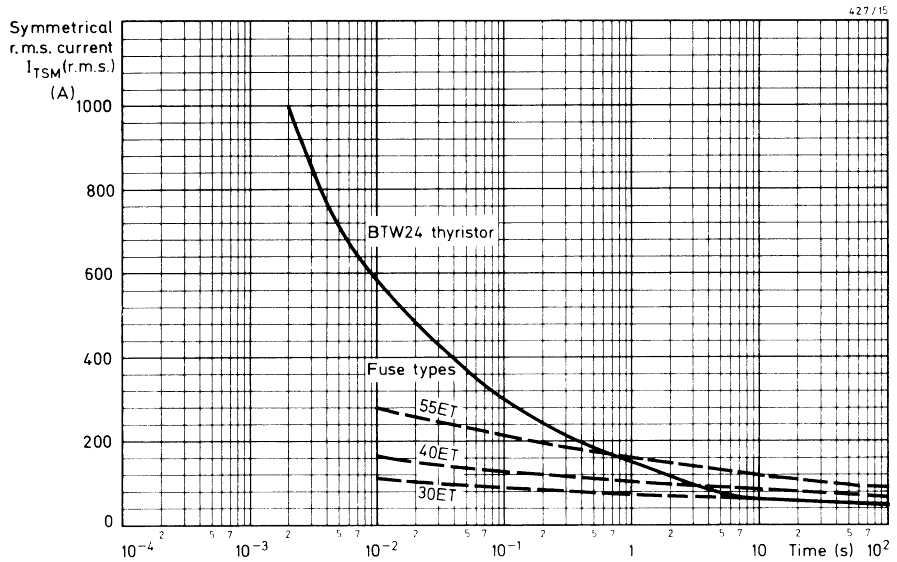


Fig.15 – Curves of surge current I_{TSM} (r.m.s.) against time for BTW24 thyristor protected by Brush 30ET, 40ET, and 55ET fuses

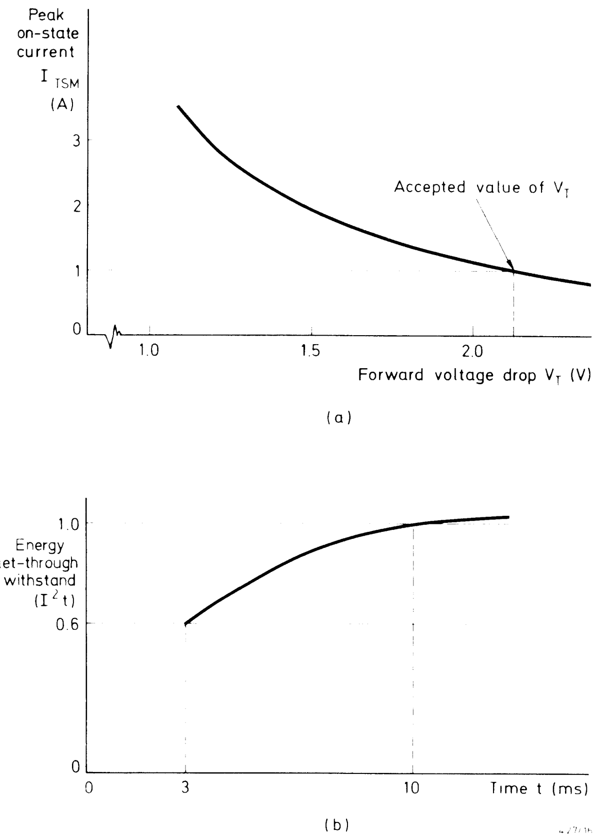


Fig.16 – Parameter limit values (indicated by broken lines) for diodes and thyristors:
(a) mean on-state current against forward voltage drop,
(b) I^2t let-through as a function of pulse width

than that shown in the published data. Conversely, the published I^2t value for the semiconductor diode, thyristor, or triac tends to be the lowest value in a complete spread of values. The probability of worst-case circuit conditions corresponding to a semiconductor device having a minimum I^2t capability is, therefore, statistically small. Based on this approach, which can be called the 'conventional' approach to fusing, a simple I^2t relationship between the fuse operating in subcycle time and the semiconductor device gives an effective method of protection in most applications.

Typical system for specifying I^2t capability of diodes, thyristors, and triacs

A typical system used by semiconductor device manufacturers for specifying the I^2t capability of a diode, thyristor, or triac enables the conventional method of protection described previously to be used with safety. The system is based largely on the method of matching the minimum I^2t capability of a device to the worst-case I^2t let-through for a nominally-rated fuse.

For any semiconductor device, it is desirable to absorb as much of the spread in parameters as possible into an acceptable marketable product. For example, V_T (d.c. forward voltage) of a thyristor is set against $I_{T(AV)}$ (the mean on-state current) to absorb the greater part of the V_T spread. Sample devices covering the full spread in V_T are subjected to a succession of 10ms half-sinewave surge-current pulses of increasing magnitude. An example of the results of these tests, in terms of I_{TSM} (thyristor non-repetitive peak on-state current) against V_T, is shown in Fig.16a in which a 'safe' contour line for pulses of 10ms period is indicated. The value of I_{TSM} for the accepted value of V_T is converted into an equivalent I^2t value for 10ms sinewave pulse width by the relationship:

$$I^2t\,(10\text{ms}) = \frac{I^2_{TSM} \times 10^{-2}}{2}. \quad \ldots(12)$$

A further test may be carried out, consisting of a 3ms pulse applied to the devices. From this test, a direct evaluation of I^2t withstand of the device can be computed from the shape of the waveform. The r.m.s. surge current capability for 3ms can be obtained from the graph of surge current against time (for example, Fig.15), and the I^2t value computed from the relationship:

$$I^2t\,(3\text{ms}) = I^2_{TSM(rms)} \times 3 \times 10^{-3}. \quad \ldots(13)$$

A comparison of the I^2t capabilities of various devices indicates that the I^2t value sometimes decreases for periods of less than 10ms for modern encapsulations, and that the thermal processes during these short periods are not of an adiabatic nature. A curve relating the I^2t capability of a device to pulse width is shown in Fig.16b. This curve shows a decreasing value of I^2t towards the 3ms pulse-width condition.

Close coordination of fuse parameters to semiconductor device surge capability

Close coordination of fuse performance to semiconductor device performance requires knowledge of the fuse performance under particular circuit conditions. It has been stated previously that curves in fuse published data are usually given for worst-case conditions. A considerable number of tests are undertaken to determine how fuse parameters vary with circuit conditions, and the variation in three principal fuse parameters is shown in Figs.8a, 8b, and 8c.

Fig.8a indicates that the fuse peak let-through (assuming the fuse to be in the current-limiting condition) has a waveform dependent on the supply voltage. When the fuse operates under maximum-rated voltage conditions, the waveform approaches a half-sinewave shape, whereas at a low voltage, a triangular-shaped waveform is produced. The r.m.s. current for a half-sinewave pulse $I_{rms}(hs)$ is given by:

$$I_{rms}(hs) = I_{S(pk)} / \sqrt{2}, \quad \ldots(14)$$

and the r.m.s. current for a triangular-shaped pulse $I_{rms}(tr)$ is given by:

$$I_{rms}(tr) = I_{T(pk)} / \sqrt{3}. \quad \ldots(15)$$

The equivalent I^2t values are given by:

$$I^2t(hs) = \frac{I^2_{S(pk)}t}{2}, \quad \ldots(16)$$

and

$$I^2t(tr) = \frac{I^2_{T(pk)}t}{3}. \quad \ldots(17)$$

If surge current applied over a definite time, resulting in excessive junction temperature and localised melting, is the primary cause of semiconductor failure, then an examination of the heating effects of different waveshapes with the same time base is desirable. Comparing the I^2t values for half-sinewave- and triangular-shaped pulses, the ratios of peak currents for pulses of an equal time base are given by:

$$I_{T(pk)} / I_{S(pk)} = \sqrt{(3/2)},$$

or

$$I_{T(pk)} = \sqrt{(3/2)}\, I_{S(pk)}. \quad \ldots(18)$$

Eq.18 suggests that the triangular waveform will produce a higher junction temperature than the sinewave for equal I^2t values. If this is correct, then I^2t ratings for a semiconductor device based on sinewave tests may have a lower safety margin than I^2t ratings based on triangular-shaped waveform tests when the fuse clears on a triangular-shaped waveform. It will be appreciated that because the let-through current waveshape of the fuse is dependent on supply conditions (that is, the supply voltage, instant of fault condition, and p.f.), it is difficult to produce rationalised curves which closely coordinate fuses to semiconductor devices unless supply conditions are known exactly.

EXAMPLES OF FUSE SELECTION FOR PROTECTION AGAINST HIGH FAULT CURRENTS IN A THYRISTOR

Fig.17 shows a pair of inverse-parallel-connected BTW92 thyristors CSR_1 and CSR_2 supplying phase-controlled power to a load. Assuming that the devices are operated near their full-load rating, fuse 1 and fuse 2 must be chosen to give short-circuit protection of the devices.

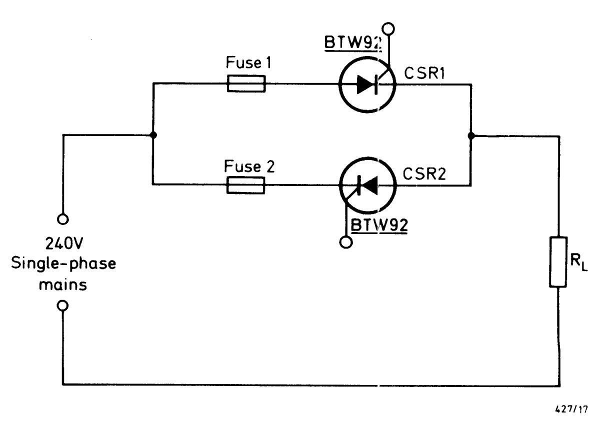


Fig.17 — Two inverse parallel connected BTW92 thyristors supplying phase-controlled power to a load

The ratings given below are from the published data for the BTW92 thyristor.

On-state conditions

Mean current $I_{T(AV)}$ = 20A

R.M.S. current $I_{T(RMS)}$ = 31A

I^2t rating (<10ms) $500A^2s$

Maximum surge current at peak of half-sinewave, and at maximum operating conditions I_{TSM} (10ms) = 320A

The I^2t value is derived directly from the I_{TSM} value by the relationship:

$$I^2t = \frac{I^2_{TSM} \times 10 \times 10^{-3}}{2}, \qquad \ldots(19)$$

or

$$I^2t = ½(320^2 \times 10 \times 10^{-3}),$$

$$= 512A^2s.$$

Included in the published data for the BTW92 is a graph showing the maximum r.m.s. surge current (A) against the duration of surge (s). The curve is based on sinewave pulses applied to the device. Given the value of I^2t at 10ms for the device, it is advisable to check the I^2t values at shorter periods to establish the law that this parameter follows.

From the published data:

$$I^2t \text{ for 5ms} = 315^2 \times 5 \times 10^{-3},$$

$$\simeq 500A^2s;$$

$$I^2t \text{ for 4ms} = 360^2 \times 4 \times 10^{-3},$$

$$\simeq 520A^2s.$$

These values show that the BTW92 has a substantially constant I^2t let-through below 10ms.

Protection by Ferraz 600V, type RE, 25A and 32A rated fuses

Examples of curves for Ferraz 600V type RE fuses are shown in Fig.7c for total I^2t as a function of prospective current, and in Fig.9 for total operating time as a function of the prospective current. The curves in Figs.7c and 9 are expressed in multiples of the rated current. Where the device is to be used at full-load current, fuses rated at 25A or 32A can be considered. By examining the curves shown in Fig.7c, it will be seen that the I^2t let-through decreases slightly at the higher values of prospective current. For a 600V type RE fuse of 25A nominal rating, the curves show that the maximum I^2t let-through is ($650A^2s \times 0{\cdot}5$) or $325A^2s$ for a 240V a.c. supply and for a prospective current of 500A r.m.s. From the Ferraz published data, the curves showing fuse clearance time as a function of prospective current and operating voltage (see Fig.9) indicate a clearance time of 5ms.

A comparison of the I^2t let-through and clearance time ratings of the 600V, type RE, 25A rated fuse and the I^2t withstand rating of the BTW92 thyristor shows that the device is adequately protected.

As a further verification of the protection of the device, the published data for the 600V type RE fuses shows that the peak let-through current of the 25A rated fuse is 500A for a prospective current of 500A r.m.s.

The 600V type RE fuse has a 600V r.m.s. rating, and the fusing current against time can be assumed to have a triangular waveform. The equivalent I^2t let-through for the fuse calculated from the peak current will be:

$$\frac{500^2 \times 5 \times 10^{-3}}{3} = 417A^2s. \qquad \ldots(20)$$

The maximum on-state peak surge current for the BTW92 is given in the published data as 320A for 10ms, and 447A for 5ms.

In the section 'Matching of semiconductor devices to fuse operation', it is shown (Eq.18) that for equal time base and I^2t values, the relationship between I_{pk} for a triangular wave to I_{pk} for a sinewave is $\sqrt{(3/2)}$. Therefore, a 320A peak sinewave pulse can be equated to $320\sqrt{(3/2)}$ or 392A for a peak triangular pulse.

The above verification indicates that the BTW92 is adequately protected by the 600V, type RE, 25A rated fuse at the value of prospective current chosen. Similarly, for higher values of prospective current for a fuse of the same type and rating, the calculations below are made for the BTW92.

1) Fuse I^2t let-through current at 2500A r.m.s. prospective current

$$= 590 \times 0{\cdot}5,$$

$$= 295A^2s.$$

2) Fuse clearing time = 1·5ms.

3) Thyristor non-repetitive peak current I_{TSM} for 1·5ms sinusoidal pulse (assuming a constant I^2t value for the device)

$$= \sqrt{\left[(2 \times 500)/(1{\cdot}5 \times 10^{-3})\right]},$$

$$= 816A.$$

4) Fuse peak current (I_{pk}) = 890A.

5) Fuse I^2t let-through calculated from peak current I_{pk} (assuming fusing current has a triangular waveform)

$$= \tfrac{1}{3}(890^2 \times 1{\cdot}5 \times 10^{-3}),$$

$$= 396\text{A}^2\text{s}.$$

6) Fuse peak current (calculated from peak sinusoidal current of device, assuming I^2t values for device and fuse are equal)

$$= 816\sqrt{(3/2)},$$

$$= 1000\text{A}.$$

Calculations 1 to 6 indicate an adequate safety margin for the thyristor protected by the fuse.

The performance of the 600V, type RE, 32A rated fuse is considered in a similar manner. The BTW92 is the device protected by the fuse.

1) Fuse I^2t let-through current at 500A r.m.s. prospective current

$$= 1000 \times 0{\cdot}5,$$

$$= 500\text{A}^2\text{s}.$$

2) Fuse clearing time = 6ms.
3) Thyristor non-repetitive peak current I_{TSM} for 6ms sinusoidal pulse (assuming a constant I^2t value for the device)

$$= \sqrt{[(2 \times 500)/(6 \times 10^{-3})]},$$

$$= 408\text{A}.$$

4) Fuse peak current (I_{pk}) = 580A.
5) Fuse I^2t let-through calculated from peak current I_{pk} (assuming fusing current has a triangular waveform)

$$= \tfrac{1}{3}(580^2 \times 6 \times 10^{-3}),$$

$$= 673\text{A}^2\text{s}.$$

6) Fuse peak current (calculated from peak sinusoidal current of device, assuming I^2t values of device and fuse are equal)

$$= 408\sqrt{(3/2)},$$

$$= 500\text{A}.$$

The calculations are repeated for the higher value of prospective current.

1) Fuse I^2t let-through current at 2500A r.m.s. prospective current

$$= 920 \times 0{\cdot}5,$$

$$= 460\text{A}^2\text{s}.$$

2) Fuse clearing time = 1·8ms.
3) Thyristor non-repetitive peak current I_{TSM} for 1·8ms sinusoidal pulse (assuming a constant I^2t value for the device)

$$= \sqrt{[(2 \times 500)/(1{\cdot}8 \times 10^{-3})]},$$

$$= 745\text{A}.$$

4) Fuse peak current (I_{pk}) = 1000A.
5) Fuse I^2t let-through calculated from peak current I_{pk} (assuming fusing current has a triangular waveform)

$$= \tfrac{1}{3}(1000^2 \times 1{\cdot}8 \times 10^{-3}),$$

$$= 600\text{A}^2\text{s}.$$

6) Fuse peak current (calculated from peak sinusoidal current of device, assuming I^2t values of device and fuse are equal)

$$= 745\sqrt{(3/2)},$$

$$= 912\text{A}.$$

The calculations indicate that the Ferraz 600V, type RE, 25A rated fuse will fully protect the BTW92 over a wide range of prospective supply current. The 600V, type RE, 32A rated fuse provides a narrower safety margin at low prospective currents.

Protection by English Electric type GSA25 25A rated fuse

Fig.18a shows the cut-off current characteristics, and Fig.18b shows the I^2t variation with prospective current, for English Electric type GSA fuses at 240V r.m.s. The I^2t let-through of the GSA25 fuse increases as a function of the prospective current of the supply. This increasing I^2t value sets a limit on the prospective current capability of the mains supply. No data is provided on the clearing time of the GSA25, although a reasonably accurate value can be calculated from the fuse published data available.

The parameters below apply to the GSA25 and the BTW92.

1) Thyristor I^2t rating = 500A^{2}s
2) For the 25A rated fuse to carry 500A^{2}s let-through, the prospective current is limited to 15kA r.m.s. or 21kA peak
3) Fuse peak current let-through (I_{pk}) (from fuse curves) = 1300A
4) Fuse pre-arc or melting I^2t let-through K = 80A^{2}s

The fuse clearing time is calculated below (see also under 'Fuse operation').

From Eq.11, fuse melting I^2t is given by:

$$K = \int_0^t i^2_m \, dt_m. \qquad \ldots(21)$$

The maximum rate of rise of current (di/dt) and peak

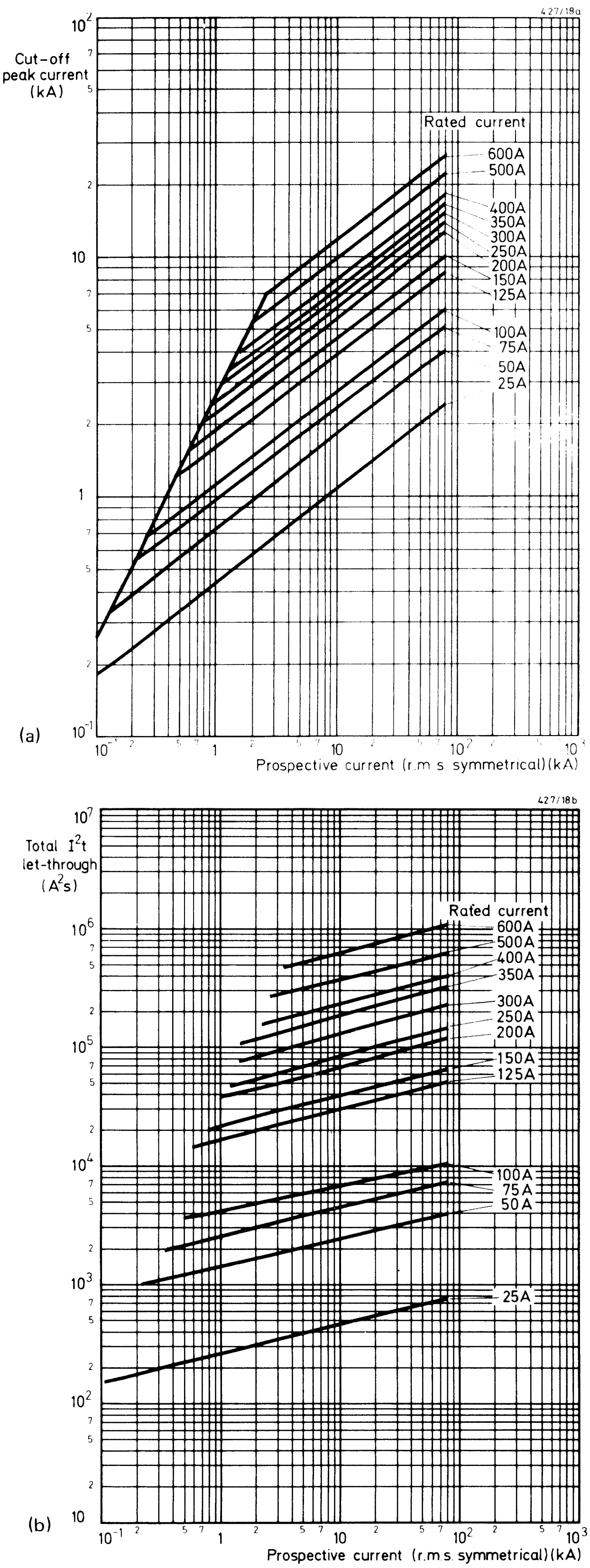


Fig.18 – English Electric fuses, type GSA, at 240V r.m.s.:
(a) cut-off current characteristics,
(b) I^2t variation with prospective current

melting current occur in a symmetrical fault period. Therefore:

$$di/dt = \omega I_{pk}(sym), \quad \ldots(22)$$

and

$$i_m = \omega I_{pk}(sym)\, t_m, \quad \ldots(23)$$

where i_m is the instantaneous current when the fuse element melts, and t_m is the melting time.

Eq.21 becomes:

$$K = \int_0^{t_m} \left(\omega^2 I_{pk}^2 (sym)\, t_m^2\right) dt_m,$$

$$= \tfrac{1}{3}\left(\omega^2 I_{pk}^2 (sym)\, t_m^3\right),$$

$$= \tfrac{1}{3}(di/dt)^2 t_m^3. \quad \ldots(24)$$

The current waveform in Fig.19 shows the clearing time for the GSA25, and the shaded area represents the I^2t melting value K. Therefore:

$$K = \frac{I^2{}_{pk(m)} t_m}{3}.$$

also:

$$K = \frac{(di/dt)^2 t_m^3 \times 10^{12}}{3},$$

or

$$3K = t_m^3 (di/dt)^2 \times 10^{12}, \quad \ldots(25)$$

where di/dt is expressed in A/µs.

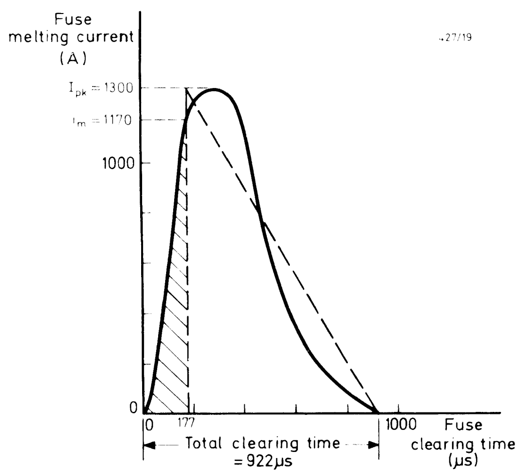


Fig.19 – Melting current against clearing time for English Electric type GSA25 fuse rated 25A. The shaded area represents the I^2t (melting) let-through K

From Eq.25, t_m is given by:

$$t_m = \left[\frac{3K \times 10^{-12}}{(di/dt)^2} \right]^{1/3} . \qquad \ldots (26)$$

From parameter 2 and Eq.22:

$$di/dt = 314 \times 21 \times 10^3 \times 10^{-6},$$

$$= 6{\cdot}6A/\mu s.$$

Therefore:

$$t_m = \left[\frac{3 \times 80 \times 10^{-12}}{6{\cdot}6^2} \right]^{1/3},$$

$$= 177\mu s;$$

and:

$$i_{m(pk)} = [3K\ di/dt]^{1/3},$$

$$= [3 \times 80 \times 6{\cdot}6 \times 10^6]^{1/3},$$

$$= 1170A.$$

The total I^2t let-through of the fuse (from parameter 2) is $500A^2s$; therefore the I^2t arcing let-through is $420A^2s$. Therefore arcing time t_{arc} is given by:

$$t_{arc} = \frac{3 \times 420}{1300^2},$$

$$= 745\mu s.$$

The total clearing time for the fuse is approximately 920μs as shown in Fig.19. For a sinewave pulse of time base 920μs, the peak current I_{pk} will be:

$$I_{pk} = \left[\frac{2 \times 500}{920 \times 10^{-6}} \right]^{1/2},$$

$$= 1042A.$$

The above calculations for the GSA25 show that a low-current fuse operated on a mains supply of high prospective current capability has a short clearing time. For many applications these calculations may be unnecessarily lengthy, particularly where the fuse to be used for short-circuit protection has an I^2t let-through that is substantially constant, or falls with increasing prospective current. Where such a fuse is used, the user may consider only the values given in the published data for the I^2t let-through of the protected device compared with the I^2t let-through for the fuse (see 'Conventional method of protection').

Some devices (for example, the BTX94 triac) have a reducing I^2t let-through capability for times less than 10μs (see Fig.16b). The Ferraz 600V, type RE, 25A rated fuse is better suited to these devices. However, the procedure for matching the fuse to the device is similar to that given in the calculations above for the English Electric GSA25 fuse and the BTW92 thyristor.

MATCHING FUSE ARC VOLTAGE TO DEVICE RATING

Generally, the higher the ratio of arc voltage to supply voltage, the quicker the fuse clears. The fuse arc voltage must not exceed the rated inverse voltage of the protected device. For example, in the circuit shown in Fig.17 a fuse arc voltage in excess of the rated inverse voltage of the non-conducting parallel-connected thyristor may result in breakdown of the device. Most fuse manufacturers give in their published data a graph of the relationship of arc voltage to supply voltage (see Refs.13, 16, and 17).

In practical fusing problems, additional conditions may need to be taken into account, for example, the environment in which the fuse and the semiconductor device are to operate, and the type of load on the system. A large amount of information on these conditions is given by the fuse manufacturer and the device manufacturer. However, the principal techniques embodied in the examples of fuse selection for the BTW92 given in the previous section will not be substantially altered by these conditions.

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APPENDIX 1

Triggering a Thyristor or Triac which has a Short-circuit Load

When a thyristor or triac is triggered under normal load conditions, a finite current-spreading time is required before full conduction at rated current can take place. This current-spreading time is usually given in the published data for the device as a permissible rate of rise of current (di/dt) in the device in terms of A/μs. When the source impedance is the impedance of an a.c. power line, Fig.3 shows that when θ is equal to 0° the initial rate of rise of current is zero, and the maximum rate of rise of current will occur when θ is equal to $\pi/2$. When θ is equal to $\pi/2$:

$$di/dt = E_{pk}/L,$$

which is similar to a d.c. condition.

As the p.f. of the source increases towards unity, the value of di/dt when θ is equal to 90° increases to the limiting condition $L \rightarrow 0$ and $di/dt \rightarrow \infty$. It will be seen that if a thyristor or triac is triggered into a short-circuit condition when supplied from a largely-resistive source of an a.c. or d.c. system, then a fuse cannot protect the device from the initial rate of rise of surge current. Therefore, the device will be damaged. In this article it has been shown that a.c. power sources are inductive under short-circuit conditions. With the typical inductance values associated with the a.c. system, the rate of rise of prospective current is usually moderate compared with the di/dt capability of the thyristor or triac.

MANUFACTURERS OF FUSES FOR SEMICONDUCTOR PROTECTION

Although three particular fuse manufacturers are mentioned in this article, it is recognised that comparable fuses are made by other manufacturers. The three manufacturers mentioned have been selected because their fuses are typical of most semiconductor protection fuses.

No preference is intended by inclusion in or omission from this present article.