Specifications

	Basic Specifications			
	Input channels:	4/8 analog (depends on model), and 16-bit logic		
	Input coupling settings:	AC 1 M Ω , DC 1 M Ω , GND, DC 50 Ω 1 M Ω + 1 0% 50 Ω + 1 0%		
	Voltage axis sensitivity setting	g range:		
	For 1 M Ω input: 2 mV/div to 10 V/div (steps of 1, 2, or 5)			
	For 50 Ω input: Maximum input voltage:	2 mV/div to 1 V/div (steps of 1, 2, or 5)		
	For 1 M Ω input (frequency of	f 1 kHz or less): 400 V (DC + ACpeak) (282 Vrms CAT II)		
	For 50 Ω input:	5 Vrms or less and 10 Vpeak or less		
	Frequency characteristics ¹ :	nive probe model 700089: aposified at probe tip)		
	For T Ms2 input. (using pas	10 V/div to 10 mV/div: DC to 400 MHz (500 MHz ⁴)		
		5 mV/div to 2 mV/div: DC to 300 MHz (400 MHz ⁴)		
	For 50 Ω input:	1 V/div to 10 mV/div: DC to 500 MHz		
	A/D conversion resolution:	8 bits (24 LSB/div)		
	Maximum sampling rate:	Real-time sampling mode:		
		Interleave mode on: 2 GS/s ²		
		Equivalent time sampling mode: 100 GS/s		
	Maximum record length:			
	701450/701470	Interleave mode on: 4 MW/channel ²		
	701460/701480	Interleave mode on: 16 MW/channel ²		
		Interleave mode off: 8 MW/channel		
	DC accuracy ¹ :	\pm (1.5% of 8 div + offset voltage accuracy)		
	Oliset voltage axis accuracy	2 mV/div to 50 mV/div ±(1% of setting ± 0.2 mV)		
		100 mV/div to 500 mV/div ±(1% of setting + 2 mV)		
	Time ouis actting ton so.	1 V/div to 10 V/div \pm (1% of setting + 20 mV)		
	Time axis setting range:	1 ns/div to 50 s/div (for record length of 10 kW of greater)		
	Time base accuracy1:	±0.005%		
	External clock input:	Input frequency range: 40 Hz to 20 MHz (continuous clock		
		signal only)		
	Trigger			
	Trigger modes:	Auto, Auto Level, Normal, Single, Single (N)		
	Trigger sources:	CH1 through CH8 (the number of channels depends on the		
		model; signals input to individual input terminals), LINE (connected utility power signal) EXT (signal input from EXT)		
		TRIG IN terminal)		
	Trigger types:	Edge, $A \rightarrow B$ (N), A Delay B, OR, Pattern, Pulse Width, TV,		
		Logic, I C (optional), CAN (optional), SPI (optional)		
	Display			
	Screen updating rate:	Maximum 60 times per second (for 10 kW all-points display)		
		Maximum 30 times per second (for 1 MW all-points display)		
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	or Ethernet port. Supported printer commands: ESC/P, ESC/P2, LIPS3,			
Floppy disk/Zip®/SCSI/Netwo	PCL5, BJ, PostScript (through Ethernet only) rk drive/PC card:			
Output formats: Postscript, HFF, BMP, JPEG, PNG				
Power Analysis Functions (optional)				
Correction of the difference in the electrical lengths of the probes (Deskew)				
Automated measurement of	voltage and current signals automatically or manually The correction range is ± 100 ns (0.01 ns resolution).			
	As with the standard measurement parameters (waveform parameters), performs automated measurement of power analysis parameters (see below).			
Valtage	Automated measurement on dual areas is also possible.			
vonage:	Amplitude UP-P, maximum value U+pk, minimum value U- pk, DC component Udc, rms value Urms, AC component Uac, rectified mean value calibrated to the rms value Umn,			
Current:	Amplitude IP-P, maximum value I+pk, minimum value I-pk, DC component Idc, rms value Irms, AC component Iac, rectified mean value calibrated to the rms value Imn, and rectified mean value (rm).			
Power:	Apparent power S. active power P. and reactive power Q			
Power factor:	Power factor I of the circuit under measurement			
Impedance:	Impedance Z of the circuit under measurement			
Watt hour:	Sum of positive and negative watt hours Wp, sum of positive watt hours Wp+, and sum of negative watt hours Wp-			
Ampere hour:	Sum of positive and negative ampere hours q, sum of positive ampere hours q+, and sum of negative ampere hours q-			
Heat energy: Statistical processing on the measured values:	Joule integral I ² t As with the standard measurement parameters, performs statistical processing on the measured values of power applysic parameters			
Waveform computation on	As with the standard waveform computation performs			
power analysis parameters:	waveform computation such as Instantaneous power,			
	impedance, Joule integral, power spectrum, and harmonics			
	comparison against the limits of IEC 6100-3-2 Edition 2.1, and EN61000-3-2 Amendment 14 is possible.			
Trend display:	Displays the trend of the change in the measured values of			
History search:	As with the standard measurement parameters performs			
	history search using power analysis parameters.			
GO/NO-GO determination:	As with the standard measurement parameters, performs GO/NO-GO determination using power analysis parameters.			
Saving of the computed results of harmonics:	Saves the computed result of harmonics to a file in CSV format			
² C bus analysis functions	(optional)			
Applicable Bus				
I ² C bus:	Bus transfer rate: Up to 3.4 Mbits/s			
SM bus	Address mode: 7 bits Conforms to the System Management Bus			
Trigger Function	Contorna to the Oyatem Management Edd.			
Trigger source:	CH1: SCL			
	CH2: SDA			
Start/Stop conditions for I ² C bus signal trigger:	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: •Ignore/Not ignore restart conditions •Ignore/Not ignore start/stop conditions that do not conform			
Start/Stop conditions for I ² C bus signal trigger: I ² C bus signal trigger • Address&Data	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: • Ignore/Not ignore restart conditions • Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the			
Start/Stop conditions for I ² C bus signal trigger: I ² C bus signal trigger • Address&Data: • Non-Ack:	CH3 to CH8(CH4): Analog signal input Select the start/stop conditions from the following: • Ignore/Not ignore restart conditions • Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates a trigger when an acknowledge is not present.			
Start/Stop conditions for I ² C bus signal trigger: ^{I2} C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: •Ignore/Not ignore restart conditions •Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates a trigger when an acknowledge is not present. trigger is activated on the combination (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition.			
Start/Stop conditions for I ² C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: •Ignore/Not ignore restart conditions •Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates a trigger when an acknowledge is not present. trigger is activated on the combination (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the address Activates a trigger on the true/false condition of the result of			
Start/Stop conditions for I ² C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: •Ignore/Not ignore restart conditions •Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates a trigger when an acknowledge is not present. trigger is activated on the combination (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the address Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address.			
Start/Stop conditions for I ² C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count • Data 2	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: • Ignore/Not ignore restart conditions • Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates a trigger when an acknowledge is not present. trigger is activated on the combination (AND logic) of the at and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger at the specified number of bytes after the start condition. The selectable range is 0 or 9999. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the safter the start condition. The selectable range is 0 or 9999.			
Start/Stop conditions for I ² C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count • Data 2 Combination trigger:	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: • Ignore/Not ignore estart/conditions from the following: • Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates a trigger when an acknowledge is not present. trigger is activated on the combination (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the address Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data that is present after the byte count passes. Possible to activate triggers by combining the CH3 to CH8(CH4 ⁹) analog signals and the I ² C bus signal (CH1 and			
Start/Stop conditions for I ² C bus signal trigger Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count • Data 2 Combination trigger: • I ² C on Pattern	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: • Ignore/Not ignore estart/conditions from the following: • Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates at trigger when an acknowledge is not present. trigger is activated on the combination (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data that is present after the byte count passes. Possible to activate triggers by combining the CH3 to CH8(CH4 ³) analog signals and the I ² C bus signal (CH1 and CH2). Activates a trigger when the trigger conditions of the I ² C bus are met on the true of false condition of the CH3 to			
Start/Stop conditions for I ² C bus signal trigger: ^{I2} C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count • Data 2 Combination trigger: • I ² C on Pattern • I ² C -> Pattern	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: • Ignore/Not ignore estart/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates at trigger on the combination (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the address Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data that is present after the byte count passes. Possible to activate triggers by combining the CH3 to CH8(CH4 ³) analog signals and the I ² C bus signal (CH1 and CH2). Activates a trigger when the trigger condition of the I ² C bus are met on the true of false condition of the I ² C bus are met on the true of talse condition of the CH3 to CH8(CH4 ³) parallel pattern. Activates a trigger when the pattern trigger condition is met after the tigger condition of the I2C bus signal is met.			
Start/Stop conditions for I ² C bus signal trigger: ^{I2} C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count • Data 2 Combination trigger: • I ² C on Pattern • I ² C -> Pattern Analysis Function Signal input: Number of data points that c	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: • Ignore/Not ignore estart/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates at trigger on the anaknowledge is not present. trigger is activated on the combination (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the address Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data that is present after the byte count passes. Possible to activate triggers by combining the CH3 to CH8(CH4 ³) analog signals and the I ² C bus signal (CH1 and CH2). Activates a trigger when the trigger condition of the H ² C bus are met on the true of false condition of the H ² C bus are net on the true of the condition of the CH3 to CH8(CH4 ³) parallel pattern. Activates a trigger when the pattern trigger condition is met after the trigger condition of the I2C bus signal is met. Select CH1 (SCL), CH2 (SDA) or CH3 (SCL), CH4 (SDA). an be analyzed			
Start/Stop conditions for I ² C bus signal trigger: ^{I2} C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count • Data 2 Combination trigger: • I ² C on Pattern • I ² C on Pattern Analysis Function Signal input: Number of data points that c Display of the analysis result	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: •Ignore/Not ignore estart/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates at trigger on the anaknowledge is not present. trigger is activated on the combination (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the address Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data that is present after the byte count passes. Possible to activate triggers by combining the CH3 to CH8(CH4 ³) analog signals and the I ² C bus signal (CH1 and CH2). Activates a trigger when the trigger condition of the I ² C bus are met on the true of false condition of the I ² C bus are met on the true of the cound to the CH3 to CH8(CH4 ³) parallel pattern. Activates a trigger when the pattern trigger condition is met after the trigger condition of the I ² C bus signal is met. Select CH1 (SCL), CH2 (SDA) or CH3 (SCL), CH4 (SDA). an be analyzed Up to 40,000 bytes S			
Start/Stop conditions for I ² C bus signal trigger: ^{I2} C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count • Data 2 Combination trigger: • I ² C on Pattern • I ² C on Pattern Analysis Function Signal input: Number of data points that c Display of the analysis result • Waveform and the list of	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: •Ignore/Not ignore estart/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates at trigger on the comparison (ADD logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the address Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address. Activates a trigger on the true/false condition of the result of the comparison with the data that is present after the byte count passes. Possible to activate triggers by combining the CH3 to CH8(CH4 ³) analog signals and the I ² C bus signal (CH1 and CH2). Activates a trigger when the trigger condition of the CH3 to CH8(CH4 ³) parallel pattern. Activates a trigger when the pattern trigger condition is met after the trigger condition of the I ² C bus signal is met. Select CH1 (SCL), CH2 (SDA) or CH3 (SCL), CH4 (SDA). an be analyzed Up to 40,000 bytes S Displays the analysis results using the following two methods. analysis results Simultaneously displays the waveform and the list of analysis results			
Start/Stop conditions for I ² C bus signal trigger • Address&Data: • Non-Ack: For Address&Data trigger, a five items below. Address, D • Start Condition • Address • Data 1 • Byte Count • Data 2 Combination trigger: • I ² C on Pattern • I ² C on Pattern • I ² C -> Pattern Analysis Function Signal input: Yumber of data points that c Display of the analysis result	CH3 to CH8(CH4 ³): Analog signal input Select the start/stop conditions from the following: • Ignore/Not ignore start/stop conditions that do not conform to the protocol Select from the following two trigger types. Activates the trigger based on the comparison of the specified address and data Activates at trigger on the achonization (AND logic) of the ata 1 and Data 2 can be enabled or disabled. Activates a trigger on the start condition. Activates a trigger on the start condition. Activates a trigger on the true/false condition of the result of the comparison with the address Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address Activates a trigger on the true/false condition of the result of the comparison with the data immediately after the address Activates a trigger on the true/false condition of the result of the comparison with the data that is present after the byte count passes. Possible to activate triggers by combining the CH3 to CH8(CH4 ³) analog signals and the I ² C bus signal (CH1 and CH2). Activates a trigger on the true of false condition of the CH3 to CH8(CH4 ³) parallel pattern. Activates a trigger when the pattern trigger condition is met after the trigger condition of the I ² C bus signal is met. Select CH1 (SCL), CH2 (SDA) or CH3 (SCL), CH4 (SDA). an be analyzed Up to 40,000 bytes S Displays the analysis results using the following two methods. analysis results			

 Search Function Data search: 	The following two types of search are possible.
Pattern search (Byte P	attern)
Indefinite data search (condition and search the waveform. (Indefinite State)
 Analysis Result Save Func 	tion
Data storage of the list of detailed analysis results:	Saves the list of detailed analysis results to a file in ASCII format.
CAN Bus Signal Analysis	Function (optional)
Supported CAN Bus	CAN Version 2.0B
Bit rate:	Set any of the following bit rates: 1 M, 500 k, 250 k, 125 k, 100 k, 95.238 k, 83.333 k, 62.5k, 50 k, 33.333 k, 20k, 10k [bps] or an arbitrary bit rate between 1 M to 10 k [bps] (Th resolution is the bit time (reciprocal of the bit rate of 0.5 us Supports High speed CAN(ISO11898) and Low speed CAN(ISO11519-2)
 Trigger Function 	
Trigger source:	CH1: CAN bus signal (Input CAN_H and CAN_L signals via differential probes.) CH2 to CH8(CH4 ³): Analog signal input
• Start of Frame	Activates a trigger on the combination (AND logic) of the five items below. Activates a trigger on the Start of Frame (SOF).
Identifier	Activates a trigger on the Identifier that matches the specified conditions.
Data Field	Activates a trigger at the data field that matches the specified conditions (up to 8 bytes can be specified).
• Error Frame Combination trigger:	Activates a trigger on an error frame. Possible to activate triggers by combining the CH2 to CH8(CH4 ³) analog signals and the CAN bus signal (CH1).
CAN on Pattern	Activates a trigger when the CAN trigger conditions are me on the true or false condition of the CH2 to CH8(CH4 ³) parallel pattern.
CAN -> Pattern	Activates a trigger when the pattern trigger condition is me after the trigger condition of the CAN bus signal is met.
Analysis Function	
Number of frames that can	be analyzed:
Frames that are analyzed.	Up to 16,000 frames
Display of the analysis rest	ults:
	waveform and the list of analysis results Simultaneously displays the waveform and the list of
	analysis results. •List of detailed analysis results Displays No., Time, ID, Data, CRC, ACK and Info. (error
Stuff bit computation	Extracts stuff bits from the CAN Bus waveform and display them as a Math waveform (Math1).
Search Function:	
Data search	The following two types of search are possible. •Pattern search (Frame Pattern) Search the waveform by specifying a field or frame pattern and find data possible (and find state)
Field jump	Indefinite data search (indefinite State) Indefinite data can be searched. Moves the zoom position (Z1 Pos) to the beginning of a certain field within the current frame.
Analysis Result Save Func	tion
Data storage of the list of detailed analysis results:	Saves the list of detailed analysis results to a file in ASCII format.
SPI Bus Signal Analysis	Function (optional)
Trigger Function Trigger source:	CH1: SCK
าามูมุฮะ จบนเบฮ.	CH2: MOSI CH3: MISO CH4: SS
SPI bus signal trigger:	CH5 to CH8: Analog signal input (only for the DL7480) Activates a trigger on the combination (AND logic) of the following four items. A Pattern and B Pattern can be enabled or disabled
Assertion of SS A Pattern	Activates a trigger on the assertion of SS. Activates a trigger on true/false condition of the result of the
	comparison with the MOSI data immediately after the assertion of SS. The length of data that is compared can be set to 1 or 8 bytes.
Byte Count	Activates a trigger the specified bytes after the assertion o SS (after the A pattern if A Pattern is enabled). The splottable range 0 or 1 000
B Pattern	Activates a trigger on the true/false condition of the result Activates a trigger on the true/false condition of the result the comparison with the data that is present after the byte count passes. The data to be compared is selectable between MOSI and MISO. The data length can be set to 1 to 8 bytes.
Combination trigger: (available DL7480 only) • SPI on Pattern	Possible to activate triggers by combining CH5 to CH8 analog signals and the SPI bus signal (CH1 to CH4). Activates a trigger when the trigger conditions of the SPI bus signal are met on the true or false condition of the CH3
SPI -> Pattern	to CH8 parallel pattern. Activates a trigger when the pattern trigger condition is me

Activates a trigger when the pattern trigger condition is met after the trigger condition of the SPI bus signal is met.

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 Analysis Function Signal input: 	CH1: Clock signal (SCK) CH2: Data 1 (MOSI) CH3: Data 2 (MISO) CH4 to CH80 or logic input: CS cianal (SS)		
Number of data points that o	an be analyzed:		
Analysis Result Display:	Up to 80,000 bytes Displays the analysis results using the following two methods. • Waveform and the list of analysis results Simultaneously displays the waveform and the list of analysis results.		
	• List of detailed analysis results Displays No., Time, Dt1, Dt2, CS.		
Search Function			
Data search:	The following two types of search are possible. • Pattern search (Frame Pattern) Search the waveform by specifying a data pattern. • Indefinite data search (Indefinite State) Indefinite data can be searched.		
 Analysis Result Save Function Data storage of the list of detailed analysis results: 	on Saves the list of detailed analysis results to a file in ASCII format .		
Rear Panel I/O			
Interfaces:	GP-IB, USB-PC connector, USB peripheral connector, Ethernet (100BASE-TX, 10BASE-T; optional), SCSI (optional)		
Signal I/O:	One for external trigger input/external clock input/trigger gate input, one trigger output, one RGB video signal output (VGA)		
Logic input:	Measured with 701981 logic probe (8 bits).		
Logic probe (sold separately			

Logic probe (Solu Separatory) Number of inputs: 8 Maximum foggle frequency: 250 MHz (701981), 100 MHz (701980) Input voltage range: ±10 V (DC + AC peak, 701981), ±40 V (DC + AC peak, 701980) Cutbut connectors: 4 (an additional 4 are available as ar Output connectors: 4 (an additional 4 are available as an option with 701470 and 701480) ±12 V Probe power connectors: Output voltage: General Specifications Rated supply voltage: 100-120 VAC/220-240 VAC (switches automatically)

Rated supply frequency:	50/60 Hz
Maximum power consumption:	320 VA
External dimensions:	373 mm (W) \times 210.5 mm (H) \times 355.3 mm (D) (when the printer cover is closed; does not include knobs and protrusions)
Weight:	Approximately 10 kg (24.2 lbs, including printer; does not include logic inputs)



Measurements are obtained following calibration with the internal clock as the time base after the warmup period under the reference operating conditions (see below). Reference operating conditions
 Ambient temperature: 23 ± 2°C
 Ambient temperature: 23 ± 10% RH
 Supply voltage/frequency tolerance: Within 1% of rating

 When interleave mode is on, the number of available channels is half the installed number of channels.
 CH4 on the DL7440, CH8 on the DL7480
 When using Miniature passive probe model 701941; specified at probe tip.

Model and Suffix Codes

Model	Suffix Code	Description
701450		DL7440 digital oscilloscope with 4 CH input and maximum 4 MW memory
701460		DL7440 digital oscilloscope with 4 CH input and maximum 16 MW memory
701470		DL7480 digital oscilloscope with 8 CH input and maximum 4 MW memory
701480		DL7480 digital oscilloscope with 8 CH input and maximum 16 MW memory
	-D	UL and CSA standard
Power cable	-F	VDE standard
	-Q	BS standard
	-R	AS standard
	-н	GB standard
Internal	-J1	Floppy disk drive ¹
storage drive) -J2	Zip [®] drive ¹
	/B5	built-in printer
	/E4	Four additional passive probes(701470, 701480 only) ²
	/EX4	Attach four 701941 probes ^{7,9}
	/EA4	Four additional 701941 probes ^{8,9}
	/P4	Four additional probe power connectors(701470, 701480 only) ³
	/N3	Logic input for 701450/701470 ⁴
Ontions	/N4	Logic input for 701460/701480 ⁴
optione	/C7	SCSI interface
	/C10	Ethernet interface
	/G2	User-defined math function ⁵
	/G4	Power Supply Analysis Function ⁵
	/F5	I ² C + SPI Bus Analyzer ⁶
	/F7	CAN + SPI Bus Analyzer ⁶
	/F8	I ² C + CAN + SIP Bus Analyzer ⁶

1: Select one only.

2: The DL7400 Series is standard-equipped with four passive probes (700988).

 The DL7400 Series is standard-equipped with four probe power connectors.
 Select /N3 for models 701450 and 701470, and /N4 for models 701460 and 701480. Logic probes are sold separately. Purchase logic probe model 701981 (shown below under Water and Water W "Accessories (Optional)").

5: (G2 and (G4 cannot be specified together. 6: Option /F5, /F7, and /F8 cannot be specified together. Select one only. The SPI Bus Analysis and Search functions are Standard feature. The SPI Bus Triggers are available only as an option.

5: Four 700988 probes are not included when this option is specified.
8: This option can be specified with model 701470, 701480 only.
9: When the option /E4 is specified, neither /EX4 nor /EA4 can be specified together.

Related Products

Standard Accessories

Name	Q'ty
Power cable	1
Passive probes (700988)	4
Printer roll paper (when option /B5 is specified)	1
User's manual (one set)	1
Front cover (transparent)	1
Soft carrying case (for probes, etc.)	1

Accessories (Optional)

Name	Model	Specifications
Passive probe	700988	10 M Ω (10:1), 400 MHz, 1.5 meters (one per unit)
FET probe	700939	900 MHz band
Logic probe (for DL7400)	701980	1 MΩ/10pF, 100 MHz toggle frequency
Logic probe (for DL7400)	701981	10 kΩ/9pF, 250 MHz toggle frequency
100:1 probe	700978	100 MHz band
Differential probe	700925	DC to 15 MHz band
Differential probe	700924	DC to 100 MHz band
Differential probe	701920	DC to 500 MHz band
Differential probe	701921	DC to 100 MHz band
Differential probe	701922	DC to 200 MHz band
Current probe	701933	DC to 50 MHz band, 30 Arms
Current probe	701930	DC to 10 MHz band, 150 Arms
Current probe	701931	DC to 2 MHz band, 500 Arms
Deskew Signal Source	701935	For /G4 option
Miniature passive probe	701941	DC-500MHz band
Rack mount kit	701965	for EIA rack

Note: See the Bulletin 7009-63E(DL series accessories) for details.

Supplies

Name	Part number	Description	Order Q'ty
Printer roll paper	B9850NX	30 meter roll (1 roll per package)	5
Passive probe	700988	10 MΩ (10:1), 400 MHz band,1.5 m (1 probe per package)	1
Front panel protective cover	B8051DP	A transparent cover	1



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NOTICE

• Before operating the product, read the user's manual thoroughly for proper and safe operation.

 If this product is for use with a system requiring safeguards that directly involve personnel safety, please contact the Yokogawa sales offices.

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- Yokogawa's electrical products are developed and produced in facilities that have received ISO14001 approval.
- In order to protect the global environment, Yokogawa's electrical products are designed in accordance with Yokogawa's
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