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Serial ATA Interface

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Why do we need a new interface?

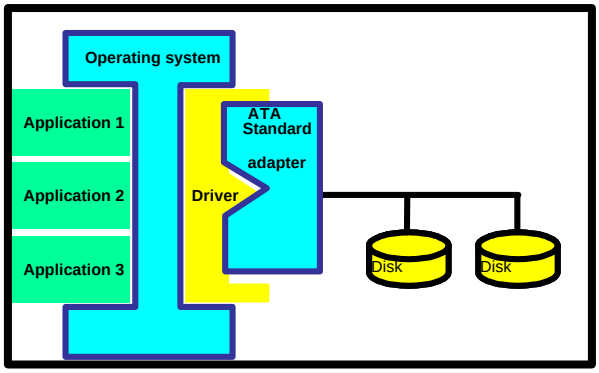
Limitations of parallel ATA

Serial ATA was designed to overcome a number of limitations of parallel ATA. The most significant limitation of parallel ATA is the difficulty in increasing the data rate beyond 100MB/s. Parallel ATA uses a single-ended signaling system that is prone to induced noise. Increasing the parallel data rate beyond 100 MB/s would require a new signaling system that would not be backward compatible with existing systems. Desktop HDDs can be expected to outrun the 100 Mbytes/sec data rate in the next few years so a new system is needed.

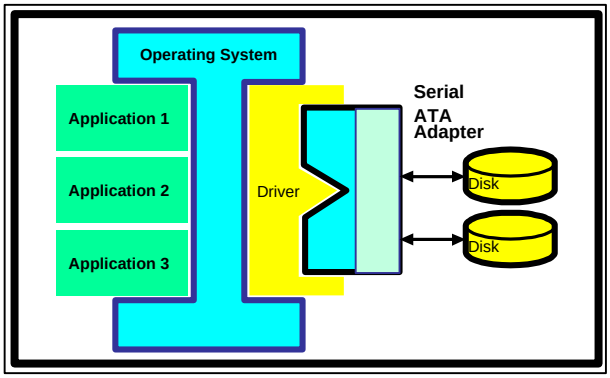
An additional limitation is that parallel ATA uses 5V signaling levels and upcoming silicon microelectronic processes are not compatible with 5V signaling.

Serial ATA overcomes these issues by moving to 250mV differential signaling method. Differential signaling rejects induced noise. The 250mV differential signal level is compatible with future microelectronic fabrication processes.

Parallel ATA Topology



Serial ATA Topology



Forecasts Indicate ATA Dominance

ATA is the dominant HDD interface in the industry. The ATA interface market is expected to be approximately 190 million units in 2003, accounting for about 90% of all HDDs shipped, according to International Data Corporations (IDC) 2002/03 forecasts. By 2006, IDC projects ATA unit shipments will increase to beyond 310 million and continue to account for 90% of all HDDs shipments. It is clear that the market will demand ATA-class HDDs for the foreseeable future.

Industry Supporters

Serial ATA v1.0 specification was developed by Serial ATA Working Group, and this published specification is in the process of being adopted by ANSI T13 public committee into its ATA/ATAPI 7 specification. At the same time, Serial ATA II Working Group is developing extensions to the v1.0 specification, as to allow Serial ATA HDDs be used in the entry level server and storage system applications. The interface specification will double to 300 Mbytes/s in Serial ATA II.

Serial ATA Features and Specifications

The Basics

Serial ATA is designed to be transparent to the host system software layer which allows existing operating systems, device drivers and applications to run without modification. The interface is a 4-wire, point-to-point configuration — supporting one device per controller connection. Thus, there are no master/slave configuration jumper issues as there are with parallel ATA drives. The interface provides a substantial pin count reduction from parallel ATA. The smaller cable helps air flow and improves cable routing.

Layering Model

The Serial ATA function is divided into 4 layers, as shown in Table 1. The Transport and Link layers control overall operation. The Application layer is designed to appear identical to parallel ATA, thereby maintaining software compatibility. The Physical layer handles the high speed serial communication between host and device. Serial ATA can transport all ATA and ATAPI protocols, and is designed to be forward compatible with future ATA standards. In addition, it provides opportunities to improve upon ATA with future features such an improved native queuing.

Table 1. Serial ATA communications layer model.

4	Application
3	Transport
2	Link
1	Physical

Physical Layer

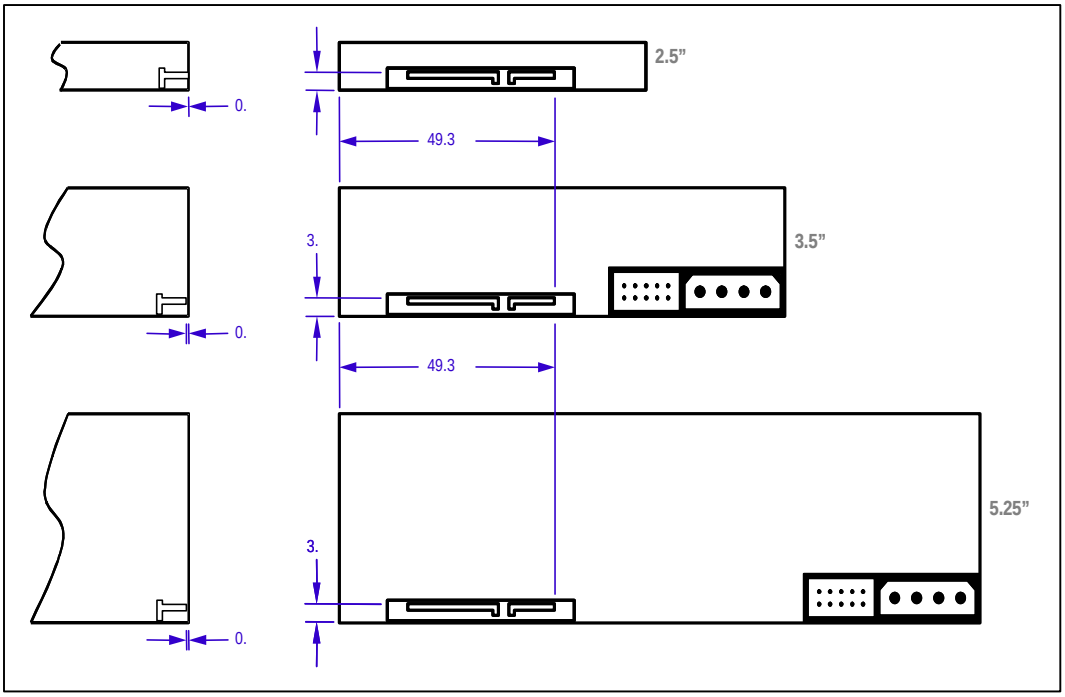
The Serial ATA physical layer (PHY) uses low-voltage (250mV) differential signaling to enable speeds of 1.5Gb/s and beyond. The roadmap is designed to carry the interface for 10 years, through 6Gb/s. There are 2 differential pairs, one for transmit and one for receive. The PHY layer incorporates serializer/deserializer, provides out of band (OOB) signaling, and handles power–on sequencing and speed negotiation. Transmit Data is serialized from 10-bit characters, and Receive Data is deserialized to 10-bit characters. Device status feedback is provided to the to the link layer.

Parallel ATA uses single-ended signaling, and requires 5V tolerant silicon.

The interface supports both cabled (up to 1 meter) and back-plane connections. The connectors are designed to blind mate, and staggered contacts are provided to facilitate hot plugging. There are three power supply voltages: 12V, 5V and 3.3V. The first generation cables and connectors are designed to support the future 3.0Gb/s speed. The connector location and interface is common for 5.25, 3.5 and 2.5 inch devices, facilitating the ability to support multiple form factors within a single bay.

Parallel ATA has an 18" cable length limit.

Common Connector Location



Link Layer

The link layer is responsible for sending and receiving frames, control signal primitives and for performing flow control. The link layer has a primitive character encoder/decoder, 8B/10B encoder/decoder, 32-bit CRC calculator, data scrambler/descrambler and a layer controller.

Transport Layer

The transport layer handles the packing and unpacking of ATA and ATAPI information into Frame Information Structures. The transport layer also manages the FIFO or buffer memory for controlling data flow.

Application Layer

The application layer interacts with the Transport layer through a register interface that is equivalent to that presented by a traditional parallel ATA host adapter. A shadow register block is defined that is both compatible with parallel ATA and anticipated future extensions. Thus, the software is backward compatible with parallel ATA devices.

Serial ATA Opportunities

The opportunity for serial ATA includes all ATA attached devices (not just HDDs), and potentially the displacement of other interfaces. The key to rapid adoption is widespread industry support. The introduction of Serial ATA support in Intel chipsets is the most significant step toward the industry adoption of Serial ATA HDDs.
At the initial stage, Serial ATA HDDs will be best suited for the high-end desktop PC market. Ultimately Serial ATA should capture the entire parallel ATA market. This will require costs dropping enough to replace parallel ATA in non-HDD applications, such as DVD drives that don't require the interface performance.
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In addition, Serial ATA HDDs could encroach on markets currently occupied by parallel SCSI. For example, the single user low-end workstation market may find Serial ATA very attractive. Parallel ATA is already entering this market, although Gartner estimates the market share in 2001 was just under 5%. This market includes low-end workstation, server and NAS.

The Serial ATA interface is an important technology upgrade to the parallel ATA interface. Serial ATA advantages include the following:

- Point to point connection, eliminating Master/Slave configurations
- Thinner and longer cables
- No new software driver is necessary for Serial ATA HDDs
- Low differential voltage for signals
- Interface bandwidth starting with 150 Mbytes/sec, then 300 Mbytes/sec and 600 Mbytes/sec; a robust migration path for the future
- Better connector design, for hot-plug, blind mate applications
- 32 bits CRC error checking on all data and control information

References and Specifications

? For more information and all latest released specifications, please go to Serial ATA Working Group web site: www.serialata.org

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