

# NI 6040E Family Specifications

This document lists the I/O terminal summary and specifications for the devices that make up the NI 6040E family of devices. This family includes the following devices:

- NI PCI-MIO-16E-4 (NI 6040E)
- NI PXI-6040E

## I/O Terminal Summary



**Note** With NI-DAQmx, National Instruments revised its terminal names so they are easier to understand and more consistent among NI hardware and software products. The revised terminal names used in this document are usually similar to the names they replace. For a complete list of Traditional NI-DAQ (Legacy) terminal names and their NI-DAQmx equivalents, refer to *Terminal Name Equivalents* of the *E Series Help*.

**Table 1.** I/O Terminals

Terminal Name	Terminal Type and Direction	Impedance Input/Output	Protection (V) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
AI <0..15>	AI	100 G $\Omega$ in parallel with 100 pF	25/15	—	—	—	$\pm 200$ pA
AI SENSE	AI	100 G $\Omega$ in parallel with 100 pF	25/15	—	—	—	$\pm 200$ pA
AI GND	—	—	—	—	—	—	—
AO 0	AO	0.1 $\Omega$	Short-circuit to ground	5 at 10	5 at -10	20 V/ $\mu$ s	—
AO 1	AO	0.1 $\Omega$	Short-circuit to ground	5 at 10	5 at -10	20 V/ $\mu$ s	—
AO EXT REF	AI	10 k $\Omega$	25/15	—	—	—	—
AO GND	—	—	—	—	—	—	—
D GND	—	—	—	—	—	—	—
+5 V	—	0.1 $\Omega$	Short-circuit to ground	1 A	—	—	—
P0.<0..7>	DIO	—	V <sub>CC</sub> + 0.5	13 at (V <sub>CC</sub> - 0.4)	24 at 0.4	1.1	50 k $\Omega$ pu

**Table 1.** I/O Terminals (Continued)

Terminal Name	Terminal Type and Direction	Impedance Input/Output	Protection (V) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
AI HOLD COMP	DO	—	—	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
EXT STROBE*	DO	—	—	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 0/ (AI START TRIG)	AI/DIO	10 kΩ	V <sub>CC</sub> + 0.5/±35	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	9 kΩ pu, 10 kΩ pd
PFI 1/ (AI REF TRIG)	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 2/ (AI CONV CLK)*	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 3/ CTR 1 SOURCE	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 4/CTR 1 GATE	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
CTR 1 OUT	DO	—	—	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 5/ (AO SAMP CLK)*	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 6/ (AO START TRIG)	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 7/ (AI SAMP CLK)	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 8/ CTR 0 SOURCE	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI 9/CTR 0 GATE	DIO	—	V <sub>CC</sub> + 0.5	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
CTR 0 OUT	DO	—	—	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ OUT	DO	—	—	3.5 at (V <sub>CC</sub> - 0.4)	5 at 0.4	1.5	50 kΩ pu

\* Indicates active low.

AI = Analog Input      DIO = Digital Input/Output      pd = pull-down  
 AO = Analog Output      DO = Digital Output      pu = pull-up  
 AI/DIO = Analog Input/Digital Input/Output

**Note:** The tolerance on the 50 kΩ pull-up and pull-down resistors is large. Actual value might range between 17 kΩ and 100 kΩ.

# Specifications

The following specifications are typical at 25 °C unless otherwise noted.

## Analog Input

### Input Characteristics

Number of channels ..... 16 single-ended  
or 8 differential  
(software-selectable  
per channel)

Type of A/D converter (ADC) ..... Successive  
approximation

Resolution ..... 12 bits, 1 in 4,096

Maximum sampling rate  
Single-channel scanning ..... 500 kS/s  
Multiple-channel scanning ..... 250 kS/s

Input signal ranges

Range (Software-Selectable)	Input Range	
	Bipolar	Unipolar
20 V	±10 V	—
10 V	±5 V	0 to 10 V
5 V	±2.5 V	0 to 5 V
2 V	±1 V	0 to 2 V
1 V	±500 mV	0 to 1 V
500 mV	±250 mV	0 to 500 mV
200 mV	±100 mV	0 to 200 mV
100 mV	±50 mV	0 to 100 mV

Input coupling ..... DC

Maximum working voltage  
(signal and common-mode) ..... Each input should remain  
within ±11 V of ground

Overvoltage protection

Powered on ..... ±25 V

Powered off ..... ±15 V

Inputs protected ..... AI <0..15>, AI SENSE

FIFO buffer size ..... 512 samples (S)

DMA

Channels ..... 3

Data sources/destinations ..... Analog input,  
analog output,  
counter/timer 0,  
or counter/timer 1

Data transfers ..... Direct memory access  
(DMA), interrupts,  
programmed I/O

DMA modes ..... Scatter-gather  
(single-transfer,  
demand-transfer)

Configuration memory size ..... 512 words  
(1 word = 8 bits)

## Accuracy Information

Nominal Range (V)	Absolute Accuracy										Relative Accuracy Resolution (mV)	
	% of Reading		Offset (mV)	Noise + Quantization (mV)		Temp Drift (%/°C)	Absolute Accuracy at Full Scale (mV)	Single Pt.		Averaged		
	24 Hours	1 Year		Single Pt.	Averaged			Single Pt.	Averaged			
±10	0.0672	0.0714	7.38	4.64	0.846	0.0010	15.373	6.27	1.11			
±5	0.0272	0.0314	3.70	2.32	0.423	0.0005	5.697	3.14	0.557			
±2.5	0.0672	0.0714	1.86	1.16	0.211	0.0010	3.859	1.57	0.278			
±1	0.0672	0.0714	0.757	0.464	0.085	0.0010	1.556	0.627	0.111			
±0.5	0.0672	0.0714	0.389	0.269	0.042	0.0010	0.789	0.339	0.056			
±0.25	0.0672	0.0714	0.205	0.134	0.021	0.0010	0.405	0.169	0.028			
±0.1	0.0672	0.0714	0.095	0.076	0.010	0.0010	0.176	0.088	0.013			
±0.05	0.0672	0.0714	0.058	0.056	0.006	0.0010	0.100	0.064	0.008			
0 to 10	0.0272	0.0314	3.70	2.32	0.423	0.0005	7.269	3.14	0.557			
0 to 5	0.0672	0.0714	1.86	1.16	0.211	0.0010	5.645	1.57	0.278			
0 to 2	0.0672	0.0714	0.757	0.464	0.085	0.0010	2.271	0.627	0.111			
0 to 1	0.0672	0.0714	0.389	0.269	0.042	0.0010	1.146	0.339	0.056			
0 to 0.5	0.0672	0.0714	0.205	0.134	0.021	0.0010	0.583	0.169	0.028			
0 to 0.2	0.0672	0.0714	0.095	0.076	0.010	0.0010	0.247	0.088	0.013			
0 to 0.1	0.0672	0.0714	0.058	0.056	0.006	0.0010	0.135	0.064	0.008			

**Note:** Accuracies are valid for measurements following an internal E-Series calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory-calibration temperature. NI recommends a one-year calibration interval. The Absolute Accuracy at Full Scale calculations were performed for a maximum range input voltage (for example, 10 V for the ±10 V range) after one year, assuming 100 points of averaged data. Go to [ni.com/info](http://ni.com/info) and enter info code `rdaspec` for example calculations.

## Transfer Characteristics

### Relative accuracy

Dithered .....	±0.5 least significant bits (LSB) typ
Undithered .....	±1.5 LSB max

Differential nonlinearity (DNL)..... ±0.5 LSB typ, ±1 LSB max

No missing codes ..... 12 bits, guaranteed

### Offset error

Pregain error after calibration.....	±16 $\mu$ V max
Pregain error before calibration.....	±4.0 mV max
Postgain error after calibration...	±0.8 mV max
Postgain error before calibration.....	±200 mV max

### Gain error (relative to calibration reference)

After calibration (gain = 1).....	±0.02% of reading max
Before calibration .....	±2.5% of reading max
Gain $\neq$ 1 with gain error adjusted to 0 at gain = 1.....	±0.02% of reading max

## Amplifier Characteristics

### Input impedance

Normal powered on .....	100 G $\Omega$ in parallel with 100 pF
Powered off .....	820 $\Omega$ min
Overload .....	820 $\Omega$ min

Input bias current ..... ±200 pA

Input offset current..... ±100 pA

CMRR, all input ranges, DC to 60 Hz

Range	CMRR
10 to 20 V	85 dB
5 V	95 dB
100 mV to 2 V	100 dB

## Dynamic Characteristics

### Bandwidth

Small signal (–3 dB) .....	600 kHz
Large signal (1% THD) .....	350 kHz

Settling time to full-scale step

Range	Accuracy*		
	±0.012% (±0.5 LSB)	±0.024% (±1 LSB)	±0.098% (±4 LSB)
All	4 $\mu$ S typ, 8 $\mu$ S max	4 $\mu$ S max	4 $\mu$ S max

\* Accuracy values are valid for source impedances <1 k $\Omega$ . Refer to *Multichannel Scanning Considerations* of the *E Series Help* for more information.

System noise (LSB<sub>rms</sub>, not including quantization)

Range	Dither Off	Dither On
1 to 20 V	0.2	0.5
500 mV	0.25	0.5
200 mV	0.5	0.7
100 mV	0.9	1.0

Crosstalk (DC to 100 kHz)

Adjacent channels .....	–75 dB
All other channels .....	–90 dB

## Stability

Offset temperature coefficient

Pregain .....	±5 $\mu$ V/°C
Postgain.....	±240 $\mu$ V/°C

Gain temperature coefficient..... ±20 ppm/°C

## Analog Output

### Output Characteristics

Number of channels.....2 voltage

Resolution.....12 bits, 1 in 4,096

Max update rate (waveform generation)

FIFO Mode		Non-FIFO Mode	
Internally Timed	Externally Timed	1 Channel	2 Channels
1 MS/s	950 kS/s	800 kS/s, system-dependent	400 kS/s, system-dependent

Type of D/A converter (DAC) .....Double-buffered, multiplying

FIFO buffer size .....512 Samples (S)

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Scatter-gather (single-transfer, demand-transfer)

### Accuracy Information

Nominal Range (V)		Absolute Accuracy					Absolute Accuracy at Full Scale (mV)
Positive Full Scale	Negative Full Scale	% of Reading			Offset (mV)	Temp Drift (%/°C)	
		24 Hours	90 Days	1 Year			
10	-10	0.0177	0.0197	0.0219	5.93	0.0005	8.127
10	0	0.0177	0.0197	0.0219	3.49	0.0005	5.685

**Note:** Accuracies are valid for measurements following an internal E Series calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings. Measurement accuracies are listed for operational temperatures within  $\pm 1^\circ\text{C}$  of internal calibration temperature and  $\pm 10^\circ\text{C}$  of external or factory-calibration temperature. NI recommends a one-year calibration interval. The Absolute Accuracy at Full Scale calculations were performed for a maximum range input voltage (for example, 10 V for the  $\pm 10$  V range) after one year, assuming 100 points of averaged data. Go to [ni.com/info](http://ni.com/info) and enter info code `rdspec` for example calculations.

### Transfer Characteristics

Relative accuracy, or integral nonlinearity (INL)  
 After calibration ..... $\pm 0.3$  LSB typ,  
 $\pm 0.5$  LSB max  
 Before calibration ..... $\pm 4$  LSB max

DNL  
 After calibration ..... $\pm 0.3$  LSB typ,  
 $\pm 1.0$  LSB max  
 Before calibration ..... $\pm 3$  LSB max

Monotonicity.....12 bits, guaranteed after calibration

Offset error  
 After calibration ..... $\pm 1.0$  mV max  
 Before calibration ..... $\pm 200$  mV max

Gain error (relative to internal reference)  
 After calibration .....  $\pm 0.01\%$  of output max  
 Before calibration .....  $\pm 0.5\%$  of output max

Gain error  
 (relative to external reference) ..... 0 to 0.67% of output max,  
 not adjustable

### Voltage Output

Ranges .....  $\pm 10$  V, 0 to 10 V,  
 $\pm$ AO EXT REF,  
 0 to AO EXT REF  
 (software-selectable)

Output coupling ..... DC

Output impedance .....  $0.1 \Omega$  max

Current drive .....  $\pm 5$  mA max

Protection ..... Short-circuit to ground

Power-on state ..... 0 V ( $\pm 200$  mV)

External reference input  
 Range .....  $\pm 11$  V  
 Overvoltage protection  
 Powered on .....  $\pm 25$  V  
 Powered off .....  $\pm 15$  V  
 Input impedance ..... 10 k $\Omega$   
 Bandwidth ( $-3$  dB) ..... 1 MHz

### Dynamic Characteristics

Settling time for full-scale step ..... 3  $\mu$ s to  $\pm 0.5$  LSB  
 accuracy

Slew rate ..... 20 V/ $\mu$ s

Noise ..... 200  $\mu$ V<sub>rms</sub>,  
 DC to 1 MHz

Glitch energy (at mid-scale transition)  
 Reglitching disabled .....  $\pm 20$  mV  
 Reglitching enabled .....  $\pm 4$  mV  
 Duration ..... 1.5  $\mu$ s

### Stability

Offset temperature coefficient .....  $\pm 50 \mu$ V/ $^{\circ}$ C

Gain temperature coefficient  
 Internal reference .....  $\pm 25$  ppm/ $^{\circ}$ C  
 External reference .....  $\pm 25$  ppm/ $^{\circ}$ C

### Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... 5 V TTL

Digital logic levels on P0.<0..7>

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Input low current ( $V_{in} = 0$ V)	—	$-320 \mu$ A
Input high current ( $V_{in} = 5$ V)	—	10 $\mu$ A
Output low voltage ( $I_{OL} = 24$ mA)	—	0.4 V
Output high voltage ( $I_{OH} = -13$ mA)	4.35 V	—

Power-on state ..... Input (high-impedance)

Data transfers ..... Programmed I/O

Transfer rate (1 word = 8 bits)  
 Maximum with NI-DAQ,  
 system-dependent ..... 50 kwords/s

Constant sustainable rate ..... 1 to 10 kwords/s, typ

### Timing I/O

Number of channels ..... 2 up/down  
 counter/timers,  
 1 frequency scaler

Resolution  
 Counter/timers ..... 24 bits  
 Frequency scaler ..... 4 bits

Compatibility ..... 5 V TTL/CMOS

Base clocks available  
 Counter/timers ..... 20 MHz, 100 kHz  
 Frequency scaler ..... 10 MHz, 100 kHz

Base clock accuracy .....  $\pm 0.01\%$

Max source frequency  
 up/down counter/timers ..... 20 MHz

Min source pulse duration ..... 10 ns

Min gate pulse duration ..... 10 ns, edge-detect mode

Data transfers ..... DMA, interrupts,  
 programmed I/O

Data transfers.....	DMA, interrupts, programmed I/O
DMA modes .....	Scatter-gather (single-transfer, demand-transfer)

## Triggers

### Analog Trigger

Source .....	AI <0..15>, external trigger (PFI 0/AI START TRIG)
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#### Purpose

Analog input .....	Start, reference, and pause trigger, sample clock
Analog output .....	Start and pause trigger, sample clock
Counter/timers .....	Source, gate

#### Level

Internal .....	±Full-scale
External .....	±10 V

Slope .....	Positive or negative (software-selectable)
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Resolution.....	8 bits, 1 in 256
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Hysteresis .....	Programmable
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Bandwidth (–3 dB) .....	650 kHz, internal; 3 MHz, external
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#### External input (PFI 0/AI START TRIG)

Impedance .....	10 kΩ
Coupling.....	DC

#### Protection

When configured as a digital signal .....	–0.5 to VCC + 0.5 V
When configured as an analog trigger signal or disabled .....	±35 V
Powered off .....	±35 V

### Digital Trigger

#### Purpose

Analog input .....	Start, reference, and pause trigger, sample clock
Analog output .....	Start and pause trigger, sample clock
Counter/timers .....	Source, gate

External sources .....	PFI <0..9>, RTSI <0..6>
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Compatibility .....	5 V TTL
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Response .....	Rising or falling edge
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Pulse width.....	10 ns min
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### RTSI Bus (PCI Only)

Trigger lines .....	7
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### PXI Trigger Bus (PXI Only)

Trigger lines .....	6
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Star trigger .....	1
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## Calibration

Recommended warm-up time .....	15 minutes
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Calibration interval .....	1 year
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External calibration reference .....	>6 and <10 V
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#### Onboard calibration reference

DC level.....	5.000 V (±3.5 mV), over full operating temperature, actual value stored in EEPROM
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Temperature coefficient .....	±5 ppm/°C max
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Long-term stability .....	±15 ppm/ $\sqrt{1,000 \text{ h}}$
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## Bus Interface

Type .....	Master, slave
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## Power

### Bus Requirement

+5 VDC (±5%) .....	1.0 A
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**Note** Excludes power consumed through +5 V available at the I/O connector.

### I/O Connector Power

Power available at I/O connector....	+4.65 to +5.25 VDC at 1 A
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## Physical

#### Dimensions (not including connectors)

NI PXI-6040E .....	16 cm × 10 cm (6.3 in. × 3.9 in.)
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NI PCI-MIO-16E-4 .....	17.5 cm × 10.7 cm (6.9 in. × 4.2 in.)
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#### Weight

NI PXI-6040E .....	218 g (7.7 oz)
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NI PCI-MIO-16E-4 .....	116 g (4.1 oz)
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I/O connector .....	68-pin male 0.050 D-type
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## Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth .....	11 V, Installation Category I
Channel-to-channel .....	11 V, Installation Category I

## Environmental

Operating temperature .....	0 to 55 °C
Storage temperature .....	-20 to 70 °C
Relative humidity .....	10 to 90%, noncondensing
Maximum altitude .....	2,000 m
Pollution Degree (indoor use only) .....	2

## Safety

The NI 6040E devices meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1
- CAN/CSA-C22.2 No. 61010-1



**Note** For UL and other safety certifications, refer to the product label, or visit [ni.com/certification](http://ni.com/certification), search by model number or product line, and click the appropriate link in the Certification column.

## Electromagnetic Compatibility

Emissions .....	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz
Immunity .....	EN 61326:1997 A2:2001, Table 1
CE, C-Tick, and FCC Part 15 (Class A) Compliant	



**Note** For EMC compliance, operate this device with shielded cabling.

## CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

Low-Voltage Directive (safety) .....	73/23/EEC
Electromagnetic Compatibility Directive (EMC) .....	89/336/EEC



**Note** Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit [ni.com/certification](http://ni.com/certification), search by model number or product line, and click the appropriate link in the Certification column.

AI 8	34	68	AI 0
AI 1	33	67	AI GND
AI GND	32	66	AI 9
AI 10	31	65	AI 2
AI 3	30	64	AI GND
AI GND	29	63	AI 11
AI 4	28	62	AI SENSE
AI GND	27	61	AI 12
AI 13	26	60	AI 5
AI 6	25	59	AI GND
AI GND	24	58	AI 14
AI 15	23	57	AI 7
AO 0	22	56	AI GND
AO 1	21	55	AO GND
AO EXT REF	20	54	AO GND
P0.4	19	53	D GND
D GND	18	52	P0.0
P0.1	17	51	P0.5
P0.6	16	50	D GND
D GND	15	49	P0.2
+5 V	14	48	P0.7
D GND	13	47	P0.3
D GND	12	46	AI HOLD COMP
PFI 0/AI START TRIG	11	45	EXT STROBE
PFI 1/AI REF TRIG	10	44	D GND
D GND	9	43	PFI 2/AI CONV CLK
+5 V	8	42	PFI 3/CTR 1 SRC
D GND	7	41	PFI 4/CTR 1 GATE
PFI 5/AO SAMP CLK	6	40	CTR 1 OUT
PFI 6/AO START TRIG	5	39	D GND
D GND	4	38	PFI 7/AI SAMP CLK
PFI 9/CTR 0 GATE	3	37	PFI 8/CTR 0 SRC
CTR 0 OUT	2	36	D GND
FREQ OUT	1	35	D GND

Figure 1. NI PXI-6040E/PCI-MIO-16E-4 Pinout

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