NIM Standard

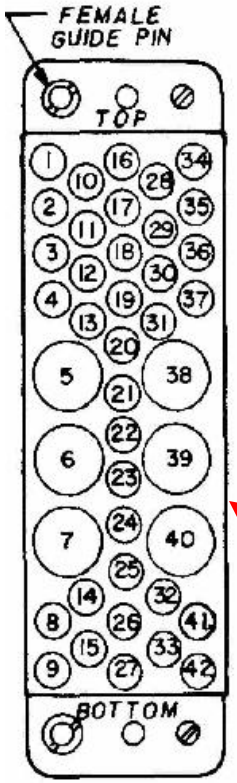
NIM is an acronym for Nuclear Instrumentation Methods. The NIM standard (DOE/ER-0457) was established in 1964 for the nuclear and high energy physics communities. The goal of NIM was to promote the interchangeability of instrumentation modules. Standard NIM modules are 8.75 inches tall and a width which is a multiple of 1.35 inches (= "single width"; "double width" = 2.7 inches)

Example: extended pin set

Well Logging NIMS Bin (NIM Crate) Pinout			
Pin	Description	Pin	Description
1	Bell/Worth Temp. Interconnect	22	
2	Bell/Worth Bond Gate	23	
3		24	
4	Bell/Worth Scope	25	
5		26	
6		27	
7		28	+24 Volts (Not In All Bell Bins)
8	Voltage Control - 300 Volt P.S.	29	-24 Volts (Not In All Bell Bins)
9	+300 Volts Downhole P.S.*	30	
10	+6 Volts / Non-Bell Bond Gate	31	
11	-6 Volts (If Implemented)	32	
12		33	120vac Line Power "Hot"
13		34	Ground, Clean (Digital)**
14	-300 Volts Downhole P.S.*	35	
15		36	Bell/Worth Scope Sync
16	+12 Volts (Always Present)	37	Bell/Worth Recorder
17	-12 Volts (Always Present)	38	
18	Electrode #1	39	
19	Bell/Worth Scope Z Mod	40	RA Logging Line (Coax)
20	Electrode #2	41	120vac Line power "Neutral"
21	Electrode #3	42	Ground, Dirty (Signal)**

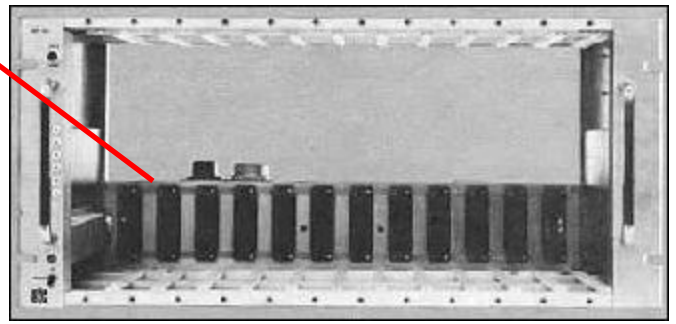
* ±250 or ±200 Volts in Comprobe bins.
**Pins 34 and 42 are usually connected together in logging bins.

Bin connector front (looking into bin)



Module

Bin



CAMAC Standard

CAMAC is also an acronym: Computer Automated Measurement and Control. The CAMAC standard (IEEE 583) was established in 1975 and has been used in virtually every physics laboratory and many industrial applications. While other modular instrumentation standards have been widely adopted, the robust CAMAC module and enclosure construction and simple hardware level interface means CAMAC is still a viable choice for instrument applications today.

CAMAC Dataway Pinout

P1	1	1R	B
P2	2	2R	F16
P3	3	3R	F8
P4	4	4R	F4
P5	5	5R	F2
X	6	6R	F1
I	7	7R	A8
C	8	8R	A4
N	9	9R	A2
L	10	10R	A1
S1	11	11R	Z
S2	12	12R	Q
W24	13	13R	W23
W22	14	14R	W21
W20	15	15R	W19
W18	16	16R	W17
W16	17	17R	W15
W14	18	18R	W13
W12	19	19R	W11
W10	20	20R	W9
W8	21	21R	W7
W6	22	22R	W5
W4	23	23R	W3
W2	24	24R	W1
R24	25	25R	R23
R22	26	26R	R21
R20	27	27R	R19
R18	28	28R	R17
R16	29	29R	R15
R14	30	30R	R13
R12	31	31R	R11
R10	32	32R	R9
R8	33	33R	R7
R6	34	34R	R5
R4	35	35R	R3
R2	36	36R	R1
-12V	37	37R	-24V
—	38	38R	-6V
—	39	39R	—
Y1	40	40R	E
+12V	41	41R	+24V
Y2	42	42R	+6V
GND	43	43R	GND

Separate 24-bit Read/Write Busses

Simple FNAD commanding:

e.g. F = 0 (read)

N = 1 (crate slot)

A = card channel #

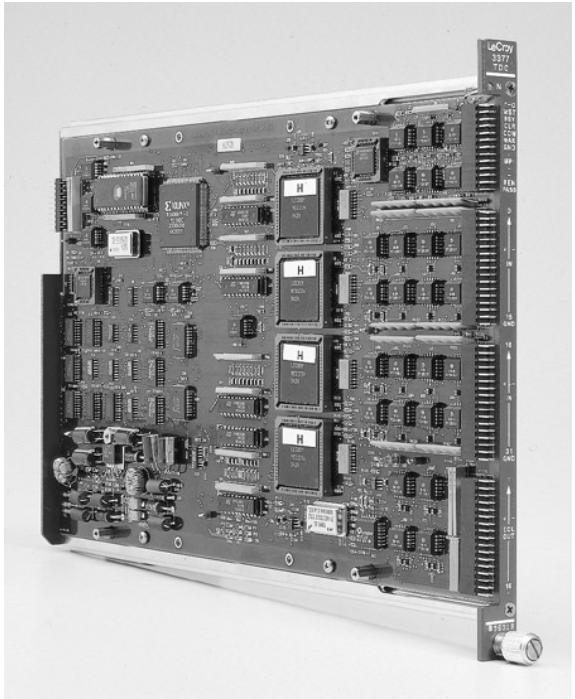
D = data (either)

Z = initialize (reset)

X = I'm responding

Q = zero suppress

L = LAM (Look-At-Me)



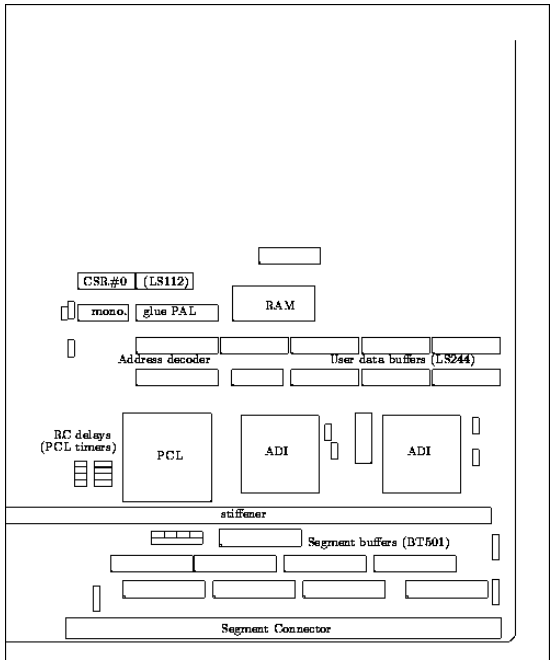
LeCroy 3377 500ps multi-hit TDC

FASTBUS Standard

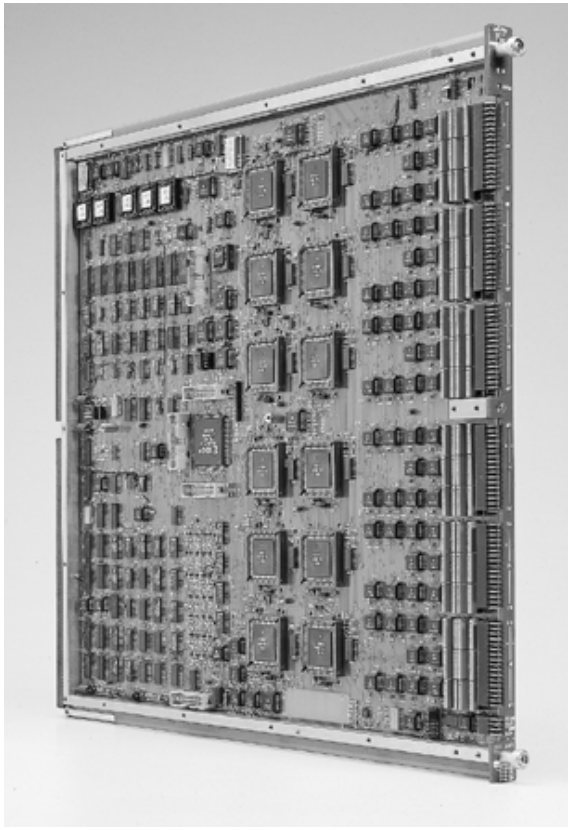
FASTBUS is a standard largely exclusive to High Energy Physics. Detailed in ANSI/IEEE 960 and IEC-547, it is designed for VERY high power operation (many kW per crate – from the age of ECL)

Hundreds of pins, Impossible to detail here and it is likely you will never need to know this.

Mechanics are frightening: bed of nails in back. However the performance can be excellent!



Back edge

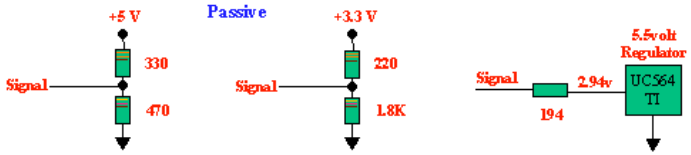


LeCroy 1877S 500ps multi-hit TDC
96-channels – backbone of Belle Exp.

VME Standard

Developed to allow high-density CPU/Memory/IO/Data Acquisition (DAQ) on a common bus.

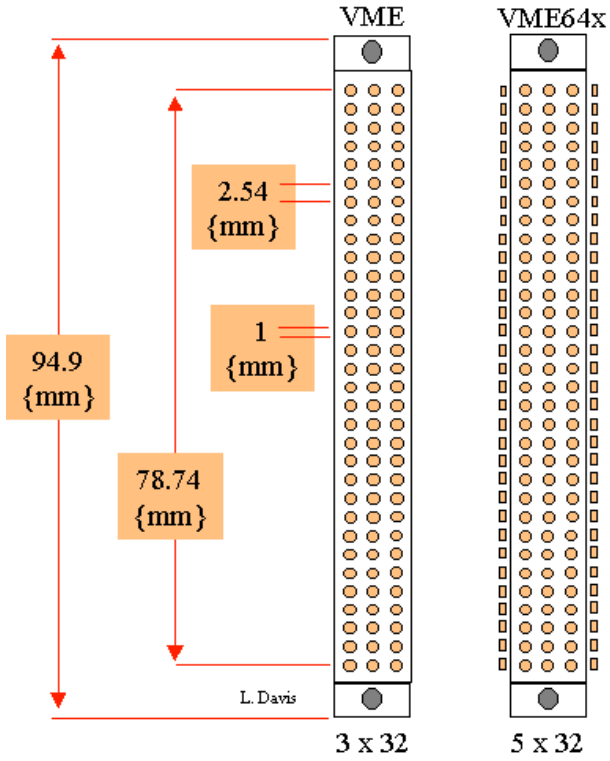
Terminated transmission lines



A computer standard

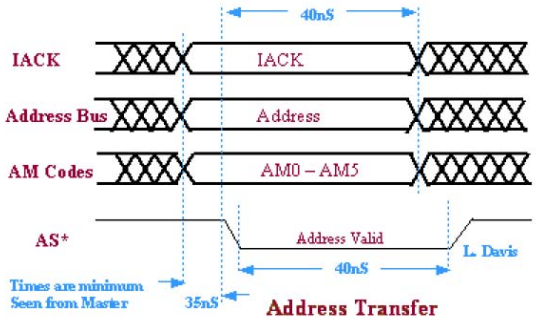
Pin	Signal Name Row A	Signal Name Row B	Signal Name Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSREST*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V Standby	+12V
32	+5V	+5v	+5V

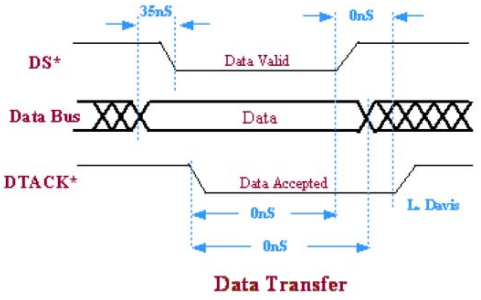
Pin	Signal Name Row A	Signal Name Row B	Signal Name Row C
1	NC	+5V	NC
2	NC	GND	NC
3	NC	RESERVED	NC
4	NC	A24	NC
5	NC	A25	NC
6	NC	A26	NC
7	NC	A27	NC
8	NC	A28	NC
9	NC	A29	NC
10	NC	A30	NC
11	NC	A31	NC
12	NC	GND	NC
13	NC	+5V	NC
14	NC	D16	NC
15	NC	D17	NC
16	NC	D18	NC
17	NC	D19	NC
18	NC	D20	NC
19	NC	D21	NC
20	NC	D22	NC
21	NC	D23	NC
22	NC	GND	NC
23	NC	D24	NC
24	NC	D25	NC
25	NC	D26	NC
26	NC	D27	NC
27	NC	D28	NC
28	NC	D29	NC
29	NC	D30	NC
30	NC	D31	NC
31	NC	GND	NC
32	NC	+5v	NC

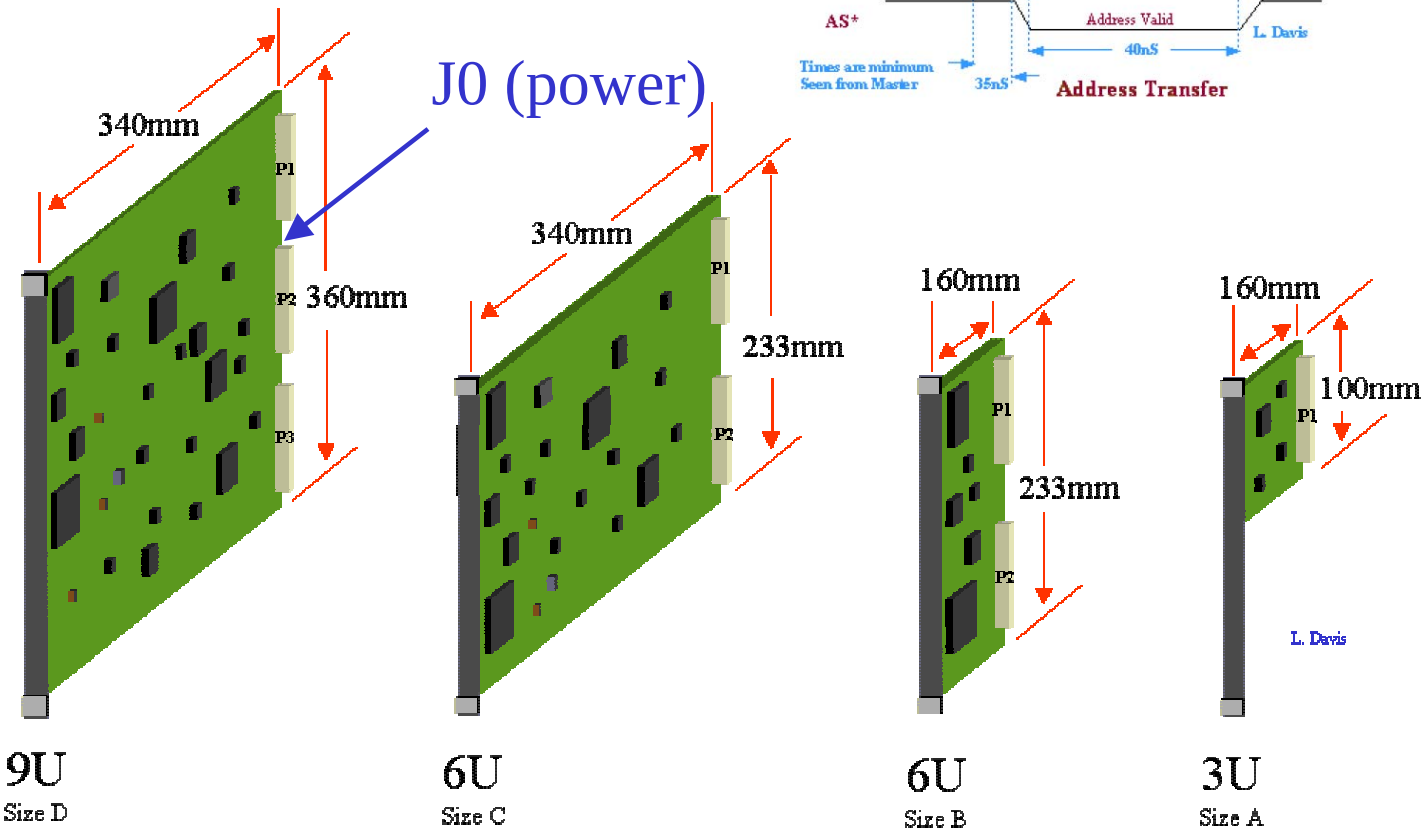


VIPA (VME64) Standard

Many extensions (too numerous to list) to allow higher speed, more usable area beyond 160mm deep 6U Eurocard standard. 5 row connectors added to help with lack of power.

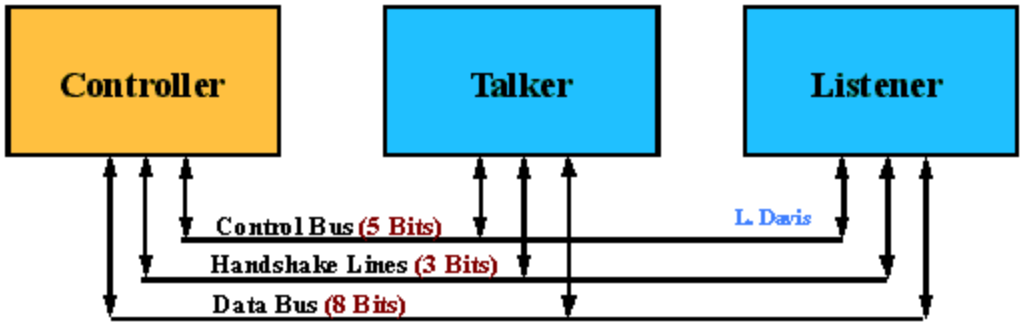






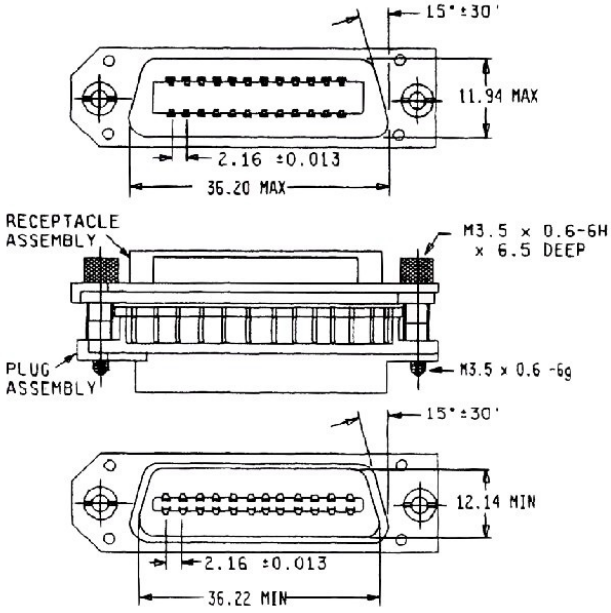
GPIB/HPIB

The IEEE-488 standard goes under a number of names (General Purpose Interface Bus/ Hewlett-Packard Interface Bus). 600kByte/s max. Convenient for slow acquistion/control.



Pin	Signal Name	Function	Pin	Signal Name	Function
1	DIO1	Data input/output bit 1	13	DIO5	Data input/output bit 5
2	DIO2	Data input/output bit 2	14	DIO6	Data input/output bit 6
3	DIO3	Data input/output bit 3	15	DIO7	Data input/output bit 7
4	DIO4	Data input/output bit 4	16	DIO8	Data input/output bit 8
5	EOI	End-or-identify	17	REN	Remote enable
6	DAV	Data valid	18	SHIELD	Ground (DAV)
7	NRFD	Not ready for data	19	SHIELD	Ground (NRFD)
8	NDAC	Not data accepted	20	SHIELD	Ground (NDAC)
9	IFC	Interface clear	21	SHIELD	Ground (IFC)
10	SRQ	Service request	22	SHIELD	Ground (SRQ)
11	ATN	Attention	23	SHIELD	Ground (ATN)
12	SHIELD	Chassis ground	24	SIGNAL GND	Signal ground

Common interface for high-end instruments

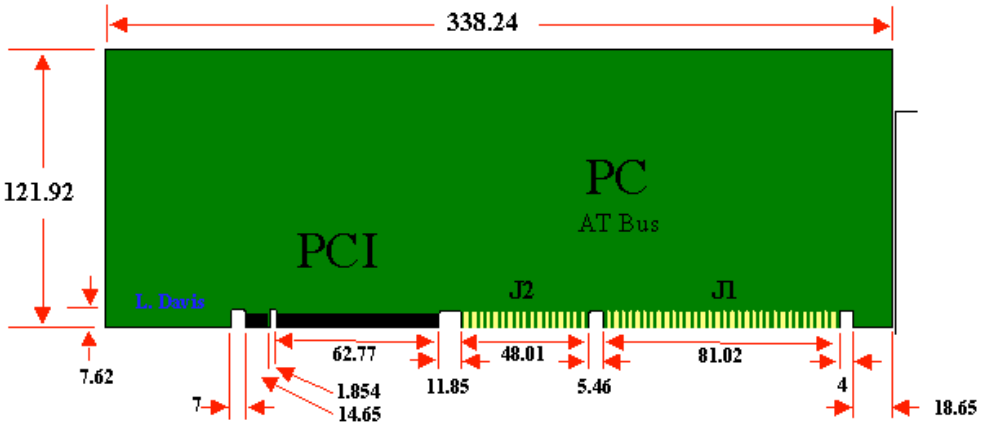


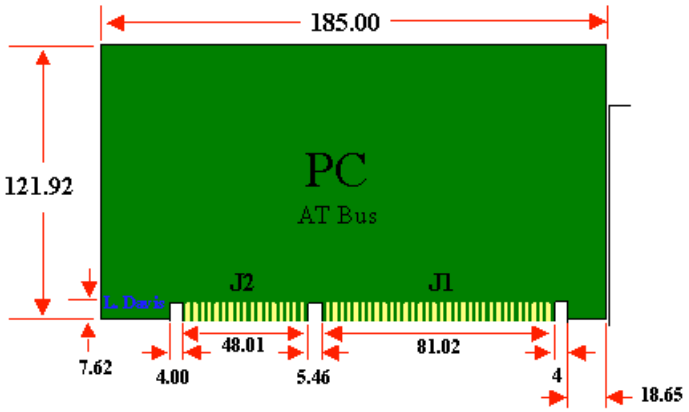
Hermaphrodite connectors easy to daisy-chain and stack.

ISA Bus

(Industry Standard Architecture) At 8MHz and 8/16 bit data bus, was the original PX-XT bus. This flexibility and open standard allowed the PC to bury the Apple.

Two popular card configurations





PC [ISA] XT/AT Connector Pin-Out

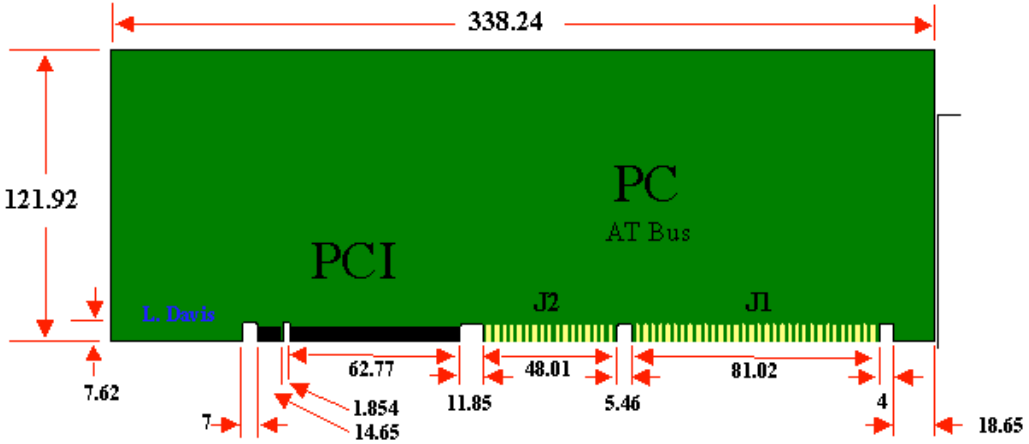
Pin	J1		J2	
#	A Row	B Row	C Row	D Row
1	Channel Check	Ground	System Enable	Memory 16 bit select
2	Data 7	Reset	Unlatched Address 22	I/O 16bit Chip Select
3	Data 6	+5v	Unlatched Address 23	IRQ10
4	Data 5	IRQ9	Unlatched Address 21	IRQ11
5	Data 4	-5v	Unlatched Address 20	IRQ12
6	Data 3	DMA Request 2	Unlatched Address 19	IRQ15
7	Data 2	-12v	Unlatched Address 18	IRQ14
8	Data 1	Zero Wait State	Unlatched Address 17	DMA ACK0
9	Data 0	+12v	Memory Read	DMA Request 0
10	I/O Channel Ready	Ground	Memory Write	DMA ACK5
11	Address Enable	Real Memory Write	Data 8	DMA Request 5
12	Address 19	Real Memory Read	Data 9	DMA ACK6
13	Address 18	I/O Write	Data 10	DMA Request 6
14	Address 17	I/O Read	Data 11	DMA ACK7
15	Address 16	DMA ACK3	Data 12	DMA request 7
16	Address 15	DMA Request 3	Data 13	+5v
17	Address 14	DMA ACK1	Data 14	Master
18	Address 13	DMA Request 1	Data 15	Ground
19	Address 12	Refresh	N/A	N/A
20	Address 11	CLK	N/A	N/A
21	Address 10	IRQ7	N/A	N/A
22	Address 9	IRQ6	N/A	N/A
23	Address 8	IRQ5	N/A	N/A
24	Address 7	IRQ4	N/A	N/A
25	Address 6	IRQ3	N/A	N/A
26	Address 5	DMA ACK2	N/A	N/A
27	Address 4	Terminal Count	N/A	N/A
28	Address 3	Address Latch En	N/A	N/A
29	Address 2	+5v	N/A	N/A
30	Address 1	Oscillator	N/A	N/A
31	Address 0	Ground	N/A	N/A

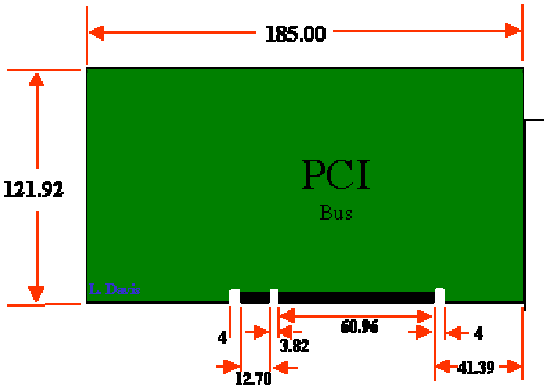
The **PCXT** bus uses the J1 A/B rows, and a **PCAT** bus uses the J1 [A/B rows] and J2 [C/D rows] connectors. The fingers are copper strips on the PWB spaced on 0.1 inch centers. The PCAT bus was an up-grade to the original PCXT bus.

PCI Bus

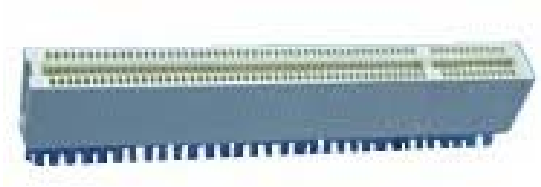
(Peripheral Components Interface) High-speed successor to the venerable ISA bus.

Reflective wave transmission: max. 7 slots





PMC, PCMCIA variants



PCI [Parallel] Bus Pin-Out

Pin	Name	Description	Pin	Name	Description
A1	TRST	Test Logic Reset	B1	-12V	-12 VDC
A2	+12V	+12 VDC	B2	TCK	Test Clock
A3	TMS	Test Mode Select	B3	GND	Ground
A4	TDI	Test Data Input	B4	TDO	Test Data Output
A5	+5V	+5 VDC	B5	+5V	+5 VDC
A6	INTA	Interrupt A	B6	+5V	+5 VDC
A7	INTC	Interrupt C	B7	INTB	Interrupt B
A8	+5V	+5 VDC	B8	INTD	Interrupt D
A9	---	Reserved	B9	PRSNT1	Present
A10	+5V	Power(+5 Vor+3.3 V)	B10	---	Reserved
A11	---	Reserved	B11	PRSNT2	Present
A12	GND03	Ground or Keyway for 3.3Universal PWB	B12	GND	Ground or Keyway for 3.3Universal PWB
A13	GND03	Ground or Keyway for 3.3Universal PWB	B13	GND	Ground or Open (Key) for 3.3Universal PWB
A14	3.3Vaux	---	B14	RES	Reserved
A15	RSTH	Reset	B15	GND	Ground
A16	+5V	Power(+5 Vor+3.3 V)	B16	CLK	Clock
A17	GNT	Grant PCI bus	B17	GND	Ground
A18	GND08	Ground	B18	REQ	Request
A19	PMEN	Power Management Event	B19	+5V	Power(+5 Vor+3.3 V)
A20	AD30	Address/Data 30	B20	AD31	Address/Data 31
A21	+3.3V01	+3.3 VDC	B21	AD29	Address/Data 29
A22	AD28	Address/Data 28	B22	GND	Ground
A23	AD26	Address/Data 26	B23	AD27	Address/Data 27
A24	GND10	Ground	B24	AD25	Address/Data 25
A25	AD24	Address/Data 24	B25	+3.3V	+3.3 VDC
A26	IDSEL	Initialization Device Select	B26	C/BE3	Command, Byte Enable 3
A27	+3.3V03	+3.3 VDC	B27	AD23	Address/Data 23
A28	AD22	Address/Data 22	B28	GND	Ground
A29	AD20	Address/Data 20	B29	AD21	Address/Data 21
A30	GND12	Ground	B30	AD19	Address/Data 19
A31	AD18	Address/Data 18	B31	+3.3V	+3.3 VDC
A32	AD16	Address/Data 16	B32	AD17	Address/Data 17
A33	+3.3V03	+3.3 VDC	B33	C/BE2	Command, Byte Enable 2
A34	FRAME	Address or Data phase	B34	GND13	Ground
A35	GND14	Ground	B35	IRDY	Initiator Ready
A36	TRDY	Target Ready	B36	+3.3V04	+3.3 VDC
A37	GND15	Ground	B37	DEVSEL	Device Select
A38	STOP	Stop Transfer Cycle	B38	GND16	Ground
A39	+3.3V07	+3.3 VDC	B39	LOCK	Lock Bus
A40	---	Reserved	B40	PERR	Parity Error
A41	---	Reserved	B41	+3.3V08	+3.3 VDC
A42	GND17	Ground	B42	SERR	System Error
A43	PAR	Parity	B43	+3.3V09	+3.3 VDC
A44	AD15	Address/Data 15	B44	C/BE1	Command, Byte Enable 1
A45	+3.3V10	+3.3 VDC	B45	AD14	Address/Data 14
A46	AD13	Address/Data 13	B46	GND18	Ground
A47	AD11	Address/Data 11	B47	AD12	Address/Data 12
A48	GND19	Ground	B48	AD10	Address/Data 10
A49	AD9	Address/Data 9	B49	GND20	Ground
A50	Keyway	Open or Ground for 3.3VPWB	B50	Keyway	Open or Ground for 3.3VPWB
A51	Keyway	Open or Ground for 3.3VPWB	B51	Keyway	Open or Ground for 3.3VPWB
A52	C/BE0	Command, Byte Enable 0	B52	AD8	Address/Data 8
A53	+3.3V11	+3.3 VDC	B53	AD7	Address/Data 7
A54	AD6	Address/Data 6	B54	+3.3V12	+3.3 VDC
A55	AD4	Address/Data 4	B55	AD5	Address/Data 5
A56	GND21	Ground	B56	AD3	Address/Data 3
A57	AD2	Address/Data 2	B57	GND22	Ground
A58	AD0	Address/Data 0	B58	AD1	Address/Data 1
A59	+5V	Power(+5 Vor+3.3 V)	B59	VCC08	Power(+5 Vor+3.3 V)
A60	REQ64	Request 64 bit	B60	ACK64	Acknowledge 64 bit
A61	VCC11	+5 VDC	B61	VCC10	+5 VDC
A62	VCC13	+5 VDC	B62	VCC12	+5 VDC
		64 bit pass KEYWAY			
		64 bit pass KEYWAY			
A63	GND	Ground	B63	RES	Reserved
A64	C/BE[7]#	Command, Byte Enable 7	B64	GND	Ground
A65	C/BE[5]#	Command, Byte Enable 5	B65	C/BE[6]#	Command, Byte Enable 6
A66	+5V	Power(+5 Vor+3.3 V)	B66	C/BE[4]#	Command, Byte Enable 4
A67	PAR64	Parity 64	B67	GND	Ground
A68	AD62	Address/Data 62	B68	AD63	Address/Data 63
A69	GND	Ground	B69	AD61	Address/Data 61
A70	AD60	Address/Data 60	B70	+5V	Power(+5 Vor+3.3 V)
A71	AD58	Address/Data 58	B71	AD59	Address/Data 59
A72	GND	Ground	B72	AD57	Address/Data 57
A73	AD54	Address/Data 54	B73	GND	Ground
A74	AD56	Address/Data 56	B74	AD55	Address/Data 55
A75	+5V	Power(+5 Vor+3.3 V)	B75	AD53	Address/Data 53
A76	AD52	Address/Data 52	B76	GND	Ground
A77	AD50	Address/Data 50	B77	AD51	Address/Data 51
A78	GND	Ground	B78	AD49	Address/Data 49
A79	AD48	Address/Data 48	B79	+5V	Power(+5 Vor+3.3 V)
A80	AD46	Address/Data 46	B80	AD47	Address/Data 47
A81	GND	Ground	B81	AD45	Address/Data 45
A82	AD44	Address/Data 44	B82	GND	Ground
A83	AD42	Address/Data 42	B83	AD43	Address/Data 43
A84	+5V	Power(+5 Vor+3.3 V)	B84	AD41	Address/Data 41
A85	AD40	Address/Data 40	B85	GND	Ground
A86	AD38	Address/Data 38	B86	AD39	Address/Data 39
A87	GND	Ground	B87	AD37	Address/Data 37
A88	AD34	Address/Data 34	B88	+5V	Power(+5 Vor+3.3 V)
A89	AD36	Address/Data 36	B89	AD35	Address/Data 35
A90	GND	Ground	B90	AD33	Address/Data 33
A91	AD32	Address/Data 32	B91	GND	Ground
A92	RES	Reserved	B92	RES	Reserved
A93	GND	Ground	B93	RES	Reserved
A94	RES	Reserved	B94	GND	Ground

Compact PCI (cPCI)

An extension of PCI dedicated to chassis operation:
HOT SWAP!!

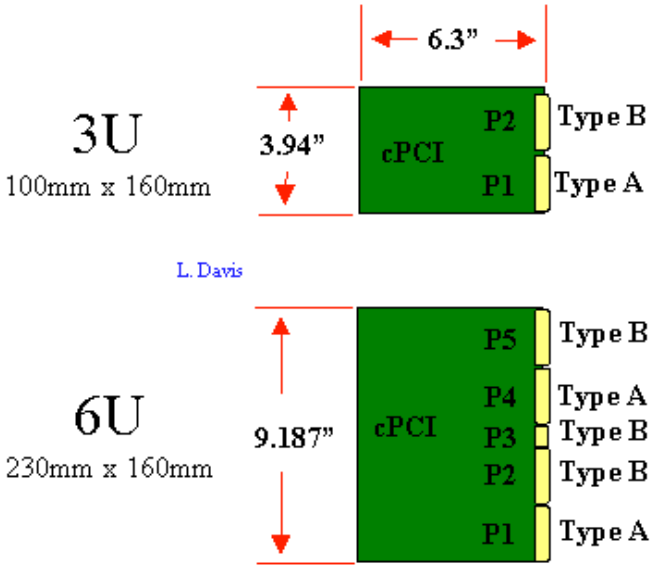
Based on same Eurocard mechanics as VME

cPCI P1 Connector Pin Out

Pin	Signal Name	Signal Name	Signal Name	Signal Name	Signal Name	Signal Name	Signal Name
--	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND
16	GND	DEV SEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*
13	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*
12	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*	*KEY*
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	BRSVP1A4	GND	V[I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

cPCI P2 Connector Pin Out

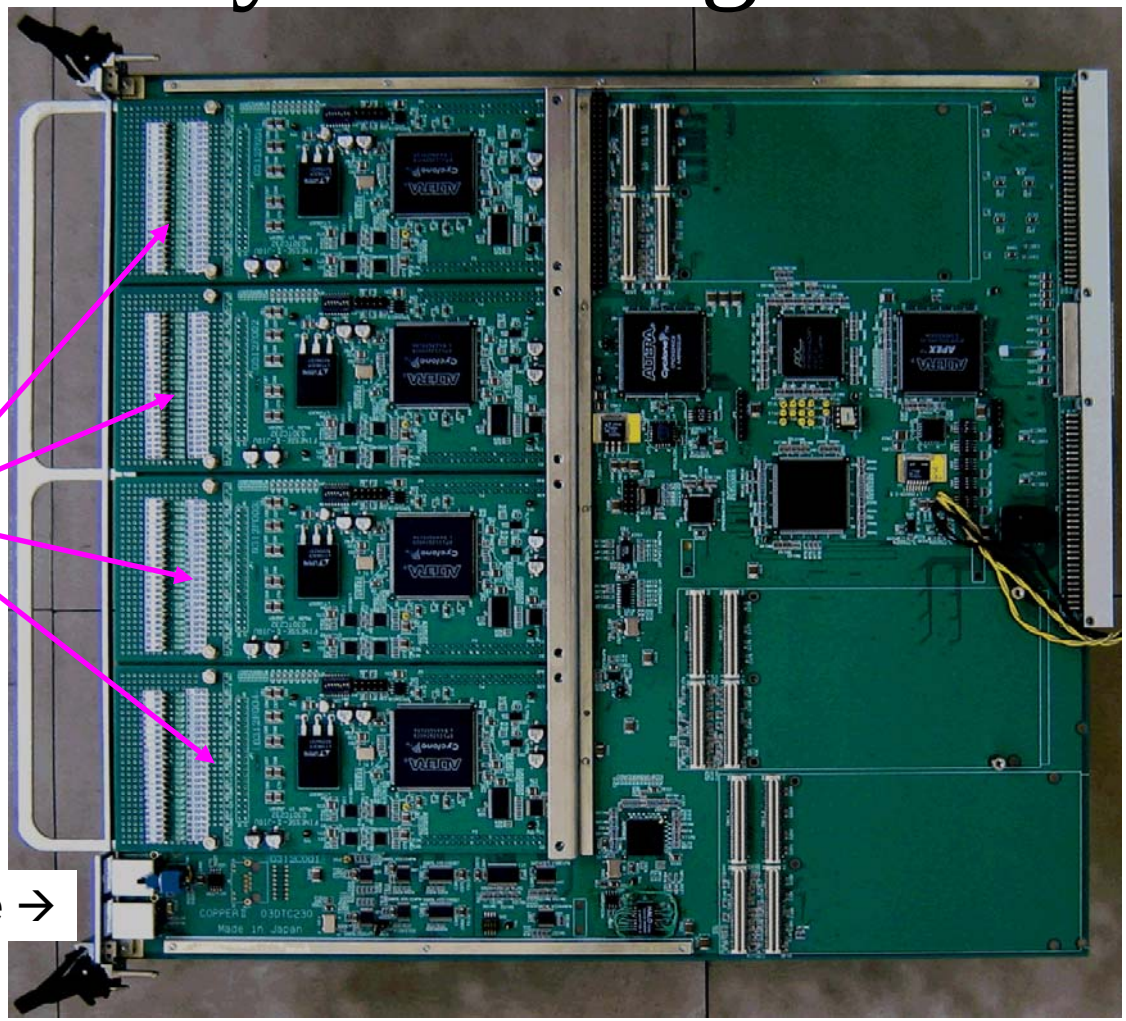
Pin	Signal Name	Signal Name	Signal Name	Signal Name	Signal Name	Signal Name	Signal Name
--	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2B16	GND
15	GND	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND
4	GND	V(I/O)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND



Euro-Card form factor with
2mm (Hard Metric) connectors

P1 only → 32 bit bus
P1&P2 → 64 bit bus
33&66 MHz clock speeds
Over 500MBytes/s possible

Custom Systems: e.g. COPPER



With on-board CPU
"crate on a board"

Needed as data rates increase: very powerful – common platform

Bizarre/Others

Because many groups have (or think they have) unique environments, they insist on designing to their own standards. Some examples:

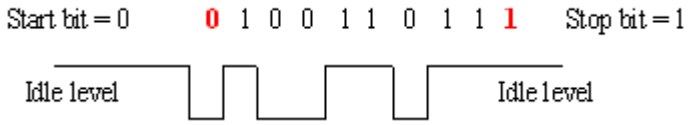
- TKO
- Rabbit
- FUTUREBUS
- VXI/PXI

Spurred by the demand for low-cost, high reliability flexible control in the IC, automotive and aircraft industries, there are a number of serial interface standards:

- CANbus and competitors
- I^2C
- JTAG
- ARCnet

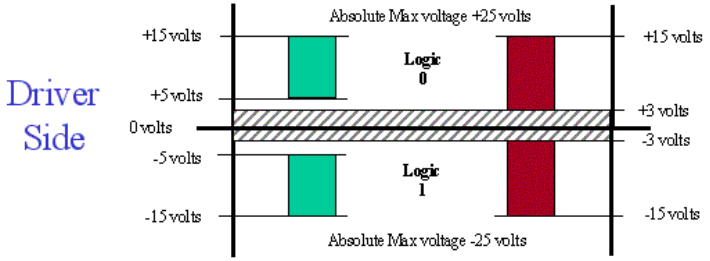
Standard Interface (I): Serial Ports

A compact, easy to implement style has kept RS-232 around despite its obvious short-comings.

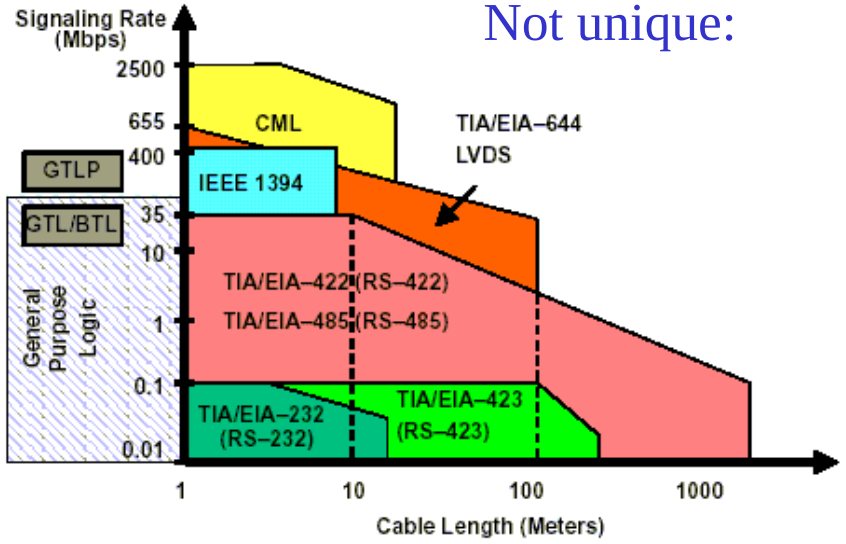


Protocol:

Number start/stop bits, Parity



Not unique:

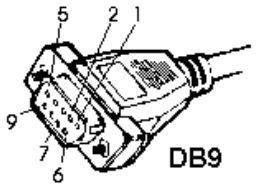


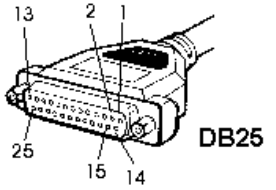
Null Modem Cable {25 pin D Connector Pin Out}

Pin	Signal Name	Description	Cable	Pin	Signal Name	Description
2	RXD	Receive Data	Cross	3	TXD	Transmit Data
3	TXD	Transmit Data	Cross	2	RXD	Receive Data
4	RTS	Request To Send	Cross	5	CTS	Clear To Send
5	CTS	Clear To Send	Cross	4	RTS	Request To Send
6	DSR	Data Set Ready	Cross	20	DTR	Data Terminal Ready
7	GND	Ground	Cross	7	GND	Ground
8	CD	Carrier Detect	Cross	20	DTR	Data Terminal Ready
20	DTR	Data Terminal Ready	Cross	6	DSR	Data Set Ready
20	DTR	Data Terminal Ready	Cross	8	CD	Carrier Detect

RJ-45 - 8 and 4 wire Pin Out

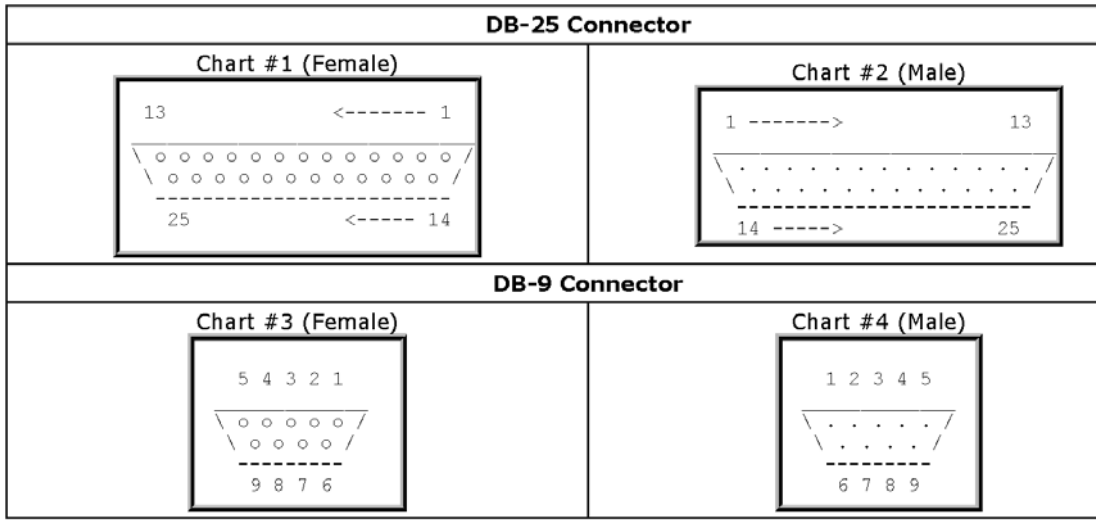
DB9, DTE		*RJ45*		DB9, DCE		******	DB25		*RJ45*		DB9	
Pin	Signal	*Pin*	*Signal*	Pin	Signal	******	Pin	Signal	*Pin*	*Signal*	Pin	Signal
7	RTS	*1*	*DCD*	1	DCD	******	4	RTS	*1*	*DCD*	7	RTS
8	CTS	*2*	*RTS*	7	RTS	******	N/A	N/A	*2*	N/A	N/A	N/A
Shell	GND	*3*	*GND*	Shell	GND	******	Shell	GND	*3*	*GND*	Shell	GND
3	RxD	*4*	*TxD*	3	TxD	******	3	RxD	*4*	*TxD*	2	RxD
2	TxD	*5*	*RxD*	4	RxD	******	2	TxD	*5*	*RxD*	3	TxD
5	GND	*6*	*GND*	5	GND	******	7	GND	*6*	*GND*	5	GND
4	DTR	*7*	*CTS*	8	CTS	******	N/A	N/A	*7*	N/A	N/A	N/A
6	DSR	*8*	*DTR*	4	DTR	******	N/A	N/A	*8*	N/A	N/A	N/A
RJ45 to DTE, DB9			N/A			******	RJ45 to DB25			N/A		
N/A		RJ45 to DCE, DB9				******	N/A		RJ45 to DB9			
@ 8 wire 8 pin RJ45						******	@ 4 wire 8 pin RJ45					

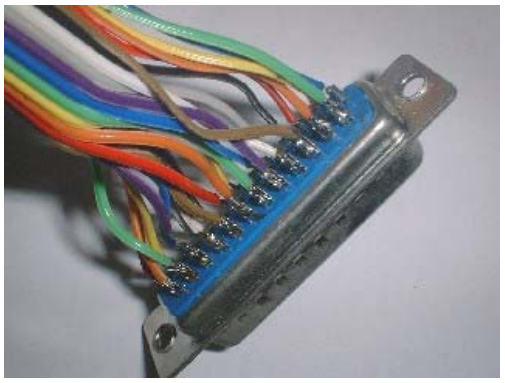




Standard Interface (II): Parallel Port

The “Printer Port” for many a generation of PCs, this is also likely in its dying days

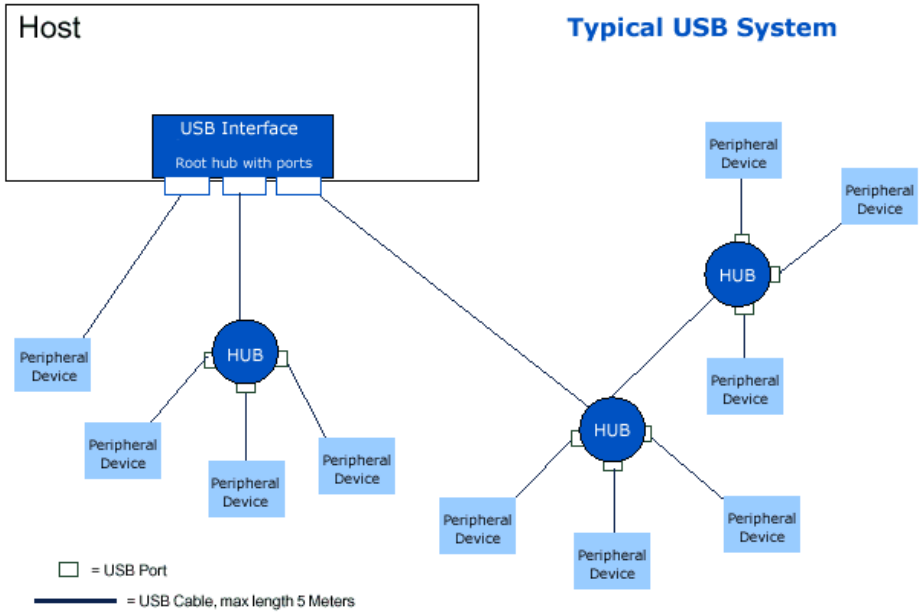




Colour	Bottom Row	Top Row	Colour	Signal	Target	Target Signal
		1	Blue	nStrobe	10	nAck
Green	14			nAutoFd	11	Busy
		2	Yellow	Data0	2	*Bidirectional*
Orange	15			*nFault	17	*nSelectIn
		3	Red	Data1	3	*Bidirectional*
Brown	16			*nInit	12	*Perror
		4	Black	Data2	4	*Bidirectional*
White	17			*nSelectIn	15	*nFault
		5	Gray	Data3	5	*Bidirectional*
Purple	18			Gnd	18	
		6	Blue	Data4	6	*Bidirectional*
Green	19			Gnd	19	
		7	Yellow	Data5	7	*Bidirectional*
Orange	20			Gnd	20	
		8	Red	Data6	8	*Bidirectional*
Brown	21			Gnd	21	
		9	Black	Data7	9	*Bidirectional*
White	22			Gnd	22	
		10	Gray	nAck	1	nStrobe
Purple	23			Gnd	23	
		11	Blue	Busy	14	nAutoFd
Green	24			Gnd	24	
		12	Yellow	*Perror	16	*nInit
Orange	25			Gnd	25	
		13	Red	*Select	13,17	
Brown	-	-		*Unused*	-	*Keep as a spare*

Standard Interface (III): USB

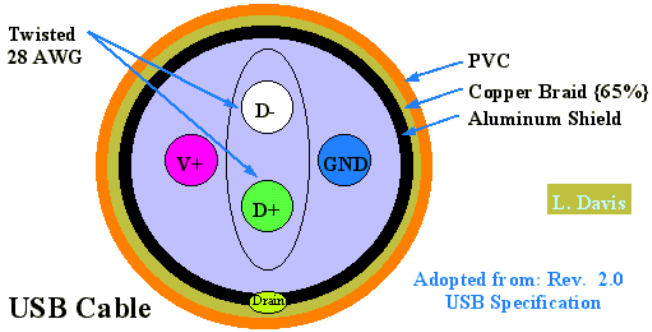
The Universal Serial Bus (USB) is currently taking over the world. Chip-sets supporting the simplest interface standard have largely done away with PS-2 and serial interfaces for keyboard/mouse.



USB1.1 – 12Mb/s
USB2 – 480Mb/s

USB Cable Assembly Pin Out

Pin	Signal Name	Description
1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
Shell	Shield	Drain



Networking

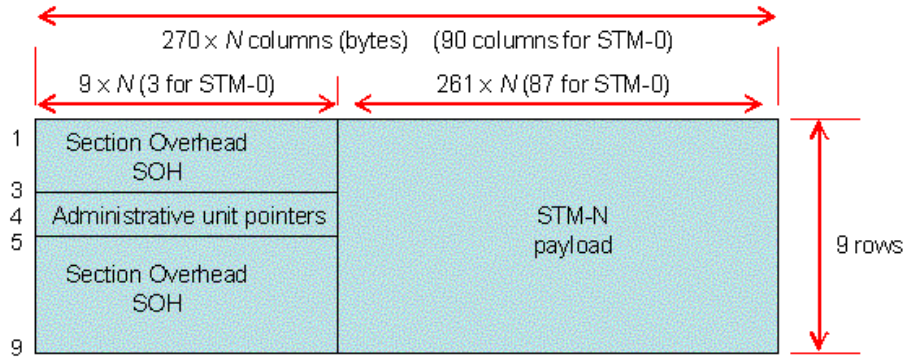
The need for high-speed interconnection…

- 10bT (coax, twisted-pair)
- 100bT
- GbE (CAT-5, fiber)
- 10GbE

- FDDI
- HIPPI
- SONET (OC-48/192/768)

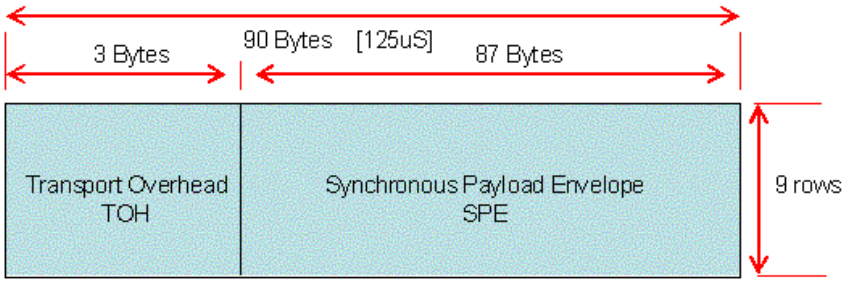
Ethernet Packet

STM Structure



Common SONET/SDH Rates

Hierarchy	Speed	SONET [US]	SDH [Europe]	OCx
----	51.84Mbps	STS-1	STM-0	OC-1
Level Zero	155.52Mbps	STS-3	STM-1	OC-3
Level One	622.08Mbps	STS-12	STM-4	OC-12
Level Two	2488.32Mbps	STS-48	STM-16	OC-48
Level Three	9953.28Mbps	STS-192	STM-64	OC-192



SONET Structure

Bus Comparison (links)

Bus	Data Rate	Type	Description	Topology	Voltage	Coax	Twisted Pair
RS-232	19.2 Kbps	Unbalanced	20 meters, Single Ended	Point-to-Point	~ 5V	15 or 25 pin cable	
RS-422	100 Kbps	Balanced	1200 meters, Differential, 100Ω	Multi-Receivers	+/-7V	------	See RS449 / 530
RS-423	100 Kbps	Hybrid	200 meters, Unbal Tx Bal Rx	Multi-Receivers	+3.6V	------	See RS449 / 530
RS-485	100 Kbps	Balanced	1200 meters, Differential	Multi-Point	+5V	------	STP or UTP
MIL-STD-1553	1.0 Mbps	Balanced	Redundant, half-duplex	Multi-Point	0 to 20V	75 Ohm Twinax	
CAN bus	1 Mbps	Balanced	High Noise Environment	Multi-Point	+16V max	------	STP or UTP
AccessBus	100 Kbps	Unbalanced	Similar to I2C, 10 meter	Multi-Point	~ 5V	4 wire,Data/Clk/V/GND	
I2C Bus	3.4 Mbps	Unbalanced	2 Wire, 1 Data, 1 Clk-Access Bus	Multi-Point	~ TTL	PWB	
SMBus	100 KHz	Unbalanced	2 Wire, based on I2C/Access Bus	Multi-Point	TTL	Undefined	
10Base2	10 Mbps	Unbalanced	183 meters, IEEE-802 Thin Net	Multi-Point	ECL	50Ω	------
10Base5	10 Mbps	Unbalanced	500 meters, IEEE-802 ThickNet	Multi-Point	ECL	50Ω	------
10Base-T	10 Mbps	Balanced	100 meters, Category 3 cable	Multi-Point	ECL	------	STP or UTP
10Base-F	10 Mbps	Fiber	2000 meters	Point-to-Point	---	Fiber	
100Base-T	100 Mbps	Balanced	100 meters, Category 5 cable	Multi-Point	+/- 1.0v	------	STP or UTP
100Base-F	100 Mbps	Fiber	2000 meters	Point-to-Point	---	Fiber	
Gigabit Ethernet	1000 Mbps	Fiber or 1000Base-T	Uses Fibre Channel or EIA568 CAT5	Point-to-Point	+/- 1.0v	Fiber or EIA568 STP	
ATM	155 Mbps	N/A	Not the Physical Layer	Point-to-Point	N/A	Fiber or STP	
SONET	9953.28Mbps	Fiber	STS-3 is 155.52Mbps	Point-to-Point	Optical	Fiber	
Fibre Channel	1 Gbps	Differential	SCSI like, Fiber, Coax, or TP	Point-to-Point	ECL	Yes	Yes
FDDI	100 Mbps	Fiber	CDDI uses copper	Token Ring	ECL/PECL	Fiber or Copper	
HIPPI	100 Mbps	Fiber	Fiber or Copper	Point-to-Point	Diff ECL	Fiber or Copper	
HSSI	52 Mbps	Balanced	SCSI II like	Point-to-Point	Diff ECL	------	STP

Bus Comparison (2)

Bus	Data Rate	Type	Description	Topology	Voltage	Coax	Twisted Pair
InfiniBand	2.5 Gbps	Balanced	Differential LVDS Pairs	Point-to-Point	LVDS	Copper or Fiber	
HyperTransport	800Mbps/bit pair	Balanced	2/4/8/16/32 bits	Daisy-Chained	LVDS	PWB	
FireWire, 1394a	400 Mbps	Differential	USB like, Back Plane or cable	Point-to-Point	0.6~0.8V	2 pairs of STP & 2 Power	
FireWire, 1394b	800 Mbps	Differential	"...." 1394b	Point-to-Point	0.6~0.8V	2 pairs of STP & 2 Power	
USB	12 Mbps	Differential	USB 1.1	Star Topology	0.3~3.6V	------	STP
USB	480 Mbps	Differential	USB 2.0	Star Topology	0.3~3.6V	------	STP
PC104	8MHz	8/16 Bit	ISA-AT Stacked PC Cards	Back Plane	TTL	Embedded Computers	
PC104-Plus	8MHz and 33MHz	8/16/32 Bit	PCI - PC104 Combo	Back Plane	TTL	Embedded Computers	
Compact-PCI	266/512Mbps	32/64 Bit	33MHz/66MHz, VME format	Back Plane	CMOS	110 pin 2mm connector	
PXI	33MHz	32/64 Bit	cPCI for Instrumentation 3U/6U	Back Plane	TTL	Industrial Computers	
AdvancedTCA	TBD	TBD	8U card size	Back Plane	TBD	TBD	
VME	40 Mbps	8/16/32 Bit	Euro card format 3U/6U x160mm	Back Plane	TTL	96 pin P1/P2	
VME64	80 Mbps	8/16/32/64 Bit	3U/6U x160mm, 6U/9U x320mm,	Back Plane	TTL	190 pin P1/P2, 92 pin P0	
VME64x	160 Mbps	8/16/32/64 Bit	2eVME; 3U/6U/9U x160mm (x320mm)	Back Plane	TTL/ETL	190 pin P1/P2, 92 pin P0	
VME320	320 Mbps	8/16/32/64 Bit	2eSST; 3U/6U/9U	Back Plane	ABTL	Copy Right-ed	
VXI	80 Mbps	64 Bit	VME for Instrumentation 3U/6U/9U	Back Plane	TTL	96 pin P1/P2	
Mezzanine	33/64MHz	8/16/32 Bit	PMC and PC MIP cards	Daughter card	PCI	Daughter Bus	

Connectors

- Signal
  - General purpose: BNC, NIM/Lemo, DB-9/25, RJ-45, USB (type-A & B), GPIB
  - RF: F-conn, SMA, SMB, N-type, MCX
- Power
  - DC: Molex, Amphernol, Bendix, banana plug
  - AC: 120V/240V (single/triple phase)
- High Voltage (red cable)
  - MHV, SHV