Pin assignments for D-sub, Centronics, and IEEE 1284C connectors.

Signal Name	Register bit	Signal Pin			Ground Return Pin		
		D-sub (IEEE 1284-A)	Centron-ics (IEEE 1284-B)	IEEE 1284-C	D-sub (IEEE 1284-A)	Centron-ics (IEEE 1284-B)	IEEE 1284-C
Data bit 0	*D0*	2	2	6	19	20	24
Data bit 1	*D1*	3	3	7	19	21	25
Data bit 2	*D2*	4	4	8	20	22	26
Data bit 3	*D3*	5	5	9	20	23	27
Data bit 4	*D4*	6	6	10	21	24	28
Data bit 5	*D5*	7	7	11	21	25	29
Data bit 6	*D6*	8	8	12	22	26	30
Data bit 7	*D7*	9	9	13	22	27	31
nError (nFault)	*S3*	15	32	4	23	29	22
Select	*S4*	13	13	2	24	28	20
PaperEnd	*S5*	12	12	5	24	28	23
nAck	*S6*	10	10	3	24	28	21
Busy	$\overline{S7}$	11	11	1	23	29	19
nStrobe	$\overline{C0}$	1	1	15	18	19	33
nAutoLF	$\overline{C1}$	14	14	17	25	30	35
nInit	*C2*	16	31	14	25	30	32
nSelectIn	$\overline{C3}$	17	36	16	25	30	34
HostLogicHigh				18			18
PeriphLogicHigh				36			36

This table is excerpted from *Parallel Port Complete* by Jan Axelson (jaxelson@lvr.com), published by Lakeview Research (http://www.lvr.com)