

EFC-3203 1.3 GHz

EFC-3208 100 MHz

MULTIFUNCTION COUNTER

OPERATOR'S MANUAL

Escort

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Section I

INTRODUCTION

The 1.3GHz Frequency Counter is a highquality, lightweight counter capable of frequency measurements from 5 Hz to 1.3 GHz. And model 100 MHz is capable of frequency measurements from 5 Hz to 100 MHz. The 1.3 GHz Frequency Counter features a special 50 Ω -terminated input for use in high frequency VHF/UHF/microwave/cellular telephone systems, as well as a standard 1 M Ω input for frequency measurements to 100 MHz.

The counters utilize an eight-digit display which provides up to 10 Hz resolution to 1.3 GHz (1.3 GHz only). 1 Hz resolution to 100 MHz, and 0.1 Hz to 10 MHz (100 MHz only).

In period mode, the unit measures the period required (in microseconds) for one cycle, over the range of 5 Hz to 3.5 MHz. At low frequencies, much greater accuracy can be achieved by period measurement than by frequency measurement.

Totalize mode permits counting of individual events. The counting process can be gated, either manually by a front panel switch, or by a gating signal applied to a rear panel jack, for more exact electronic control.

Operating mode and one of four decades of resolution are selected by front panel pushbutton switches. Easy-to-interpret readouts are provided by large bright digits, automatic decimal

point placement, leading zero blanking, and LED display of proper measurement units. Overrange and GATE function (indication of a measurement in progress) are also shown on front panel indicators.

A front panel HOLD switch is provided which "freezes" the display at the present reading, as well as a RESET button which clears the counter display and initiates a new measurement when released.

A selectable $\times 10$ attenuator and selectable 100 kHz low-pass filter are incorporated at the standard frequency input jack, for lessened susceptibility to noise and (in low frequency measurements) undesirable high frequency components.

The 10 MHz time base is generated by a crystal controlled oscillator for good stability with regard to temperature (± 10 ppm, 0°C to 40°C) and Line voltage variation (± 1 ppm for 10% variation) in standard version. For optional of high stability time base, temperature-compensated crystal oscillator (TCXO) for exceptional stability with regard to temperature (± 1 ppm, 0°C to 40°C) and line voltage variation (0.1 ppm for $\pm 10\%$ variation).

Other features include universal ac capability, a multi-position carrying handle/tilt stand for portability, and internal RF shielding.

INTRODUCTION

The exceptional accuracy, sensitivity, and range of these counters make them extremely valuable instruments for the scientist, engineer, and communications technician.

Section II

SAFETY SUMMARY

- Read this manual carefully to ensure your personal safety and to prevent damage either to the instrument or to equipment connected to it.
- Always operate from a power source that does not apply more than 250 Vrms between protective ground connection, through the grounding conductor in the power cord, is essential for safe operation.
- To avoid electric shock, plug the power cord into a properly wired receptacle where earth ground had been verified by a qualified service person. Due to this unit is grounded through the power cord, do this before making any connections to the input terminals of the meters.
- Make sure that the power cord and the fuse are in good condition before use. When servicing, use only the power cord and fuse specified for the counters.
- To avoid personal injury, never operate the instrument without the panels or covers.
- Do not work alone. Trained person should be nearby to render aid if necessary.

Section III

CONTROLS AND INDICATORS

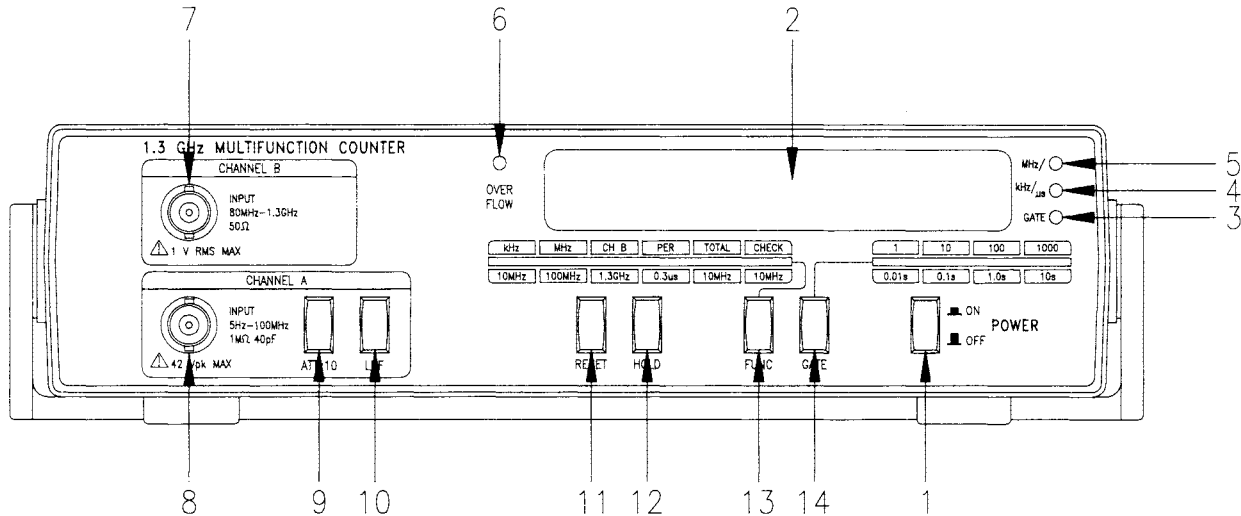


Figure 1-1. Front Panel (1.3 GHz)

CONTROLS AND INDICATORS

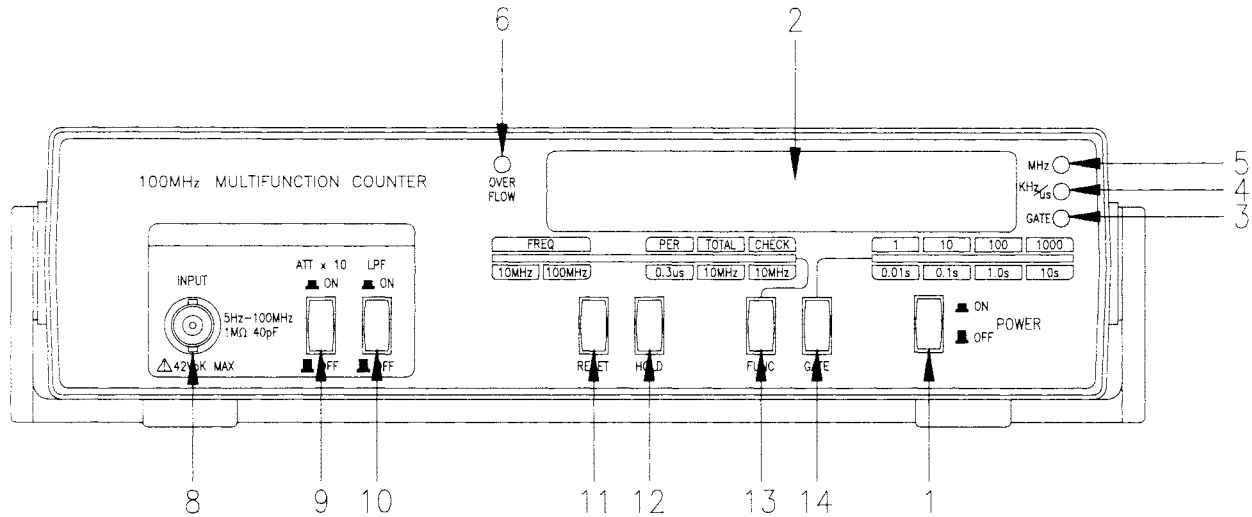


Figure 1-2. Front Panel (100 MHz)

CONTROLS AND INDICATORS

FRONT PANEL. Refer to Fig. 1-1, 1-2.

1. **POWER Switch.** Turns the unit on and off.
2. **Display.** Eight-digit display used for all readings.
3. **GATE Indicator.** Lights whenever a measurement is being taken.
4. **kHz/ μ s Indicator.** In kHz Frequency or CHECK mode, indicates that the frequency displayed is in kilohertz. In PERiod mode indicates that the period displayed is in microseconds. Not used in TOTALize mode.
5. **MHz Indicator.** In MHz Frequency or CH B (PRESCALE) mode, indicates that the frequency displayed is in megahertz. Not used in TOTALize mode.
6. **OVERFLOW Indicator.** Lights whenever the range of the display is exceeded. One or more most significant digits are not displayed.
7. **Channel B Input Jack.** Female BNC connector terminated in a 50 ohm input resistance (1.3 GHz only).
8. **Channel A Input Jack.** Female BNC connector terminated in a 1 megohm input resistance, shunted by ≤ 40 pF capacitance.
9. **x10 Attenuator Switch.** When this switch is pushed in, the Channel A input is attenuated 10:1 before application to the counter. With the switch released (out), the signal is applied unattenuated.
10. **LPF (Low-Pass Filter) Switch.** With this switch pushed in, the Channel A input is routed through a low-pass filter with a -3 dB point of approximately 100 kHz. When it is released (out), the input is applied directly.
11. **RESET Switch.** In all modes, pushing this momentary switch resets the counter to zero. When it is released, the measurement starts again.
12. **HOLD Switch.** Functions as follows:
 - a. All modes except TOTALize: Setting this switch to on "freezes" the display at the existing reading and resets the counter. Releasing the switch starts a new measurement; the display is updated when this measurement is completed.
 - b. TOTALize mode: Setting the switch to on "freezes" the display at the existing reading and halts the totalizing process. When the switch is released, counting resumes, provided that the gating signal at the rear panel **TOTALIZE START/STOP INPUT** jack (18) is high (or jack is open).
13. **FUNCTION Switch.** Pushing this momentary switch selects the six counter operating modes and lights the corre-

CONTROLS AND INDICATORS

sponding mode indicators as follows:

- a. **kHz Frequency Mode Indicator.** When selected, the unit measures the frequency of the signal at the **Channel A Input** (8). Readings are in kHz as indicated by the **kHz/ μ s** indicator (4). Resolution is selected by the **GATE** switch (14). This mode is automatically selected when the counter is powered ON.

Note:

Guaranteed frequency measurement range in kHz Frequency mode is 5 Hz to 10 MHz (above 10 MHz, display may show zero with no OVERFLOW indication); sine wave sensitivity: 20 mV rms, 5 Hz to 10 MHz.

- b. **MHz Frequency Mode Indicator.** When selected, the unit measures the frequency of the signal at the **Channel A Input** (8). Readings are in MHz as indicated by the **MHz** indicator (5). Resolution is selected by the **GATE** switch (14).

Note:

Guaranteed frequency measurement range in the MHz frequency mode is 5 Hz to 100 MHz.

- c. **CH B (PRESCALE) Frequency Mode Indicator.** When selected, the unit measures the frequency of the signal

at the **Channel B Input** (7). Readings are in MHz as indicated by the MHz indicator (5). Resolution is selected by the **GATE** switch (14). (1.3 GHz only)

- d. **PERiod Mode Indicator.** When selected, the unit measures the period of the signal at the Channel A input. Readings are in μ s as indicated by the **kHz/ μ s** indicator (4). Cycles Averaged; 1, 10, 100, or 1000 are selected by the **GATE** switch (14).

- e. **TOTALize A Mode indicator.** When selected, the unit counts cycles of the Channel A input and continuously displays that count. Totalization can be controlled by a gate signal at the rear panel **TOTALIZE START/STOP** jack (18).

- f. **CHECK Mode Indicator.** When selected, the unit displays the frequency of the internal time base, providing a general check of performance.

14. **GATE Switch.** Pushing this momentary switch selects the degree of display resolution in all modes except TOTALize as follows;

- a. **1/0.01s Indicator.** When selected, the unit measures kHz or MHz Frequency with a 0.01s Gate Time, CH B Frequency with a 1 Gate Time, and PERiod for one cycle between display updates. This Gate Time is automatically selected when the unit is powered on.
- b. **10/0.1s Indicator.** When selected, the unit measures

CONTROLS AND INDICATORS

kHz or MHz Frequency with a 0.1s Gate Time, CH B Frequency with a 10 Gate Time, and PERiod for 10 cycles averaging between display updates.

c. **100/1.0s Indicator.** When selected, the unit measures kHz or MHz Frequency with a 1.0s Gate Time, CH B Frequency with a 100 Gate Time, and PERiod for 100 cycles averaging between display updates.

d. **1000/10s Indicator.** When selected, the unit measures kHz or MHz Frequency with a 10s Gate Time, CH B Frequency with a 1000s Gate Time, and PERiod for 1000 cycles averaging between display updates.

Remark

For 1.3 GHz counter, Gate switch selections of 1/10/100/1000 are 25.6ms/256ms/2.56s/25.63 (crystal version) and 32ms/320ms/3.2s/32s (TXCO version)

Note:

Measuring the PERiod of low frequencies such as 10 Hz with 100 or 1000 cycles averaging will result in extremely long display update times.

CONTROLS AND INDICATORS

REAR PANEL. Refer to Fig. 2-1, 2-2, 2-3.

15. **Fuseholder.**

16. **Line Cord Receptacle.**

17. **LINE VOLTAGE SELECT Indicator.** Settings allow Universal Power Operation: 100/120/220/240 VAC, 50/60 Hz.

18. **TOTALIZE START/STOP Input Jack.** Input jack used to control the totalization function, if desired. Unit stops totalizing whenever the signal applied at this jack goes to a TTL low level (or is connected to chassis ground).

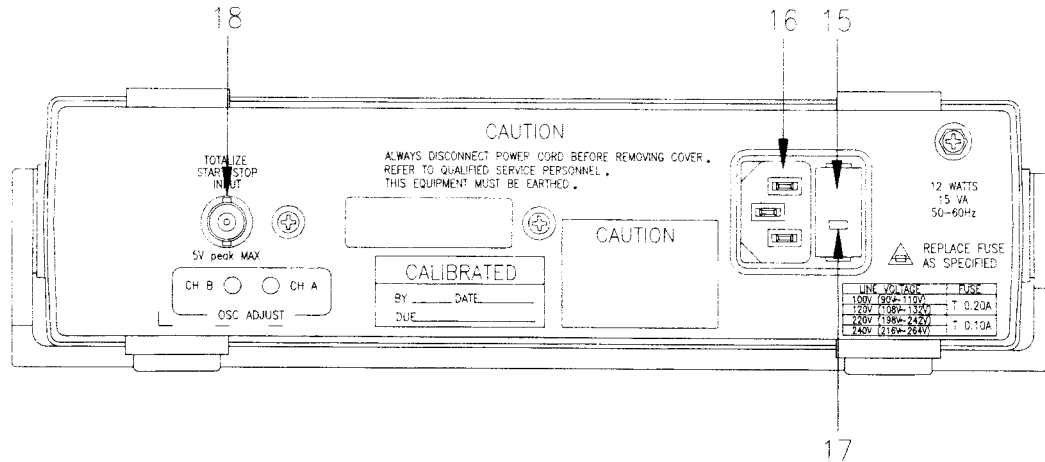


Figure 2-1 Rear Panel (1.3 GHz/crystal version)

CONTROLS AND INDICATORS

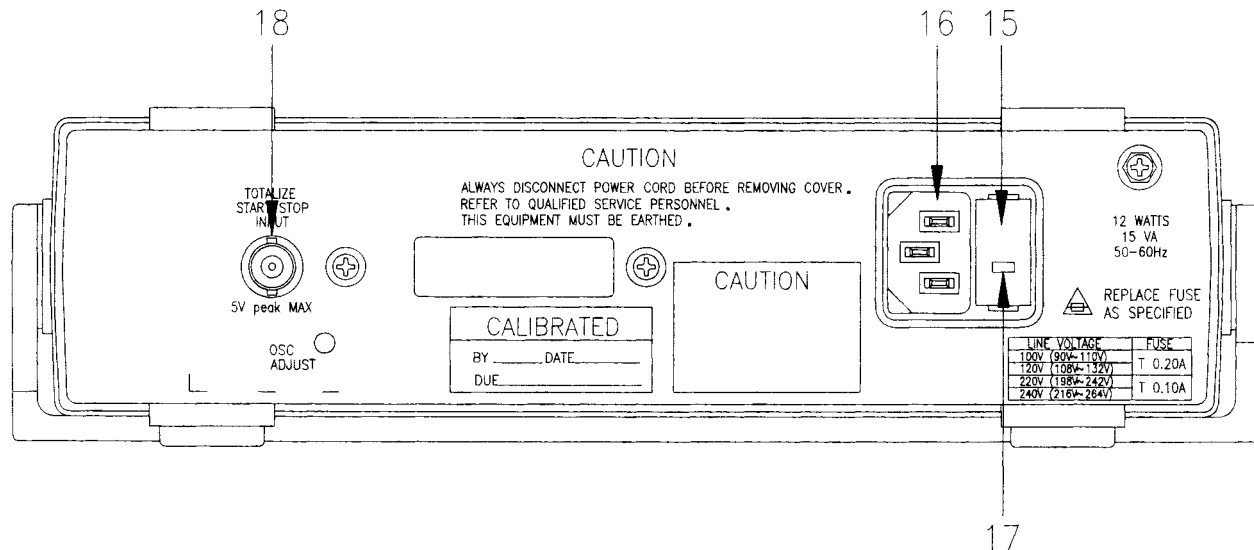


Figure 2-2 Rear Panel (100 MHz/crystal version)

CONTROLS AND INDICATORS

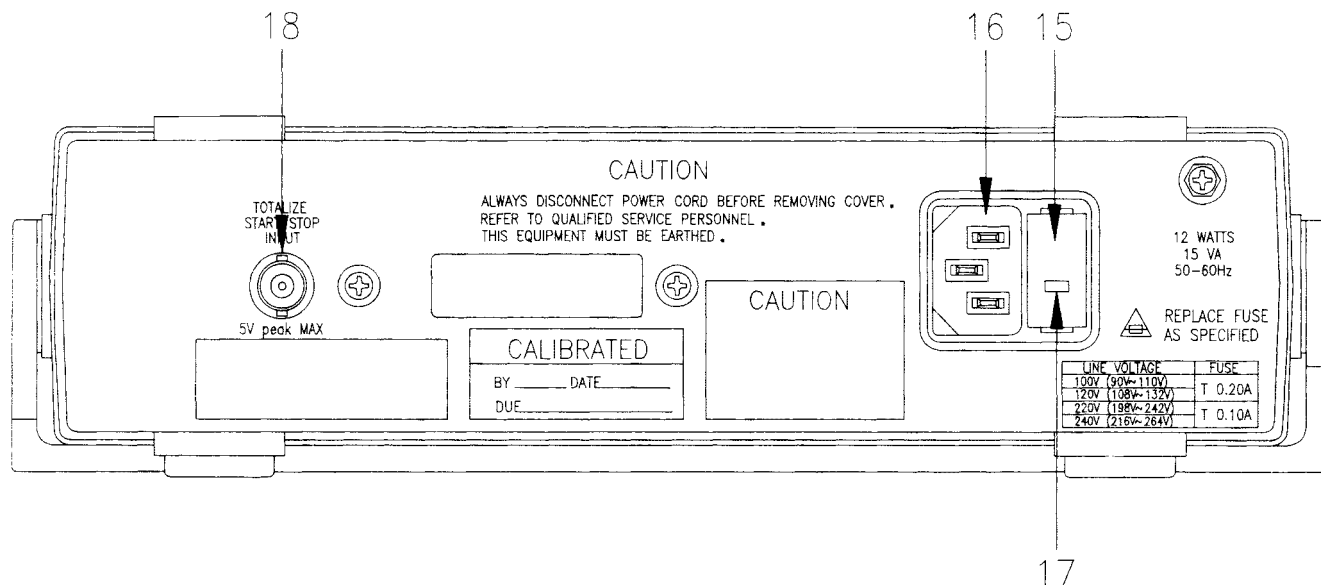


Figure 2-3. Rear Panel (100MHz, 1.3GHz/TCXO version)

Section IV

SPECIFICATIONS

FUNCTIONS

Frequency.	Period Average.
1.3 GHz Frequency	Totalize.
Prescaler. (1.3 GHz only)	Check (Self Test).
100 MHz Frequency	
Period.	

Accuracy:

\pm Time base accuracy,
 \pm 1 count.

Resolution:

0.1 Hz to 100 Hz, kHz
mode.

Channel A:

1 Hz to 1000 Hz, MHz
mode.

Channel B:
(PRESCALE)

10 Hz to 10 kHz.

(1.3 GHz only)

Display:

Input signal frequency with
decimal point positioned by
GATE switch.

Units of measurement (kHz,
MHz) indicated on front
panel by LED indicators and
selected by front panel
switches.

Number of Digits Displayed See Tables 1 and 2.

FEATURES

8 Digits, 0.56".	2-Position Attenuator.
Low Pass Filter.	Remote Stop-Start.
Display Hold.	

FREQUENCY CHARACTERISTICS

Rege:	5 Hz to 10 MHz sinewave, kHz mode.
Channel A:	5 Hz to 100 MHz sinewave, MHz mode.
Channel B: (1.3 GHz only) (PRESCALE)	80 MHz to 1.3 GHz (1300 MHz) sinewave.

SPECIFICATIONS

	Number Of Significant Digits Displayed							
Gate Time	10 SEC		1 SEC		0.1 SEC		0.01SEC	
Resolution	.1 Hz	1 Hz	1 Hz	10 Hz	10 Hz	100 Hz	100 Hz	1000 Hz
Function Typical Frequency	kHz	MHz	kHz	MHz	kHz	MHz	kHz	MHz
100 MHz	—	8*	—	8	—	7	—	6
10 MHz	8*	8	8	7	7	6	6	5
1 MHz	8	7	7	6	6	5	5	4
100 kHz	7	6	6	5	5	4	4	3
10 kHz	6	5	5	4	4	3	3	2
1 kHz	5	4	4	3	3	2	2	1
100 Hz	4	3	3	2	2	1	1	—
10 Hz	3	2	2	1	1	—	—	—
5 Hz	2	1	1	—	—	—	—	—

* = Overflow

**Table 1. Number of Significant Digits Displayed for Typical Frequencies
for Channel A Input and kHz or MHz Frequency Modes.**

SPECIFICATIONS

	Number Of Significant Digits Displayed			
Gate Time	25.6/32 SEC	2.56/3.2 SEC	0.256/0.32 SEC	0.0256/0.032 SEC
Resolution Typical Frequency	10 Hz	100 Hz	1 kHz	10 kHz
80 MHz	7	6	5	4
150 MHz	8	7	6	5
520 MHz	8	7	6	5
1.3 GHz	8*	8	7	6

* = Overflow

Table 2. Number of Significant Digits Displayed for Typical Frequencies for Channel B (PRESCALE) (1.3 GHz only)

PERIOD CHARACTERISTICS

Range: 0.285 μ s to 200,000 μ s.

Frequency Range: 5 Hz to 3.5 MHz sine wave.

Accuracy: ± 1 count \pm time base error \pm trigger error*

Resolution: 100 ps to 100 ns, switch selectable in four decade steps.

Display: μ s with decimal point.

Minimum Pulse

Width: 250 ns.

Number of Digits

Displayed: See Table 3.

*Note: Trigger error is typically $\pm 0.3\%$ of reading divided by the number of cycles averaged, for input signals having better than 40 dB S/N ratio and greater than 100 mV amplitude.

SPECIFICATIONS

		Number Of Significant Digits Displayed			
	Gate (CHA)	0.01s	0.1s	1.0s	10s
	Resolution	0.1 μ s	0.01 μ s	0.001 μ s	0.0001 μ s
Typical Period	Corresponding Frequency	(1 Period Average)	(10 Period Average)	(100 Period Average)	(1000 Period Average)
0.285 μ s	3.5 MHz	1	2	3	4
1.0 μ s	1 MHz	2	3	4	5
10 μ s	100 kHz	3	4	5	6
100 μ s	10 kHz	4	5	6	7
1000 μ s	1 kHz	5	6	7	8
10,000 μ s	100 Hz	6	7	8	8*
100,000 μ s	10 Hz	7	8	8*	8*
200,000 μ s	5 MHz	7	8	8*	8*

* = Overflow

Table 3. Number of Significant Digits Displayed for Typical Periods.

TOTALIZE CHARACTERISTICS

Range: 5 Hz to 10 MHz sine wave.

Capacity: 0 to 99,999,999 plus overflow LED.

Control:

Manual reset and hold from the front panel. Normally enabled, except when signal at back panel START/STOP jack is low.

SPECIFICATIONS

CHANNEL A INPUT CHARACTERISTICS (5 Hz to 100 MHz input)

Impedance:	1 M Ω resistance, shunted by 40 pF capacitance.
Connector:	BNC on front panel.
Coupling:	AC.
Sinewave	20 mV rms, 5 Hz to 30 MHz.
Sensitivity:	50 mV rms, 30 MHz to 100 MHz.
Maximum Input:	See Fig. 3.
Attenuator:	x1/x10, switch selectable.
Filter:	Low pass filter, — 3 dB point of 100 kHz, switch selectable.

PRESCALE INPUT CHARACTERISTICS (80 MHz to 1.3 GHz input) (1.3 GHz only)

Impedance:	50 ohms.
Connector:	BNC on front panel.
Coupling:	AC.

Sinewave	10 mV rms, 80 MHz to 600 MHz.
Sensitivity:	25 mV rms, 600 MHz to 1.0 GHz. 50 mV rms, 1.0 GHz to 1.3 GHz.
Maximum Input:	1 V rms.

TOTALIZE START/STOP INPUT

Logic Levels:	Standard TTL levels; low level inhibits totalizing, high level enables it.
Loading:	One standard TTL gate.
Maximum Input:	5V DC peak.

TIME BASE CHARACTERISTICS (STANDARD):

Type:	crystal-controlled oscillator
Frequency:	10 MHz.
Stability:	less than ± 10 ppm (0 °C to 40 °C) less than ± 1 ppm (line voltage $\pm 10\%$)
Maximum Aging Rate:	± 1 ppm/yr.

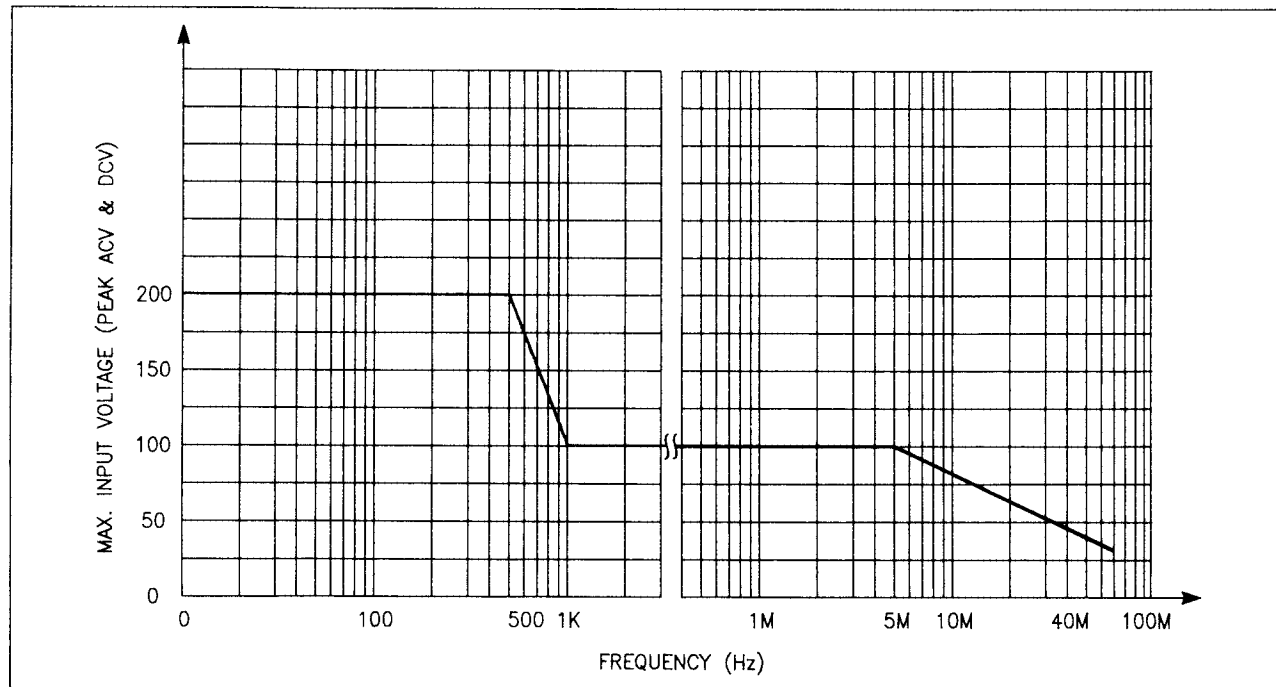


Figure 3 Maximum Input Protection Derating Curve.

(Channel A Input)

SPECIFICATIONS

TIME BASE CHARACTERISTICS

Type:	TCXO (temperature compensated crystal oscillator).
Frequency:	10 MHz.
Line Voltage Stability:	≤ 0.1 ppm with $\pm 10\%$ with line voltage variation.
Temperature Stability:	$\leq 0.0001\%$ (± 1 ppm from 0°C to 40°C ambient).
Maximum Aging Rate:	± 1 ppm/year.

DISPLAY CHARACTERISTICS

Visual Display:	Eight 0.56" seven-segment digits with kHz, MHz, μs , GATE, and OVERFLOW LED indicators.
OVERFLOW Indication:	LED indicator lights when count exceeds 99,999,999 during any selected gate time.
Display Update Time:	1. KHz and MHz FREQUENCY Mode: User

selected gate time plus fixed 200 ms interval.

2. Pre-scale Mode: User selected gate time plus fixed 640 ms interval.
3. PERiod Mode: User selected cycles averaging plus fixed 200 ms interval.
4. TOTALize Mode: Continuous.

Resolution:

Selectable in four steps as follows:

GATE		kHz	MHz	
Time:	Period	Frequency	Frequency	Prescale
0.01s	0.1 μs	100Hz	1000Hz	10kHz
0.1s	0.01 μs	10Hz	100Hz	1kHz
1.0s	0.001 μs	1Hz	10Hz	100Hz
10s	0.0001 μs	0.1Hz	1Hz	10Hz

RESET and HOLD Switches

RESET:

Resets the display to zero.

HOLD:

In FREQUENCY and PERi-

SPECIFICATIONS

od modes, measurement in progress is stopped, and the last complete measurement is displayed. When HOLD is released, a new measurement begins. In TOTALize mode, counter is stopped but not reset, and the last count is displayed. When HOLD is released, count continues from where the counter stopped.

GENERAL

Power Requirements:	100/120/220/240 VAC ($\pm 10\%$), 50/60 Hz; 12 W.
Dimensions (HxWxD):	71 x 261 x 211 mm (2.8 x 10.3 x 8.3")
Weight:	1.8 kg (3.96 lbs).
Temperature and Humidity:	
Operation:	0 °C to + 40 °C \leq 80% R.H.
Storage:	- 20 °C to + 60 °C \leq 70% R.H.

Standard Accessories:

Operator's manual, power cord.

Optional Accessories:

EB-10: 3 feet, 50 Ω BNC to BNC coaxial cables
EB-11: 3 feet, 50 Ω BNC to alligator clip coaxial cables
EB-32: Carrying case

Section V

PREPARATION FOR USE

Line Voltage Selection

This product is intended to operate from a power source that does not supply more than 250 Vrms between the supply conductors or between either supply conductor and ground. Before connecting the power cord to a power-input source, verify that the line voltage indicator on the rear panel is corrected (see Figure 2-1, 2-2, 2-3).

Grounding the Equipment

A protective ground connection, the third wire in the power cord, is necessary for safe operation. To avoid electrical shock, plug the power cord into a properly wired receptacle before making any connections to the equipment input terminals. Do not remove the ground lug from the power cord for any reason. Use only the power cord and connector specified for this equipment.

Fuses

To avoid fire hazard, use only a fuse of the specified type, voltage rating and current rating for this equipment. See Controls, Connectors, and Indicators in Section III.

Section VI

OPERATING INSTRUCTIONS

PRELIMINARY

Numbers in parentheses refer to items in "CONTROLS AND INDICATORS" section and Fig 1-1, 1-2, 2-1, 2-2 and 2-3.

1. Connect the unit to ac power.
2. Set the POWER switch (1) to on (pushed in).

CAUTION

1. *Application of input voltages higher than the limits listed in the "SPECIFICATIONS" section may damage the counter. Before applying any signal to the inputs, make certain that it does not exceed these specified maximums.*
2. *Engaging the x10 Attenuator switch (9) does not alter these upper limits.*
3. *Counter ground points are connected to earth ground through the counter's ac power cord. Always connect counter (probe) ground only to ground points or isolated points in the circuit under test.*

FREQUENCY MEASUREMENTS

Using Channel A Input (5 Hz to 100 MHz)

1. Apply the signal to be measured to the Channel A input jack (8).
2. Select measurement units of kHz Frequency with the FUNCTION switch (13). The kHz/ μ s or MHz indicator (4,5) lights accordingly.

Note:

In kHz mode, maximum guaranteed frequency is 10 MHz. Maximum frequency in MHz mode is 100 MHz. Exceeding these ranges may produce unpredictable results, such as a display of zero, with no OVERFLOW indication.

3. Select the degree of resolution desired, using the GATE switch (14). The actual Gate Times of 0.01s, 0.1s, 1.0s, and 10s are given by the CH A labels below the LED indicators.
4. Frequency is given by the display (2). The GATE indicator (3) lights while each measurement is in progress, and the

OPERATING INSTRUCTIONS

display is updated at the end of each measurement interval (when GATE goes off).

Note:

Some measurement delay and display instability may be encountered; see "Display Interpretation".

5. The OVERFLOW indicator (6) lights whenever the range of the display is exceeded.
6. If necessary, engage the x10 Attenuator switch (9). When set to x10 (pushed in), this switch attenuates the Channel A signal by a factor of approximately 10 before application to the counter. This helps prevent mis-counting caused by noisy or improperly terminated high-amplitude signals.
7. If necessary, engage the LPF (Low-Pass Filter) switch (10). This routes the Channel A input through a low-pass filter (- 3 dB frequency of approximately 100 kHz) before application to the counter. This helps eliminate counting errors in low frequency measurements by minimizing effects of high-frequency noise present on the input.
8. Engaging the HOLD switch (12) during frequency measurements causes the display to "freeze" at the existing reading. When HOLD is released, a new measurement begins, but the display continues to hold the old reading

until the new measurement is completed.

9. Pushing RESET (11) in frequency measurements resets the display to zero. When the button is released, a new measurement begins, but the display remains at zero until the new measurement is completed.

Using Channel B (PRESCALE) input (80 MHz - 1.3 GHz) (For 1.3 GHz only)

1. Apply the signal to be measured to the Channel B (PRESCALE) input jack (7).



CAUTION

The maximum input limit to this jack is 1.5V rms maximum over the input frequency range. The input impedance is 50 ohms.

2. Engage the CH B (PRESCALE) Frequency mode with the FUNCTION switch (13).
3. Select the degree of resolution desired, using the GATE switch (14). The actual Gate Times of 1, 10, 100 and 1000 are given by the CH B labels above the LED indicators.
4. Frequency is given by the display (2). The GATE indicator (3) lights while each measurement is in progress, and the display is updated at the end of each measurement interval (when GATE goes off).

OPERATING INSTRUCTIONS

Note:

Some measurement delay and display instability may be encountered; see "Display Interpretation".

5. The OVERFLOW indicator (6) lights whenever the range of the display exceeded.
6. Engaging the HOLD switch (12) during frequency measurements causes the display to "freeze" at the existing reading. When HOLD is released, a new measurement begins, but the display continues to hold the old reading until the new measurement completed.
7. Pushing RESET (11) in frequency measurements resets the display to zero. When the button is released, a new measurement begins, but the display remains at zero until the new measurement is completed.
8. The x10 Attenuator and LPF switches (9,10) have no effect in CH B (PRESCALE) Frequency mode.

PERIOD MEASUREMENTS

In period mode, the unit displays the period, or time required for one cycle of the input signal to occur. The actual measurement is made by averaging over 1, 10, 100, or 1000 cycles. Maximum frequency is 3.5 MHz.

1. Apply the signal to be measured to the Channel A input jack (8).
2. Engage the PERiod mode with the FUNCTION switch (13). The kHz/ μ s indicator (4) lights to indicate that readings are in microseconds.
3. Select the degree of resolution desired, using the GATE switch (14). (The GATE switch determines how many cycles are averaged in the measurement: 1, 10 100, or 1000, respectively, from left to right.)
4. Period is given by the display (2). The GATE indicator (3) lights while each measurement is in progress, and the display is updated at the end of each measurement interval (when GATE goes off). (At higher frequencies, the GATE indicator may flash too quickly to be seen).

Note:

Some measurement delay and display instability may be encountered; see "Display Interpretation".

5. The OVERFLOW indicator (6) lights whenever the range of the display is exceeded.
6. If necessary, engage the x10 Attenuator switch (9). When set to x10 (pushed in), this switch attenuates the Channel

OPERATING INSTRUCTIONS

A signal by a factor of approximately 10 before application to the counter. This helps prevent mis-counting caused by noisy or improperly terminated high-amplitude signals.

7. If necessary, engage the LPF (Low-pass Filter) switch (10). This routes the Channel A input through a low-pass filter (- 3 dB frequency of approximately 100 kHz) before application to the counter. This helps eliminate counting errors in low frequency measurements by minimizing effects of high-frequency noise present on the input.
8. Engaging the HOLD switch (12) during period measurements causes the display to "freeze" at the existing reading. When HOLD is released, a new measurement begins, but the display continues to hold the old reading until the new measurement is completed.
9. Pushing RESET (11) in period measurements resets the display to zero. When the button is released, a new measurement begins, but the display remains at zero until the new measurement completed.

TOTALIZE MEASUREMENTS

The TOTALize mode is used to count the total number of events occurring during a specific time period. This time period can be defined manually by front panel switch action, or for better accuracy, by a gating signal applied to the rear panel.

Because of capacitive coupling of the counter input, events should occur at least five times per second for accurate counting. Maximum frequency is 10 MHz.

1. Engage the TOTALize mode with the FUNCTION switch (13). Any GATE (14) setting is ignored.
2. If the counting is to be controlled electronically, connect the gating signal to the rear panel TOTALIZE START/STOP jack. A TTL high at this input enables the totalizing process; a TTL low disables it, holding the display at the accumulated value. If no signal is connected, the jack is pulled high internally so counting occurs.
3. Depress the RESET switch (11) to zero the counter. If no gating signal is connected to the TOTALIZE START/STOP jack, the unit starts counting as soon as the RESET switch is released. If a gating signal is connected, counting starts when RESET is released and the gating signal goes high.
4. As the unit totalizes, it displays the count continually. Maximum count is 99,999,999. If this is exceeded, the OVERFLOW indicator (6) lights, and the count continues.
5. Counting is halted by one of three methods:
 - a. If the gating signal at the TOTALIZE START/STOP jack goes low, counting stops and the display is held at the accumulated total. Counting resumes when the gating

OPERATING INSTRUCTIONS

- signal again goes high.
- b. If the HOLD switch (12) is engaged, counting stops and the display is held at the accumulated total. Counting resumes when the switch released.
 - c. Pressing RESET (11) at any time clears the counter and resets the display to zero.
6. If necessary, engage the x10 Attenuator switch (9). When set to x10 (pushed in), this switch attenuates the Channel A signal by a factor of approximately 10 before application to the counter. This helps prevent mis-counting caused by noisy or improperly terminated high-amplitude signals.
7. If necessary, engage the LPF (Low-Pass Filter) switch (10). This routes the Channel A input through a low-pass filter (– 3 dB frequency of approximately 100 kHz) before application to the counter. This helps eliminate counting errors in low frequency measurements by minimizing effects of high-frequency noise present on the input.

DISPLAY INTERPRETATION

Display Formats

Sample displays are given in Fig. 4. In Fig. 4, a value of 1234.567 is displayed, and the kHz/μs indicator is lit. This may represent either a frequency or a period reading; a glance at the mode switches indicates which is correct.

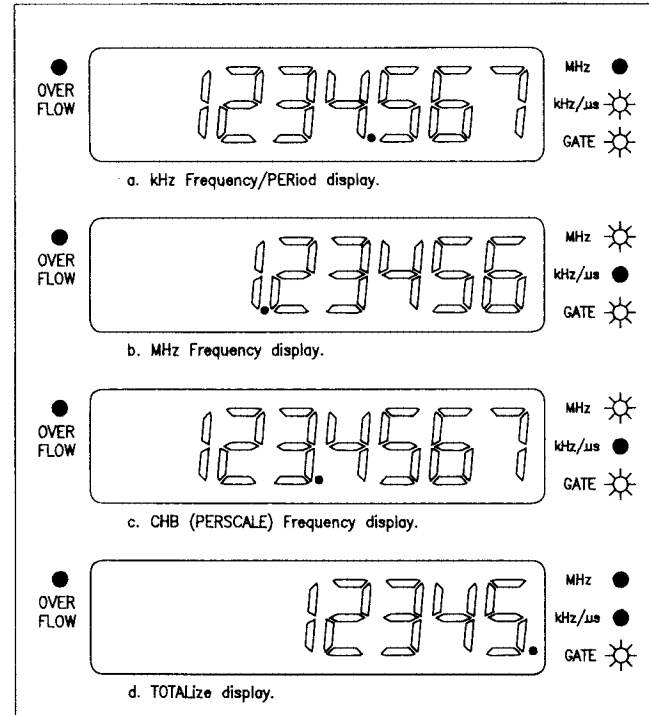


Figure 4. Samples of Various Displays.

OPERATING INSTRUCTIONS

Assuming that Fig. 4 represents a frequency reading, the resolution displayed is .001 kHz, or 1 Hz;. If the MHz Frequency mode is engaged with the FUNCtion switch, leaving all else unchanged, the display changes to that of Fig. 4. This is the same frequency as in Fig. 4, but given in megahertz. Note that the resolution is now .00001 MHz, or 10 Hz, even though a different Gate Time was not selected with the GATE switch. The display resolutions vary with the FUNCtion and GATE selections.

The frequency displays of Fig. 4 and b are obtained by engaging the 1.0s Gate Time with the GATE switch. A typical Channel B (PRESCALE) (1.3 GHz only) reading using this same Gate Time setting is shown in Fig. 4. Note that the resolution is now .0001 MHz, or 100 Hz.

Fig. 4 gives a typical totalize display. Totalizations have no units, and are always integers (no digits to right of decimal point). At higher totalizing frequencies, the least significant display digits tend to fade due to their rapid rate of change.

Display Instability

An uncertainty of ± 1 least significant digit is inherent in all digital measurements. However, greater display uncertainties can result from other factors, as follows:

Noise or ringing on the input can cause false triggering. In some cases the display may be unstable, whereas in others it may appear stable but at an incorrect reading. For Channel A measurements, this type of error can be reduced by using the attenuator and filter. Similar errors introduced by standing waves may be avoided by using proper terminations and cable lengths when appropriate. The Channel B (PRESCALE) (1.3 GHz) input jack is provided with an internal 50 Ω termination, to avoid standing wave difficulties for measurements in 50 Ω systems.

Uncertainty may be introduced by instability of the input frequency. This is common with LC oscillators; crystal-controlled oscillators are much more stable.

In period measurements, uncertainty is introduced by trigger error (see "SPECIFICATIONS"). This uncertainty can be reduced by taking the measurement over a greater number of cycles.

Period and frequency are reciprocals of each other. At low frequencies, more digits can be obtained (lessening the effects of instability) using period mode. Similarly, high frequency accuracy is enhanced by using frequency mode. The "crossover" point between the two modes is 10 kHz.

Measurement Delays

In all measurements (except totalize), the display is updated at the end of a finite measurement interval. The GATE indicator lights during this interval, which varies in length according to operating mode and resolution selected. For some conditions, the delay can become significant. This should be kept in mind when changing resolution or operating mode, or when using HOLD or RESET, because each of these actions initiates a new measurement. Measurement delays for each mode are discussed here.

Frequency

In frequency measurements, each GATE setting establishes a set time during which the measurement is made and results in a different display resolution. Gate Times settings for kHz, MHz, and CH B (PRESCALE) (1.3 GHz). Frequency modes and their resulting display resolutions are as follows:

FUNCTION mode	GATE Time setting	Display Resolution
kHz	0.01s	100 Hz
kHz	0.1s	10 Hz
kHz	1.0s	1 Hz
kHz	10s	0.1 Hz
MHz	0.01s	1 kHz
MHz	0.1s	100 Hz
MHz	1.0s	10 Hz
MHz	10s	1 Hz
CH B	0.032s	10 kHz
CH B	0.32s	1 kHz
CH B	3.2s	100 kHz
CH B	32s	10 Hz

Table 4. Gate time and measurement resolution in Frequency mode.

OPERATING INSTRUCTIONS

As observed in the table, smaller GATE Times result in lower resolutions. They are useful when quicker updates are desired, for example, while tuning an oscillator. Better resolutions require longer update intervals.

Period

Period measurements are made by averaging over a set number of cycles. That number is determined by the GATE switch as follows:

GATE setting	Number of cycles averaged
1/0.01s	1
10/0.1s	10
100/1.0s	100
1000/10s	1000

Note: Gate selections of 1/10/100/1000 for model (1.3 GHz) only.

The time required for a period measurement to be completed can be found by the formula:

$$\text{Time} = \left(\begin{array}{c} \text{Number of} \\ \text{cycles} \\ \text{averaged} \end{array} \right) \times \left(\begin{array}{c} \text{Average} \\ \text{cycle} \\ \text{length} \end{array} \right)$$

where time units are same (seconds, milliseconds, etc.) on both sides.

For a constant input frequency this is:

$$\text{Time} = \frac{\text{Number of cycles averaged}}{\text{Input frequency (Hz)}}$$

Note that two GATE switch settings select 100 and 1000 cycle averaging. Because of this, significant delays may occur between display updates at low frequencies.

Inter-Measurement Interval

The inter-measurement interval is fixed at 200 milliseconds in all modes except CH B (PRESCALE) (1.3 GHz) and TOTALize. In CH B (1.3 GHz) mode it is 640 ms, and in TOTALize, counting is continuous.

This fixed interval is independent of gate time, number of cycles, or input frequency.

GENERAL CONSIDERATIONS

Use of Attenuator Probes

Channel A input resistance (1 M Ω) and input capacitance (40 pF max) are independent of the x10 Attenuator switch. To decrease loading, a high-impedance oscilloscope probe may be used with Channel A.

Note:

When using a 10:1 probe make certain that the signal amplitude is large enough to provide at least the minimum required signal to the counter after probe attenuation (see "Channel A Sensitivity" in "SPECIFICATIONS").

Note:

Do not use a 10:1 probe with the CH B (PRESCALE) (1.3 GHz) input. The probe is designed for 10:1 attenuation with a counter input resistance of $1\text{ M}\Omega$. The $50\ \Omega$ termination of the CH B jack would result in unacceptably high (180,001/1) attenuation.

Cable Considerations

Accuracy of radio frequency measurements can be affected by connections between signal source and counter. Main considerations are standing waves and shunt cable capacitance.

Standing waves are usually present due to reflections when a transmission line is not terminated in its characteristic impedance. These standing waves may cause damage to the signal source or produce inaccurate measurements, and their effects increase as cable length reaches one-fourth of the wave-

length for the frequency being measured.

Standing waves can be minimized by keeping cable lengths short, and, more importantly, providing a proper termination. The cable's characteristic impedance and the terminating impedance should match the source impedance. For example, for a source impedance of 50 ohms, use 50 ohm coaxial cable terminated with a 50 ohm resistive load. Use a dc blocking capacitor in situations where bias voltage or other dc voltages could be affected by the termination resistor.

Shunt cable capacitance, which can cause undesirable signal attenuation, increases with increased cable length. It is recommended that for radio frequency measurements, the cable be no longer than three feet (90 cm), to keep shunt capacitance within acceptable limits.

In $50\ \Omega$ systems the internal $50\ \Omega$ input termination of the CH B (PRESCALE) (1.3 GHz) jack minimizes reflections and the resulting standing waves. Thus, the need for an external termination is eliminated. Also, shunt capacitance has a much lesser effect at this jack than at the Channel A input, and the above restriction on cable length is reduced. However, CH B measurements must always be taken from a $50\ \Omega$ point in the circuit under test.

OPERATING INSTRUCTIONS

FUNCTION or GATE Time Changes

When switching gate times or function modes, note that such a change initiates a new measurement; the display is not updated until the new measurement is completed. Even though the decimal point and leading zeroes are adjusted immediately, appearance of the correct value may be significantly delayed depending on measurement interval (see "Display Interpretation - Measurement Delays").

Line Frequency Measurement

WARNING

Use caution in measuring the line frequency of an ac outlet. Using the probe tip only, measure both sides of the line. The ground side will give a zero reading and the hot side will provide the desired measurement. Do not use the "ground" lead of the probe. Remember that the chassis of the counter and the "ground" lead of the probe are already at earth ground (via the 3-wire power cord of the instrument). Touching the "ground" lead to the "hot" side of the line would place a direct short on the power line through the probe cable, resulting in possible

injury and damage to the probe cable.

Use of the attenuator, filter, and/or a x10 probe is advisable when measuring line frequency, because of the high amplitude signal, and because noise is usually present and can cause mis-counting.

CHECK (SELF TEST)

The CHECK mode provides a quick, general self test of instrument operation.

1. Engage the CHECK Mode with the FUNCTION switch (13). This connects the counter input internally to the time base oscillator.
2. Engage each GATE Time Mode with the GATE switch (14) and check that the results match the following:

GATE setting*	Ddisplay reads
0.01s	10000.0 kHz
0.1s	10000.00 kHz
1.0s	10000.000 kHz
10s	0000.0000 kHz, OVERFLOW lit

OPERATING INSTRUCTIONS

3. Pressing the HOLD switch (12) should hold the display value and keep the GATE indicator off for as long as the button is pushed in. When HOLD is disengaged, GATE should resume flashing. (If a new GATE Time has been selected, the display is updated to its proper value after the first GATE interval.
4. Pressing the RESET switch (11) should clear the display. The GATE indicator should stay off as long as RESET is pushed. Upon release of the button, GATE should resume flashing and the display should be updated at the end of the first GATE interval.

*GATE indicator lights during this interval; time between measurement is 200 ms.

Section VII

CIRCUIT DESCRIPTION

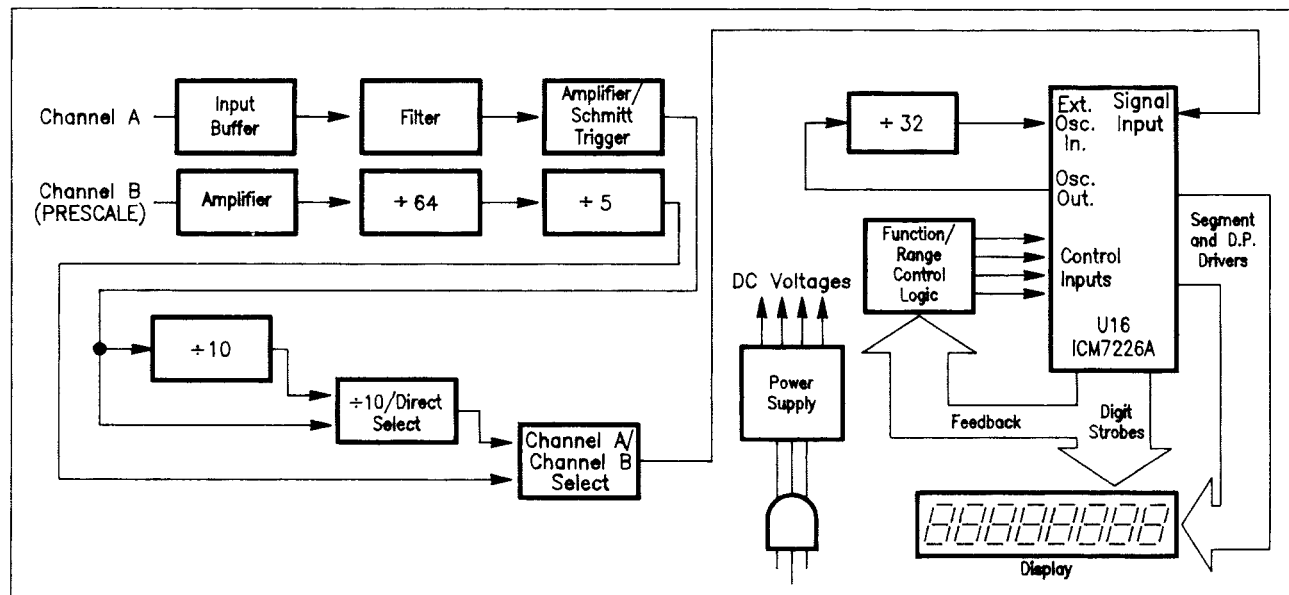


Figure 5. Block Diagram. 1.3 GHz (TCXO)

CIRCUIT DESCRIPTION

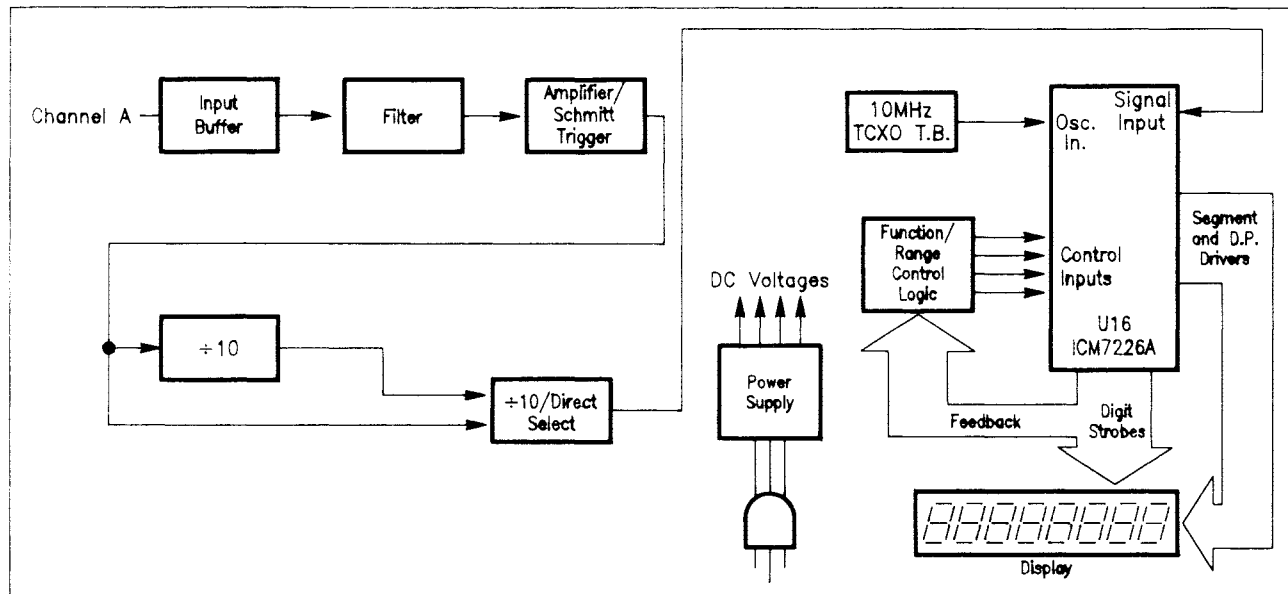


Figure 5-1. Block Diagram. 100 MHz (TCXO)

CIRCUIT DESCRIPTION

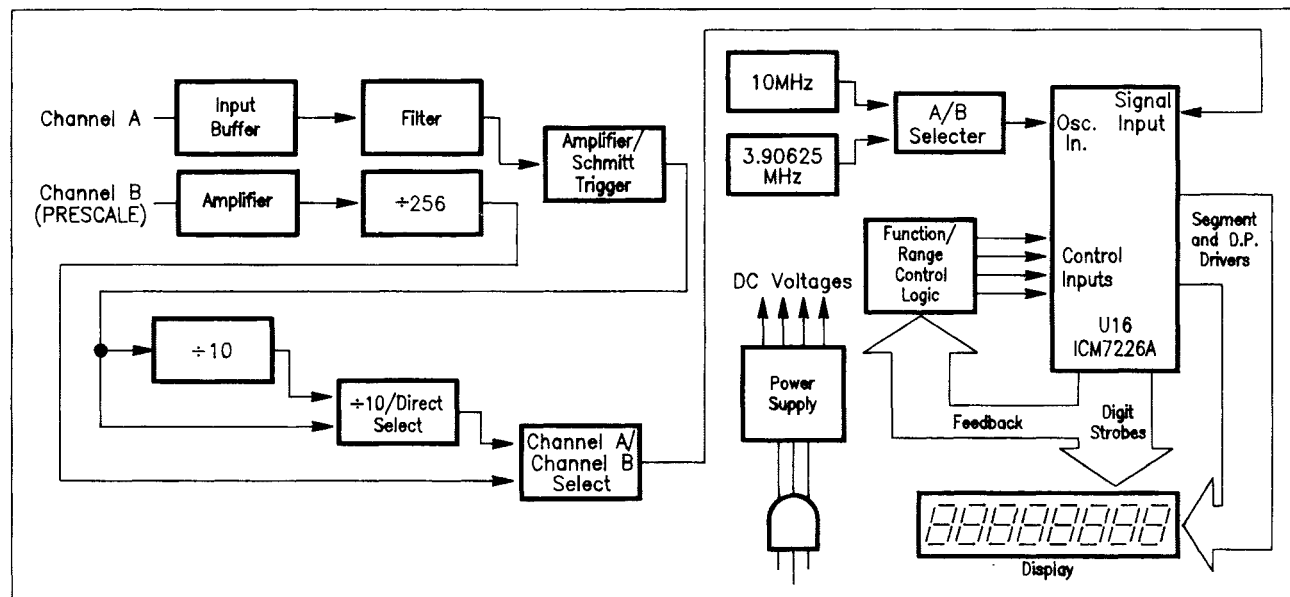


Figure 5-2. Block Diagram. 1.3 GHz (X'TAL)

CIRCUIT DESCRIPTION

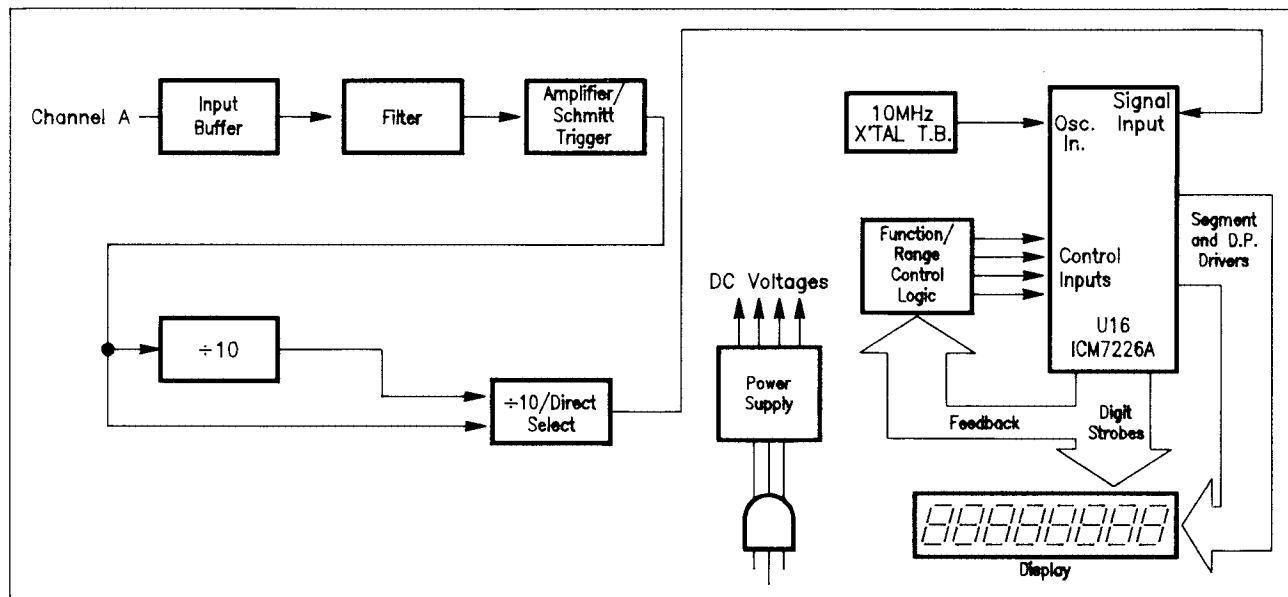


Figure 5-3. Block Diagram. 100 MHz (X'TAL)

CIRCUIT DESCRIPTION

BLOCK DIAGRAM ANALYSIS

Refer to the block diagram of Fig. 5 for an overall view of circuit operation. The counters are designed around an ICM7226A counter chip, U16, which performs all frequency, period, and totalization counting functions.

Before being applied to the 7226A, the Channel A input signal is processed by a high-impedance FET input buffer (including a selectable $\times 10$ attenuator), a selectable low-pass filter, and an amplifier/Schmitt trigger circuit which squares up the signal.

The Channel B (PRESCALE) (1.3 GHz) input is processed by a high-frequency amplifier and prescaler, which divides the incoming frequency by 64. The signal is further divided by 5 on the main board, giving a total division of 320. This division in input frequency is offset by a decimal point shift, and a division by 32 of the time base.

According to operating mode, either the Channel A (either directly or via a divide-by-ten circuit) or the Channel B (PRESCALE) (1.3 GHz) signal is selected and applied to the 7226A.

Four control inputs on the 7226A determine operating mode, resolution, time base frequency, and decimal point placement. As the diagram shows, selected time-multiplexed digit strobes

are fed back to these control inputs via the front panel switches. The control inputs set operating conditions according to which strobes are applied.

The power supply provides various regulated dc voltages. The tap. Of the transformer is universal, and can be switched as needed to accommodate various line voltages via the fuse holder with voltage selection located on the rear panel.

SCHEMATIC DIAGRAM ANALYSIS

This discussion can best be followed by referring to the separately supplied schematic diagram, and to the accompanying figures when directed by the text.

Channel A Input Circuit

The input signal is capacitively coupled via C1 to the divider of R2/R33 and R3. $\times 10$ Attenuator switch S6 selects either the full voltage across this divider ($\times 1$ position) or only the portion across R3 (approximately one tenth of the full amount, $\times 10$ position). This voltage is level-clamped to a maximum of 0.7 volts by transistors Q1 and Q2 and applied to the high-impedance buffer stage. This consists of FET Q3, which provides good sensitivity over the Channel A frequency range, and Q4, which serves as a current source for successive stages.

Channel A Filter

The signal is applied to the low-pass filter consisting of R9 and C9, whose values set a -3dB point of approximately 100 kHz. When LPF switch S7 is pushed in (ON position on schematic), diodes D1 and D2 are biased on. This provides an ac path to ground through D1, and the filter action of R9 and C9 is enabled. When the switch is released (OFF), D1 and D2 are off, isolating C9 from ground, and disabling the filter action.

Channel A Amplifier/Schmitt Trigger

This stage amplifies and shapes the Channel A input to ultimately produce a square wave which is suitable for use in the digital circuits following. The circuit makes use of a 10116 ECL triple line receiver for good response to 100 MHz. Two of the amps in this IC are used to square up the signal, and the third is used as a Schmitt trigger.

The chip supplies a voltage reference of 3.8 volts at pin 11; this is applied through resistors R12 and R13 to the inputs of the first amp (pins 9 and 10). The resistor divider of 5 volts consisting of R10 (Channel A Sensitivity Trimmer) and R11 is also applied to pin 9 of IC1. This results in a quiescent voltage difference of approximately 5 millivolts between the two inputs. This defines the amount of input signal required for proper "squaring" to occur in the first two amps.

The second amp, at pins 4 and 5, is used as a Schmitt

trigger to eliminate false triggering caused by noise. Its trigger threshold is obtained by the resistors R16 and R17.

The third amp, at pins 12 and 13, is also used as a Schmitt trigger to eliminate false triggering caused by noise. Its trigger threshold is obtained from the pin 11 reference through R20, and the amount of hysteresis is controlled by R21.

Transistors Q5 and Q6 are used as ECL-to-TTL level shifters. The waveform obtained across R25 is a 0 to 3 volt square wave with polarity opposite that of the Channel A input signal.

Channel A Divide-by-Ten Circuit/Select

The Channel A output is fed to NAND gate U13A which is used as an inverter. The U13A output at pin 3 is connected to U14, a decade ripple counter which functions as a divide-by-ten. U13B/U13C/U13D pins 4-13 (plus v U15A pins 1-3) selects either the decade-divided signal from U14 pin 2 or the undivided signal from U13A pin 3. This selection is governed by two lines: one from U4B pin 4, which is high in MHz mode, and one from U2 pin 2, which goes high whenever MHz Frequency function is selected. In either of these modes, the decade-divided version is gated via U13C pin 8 through to U16, the counter chip. In other modes, the undivided signal is used.

CIRCUIT DESCRIPTION

Channel B (PRESCALE) Input Circuit (1.3 GHz only)

The input signal is capacitively coupled via C19 and C26 to resistor R27 which provides the 50 Ω termination for the input jack and is level-clamped by high-frequency "hot carrier" diodes D8 and D9 before application to the amplifier IC5. The input signal is capacitively coupled via C19 to IC5, a MAR-6 amplifier which provides a voltage gain of about 3.5, to at least 2000 MHz. Resistors R34 and R35 provide biasing and power supply decoupling and capacitor C24 provides power supply bypassing.

The signal is next capacitively coupled via C20 to IC4, a 64 circuit with standard ECL outputs. The Circuit is operated single-ended with resistor R28 providing hysteresis so the circuit does not self-oscillate and C21 providing AC bypassing.

Transistors Q7 and Q8 are used as ECL-to-TTL level shifters. The waveform obtained across R32 is a 0 to 3.5 volt square wave with a frequency of one-sixty-fourth of the Channel B Input signal.

Channel B Divide-by-Five Circuit (1.3 GHz only)

The Channel B output is fed to U18, a decade ripple counter configured as a divide-by-five. The signal is connected to the second clock pin 6 and the output is taken from the Q3

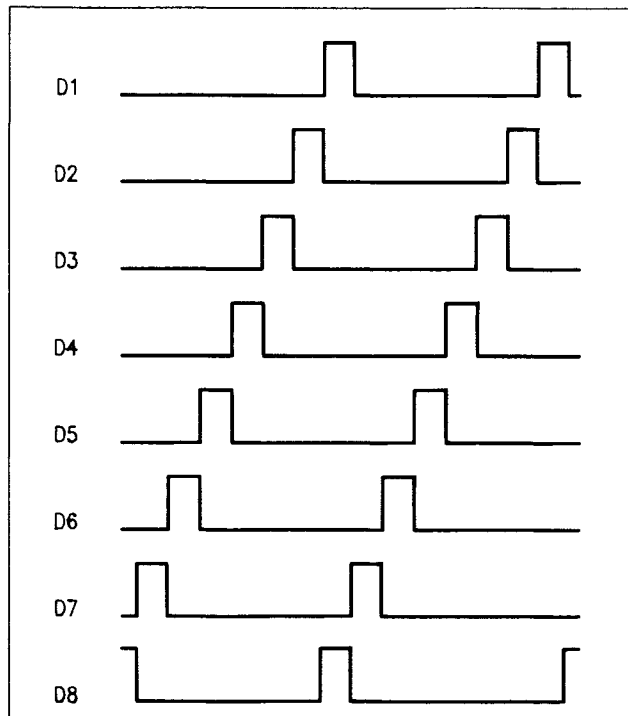


Figure 6. U16 Digit Strokes.

output pin 2.

The upper frequency limit of the ICM7226A counter chip is 10 MHz; the input frequency must be scaled down to within that range. Dividers IC4 and U18 function together to scale the Channel B input by a factor of 320. At the maximum frequency, 1.3 KHz, the output of U18 at pin 2 is a 4.0625 MHz TTL level waveform with a 40% duty cycle.

Channel A/Channel B Select (For 1.3 GHz only)

The Channel A signal from U13C pin 8 (direct or divide-by-ten) and the Channel B signal from U18 pin 2 (divide-by-320) are applied to the circuit consisting of NAND gates U15B/U15C/U15D. U15B input pin 4 is connected to U2 pin 4; this input goes high whenever CH B Frequency function is selected, and the Channel B signal is gated through to U15C pin 8. At all other times, the Channel A signal is gated through.

The combined action of U13 and U15, which is controlled by the front panel FUNC switch S3 via U2/U3C/U3D, provides U16 with an input signal within its frequency limits. In the MHz Frequency function, the Channel A signal (divided by ten in U14) is applied. In CH B Frequency function, the Channel B signal (divided by 320), is applied. In kHz Frequency, PERiod, and TOTALize functions, the Channel A signal is applied with no frequency division.

Channel A Signal Gating (TOTALize mode)

U1D pin 12 is controlled by HOLD switch S2 via debounce flip-flop U1A/U1B pins 1-6. U1D pin 13 is connected via R105 to the rear panel TOTALIZE START/STOP jack. When no signal is connected to the rear panel jack, the jack is pulled high by R103. One of the inputs to the U1C circuit (pin 9) is a line from U2 pin 10 which goes high when the TOTALize frequency is enabled. The undivided signal from U15C pin 11 can thus be gated either manually, by S2, or electronically, by a signal applied at the rear panel jack when the TOTALize function is enabled through U1C.

ICM7226A Counter Circuit

This integrated circuit (U16) is the heart of the unit. It performs all frequency, period, and totalize functions and multiplexes and drives the displays. It requires an input signal of digital logic levels, as provided by the circuits previously discussed. A crystal for the timebase oscillator is required, as well as external connections for feedback of display digit strobes, as described in the following sections.

Digit Strokes and Feedback

The 7226A multiplexes the display by means of digit strobes D1-D8. Each strobe goes high in sequence, as in Fig. 6, turning its display digit on momentarily. As each digit is selected,

CIRCUIT DESCRIPTION

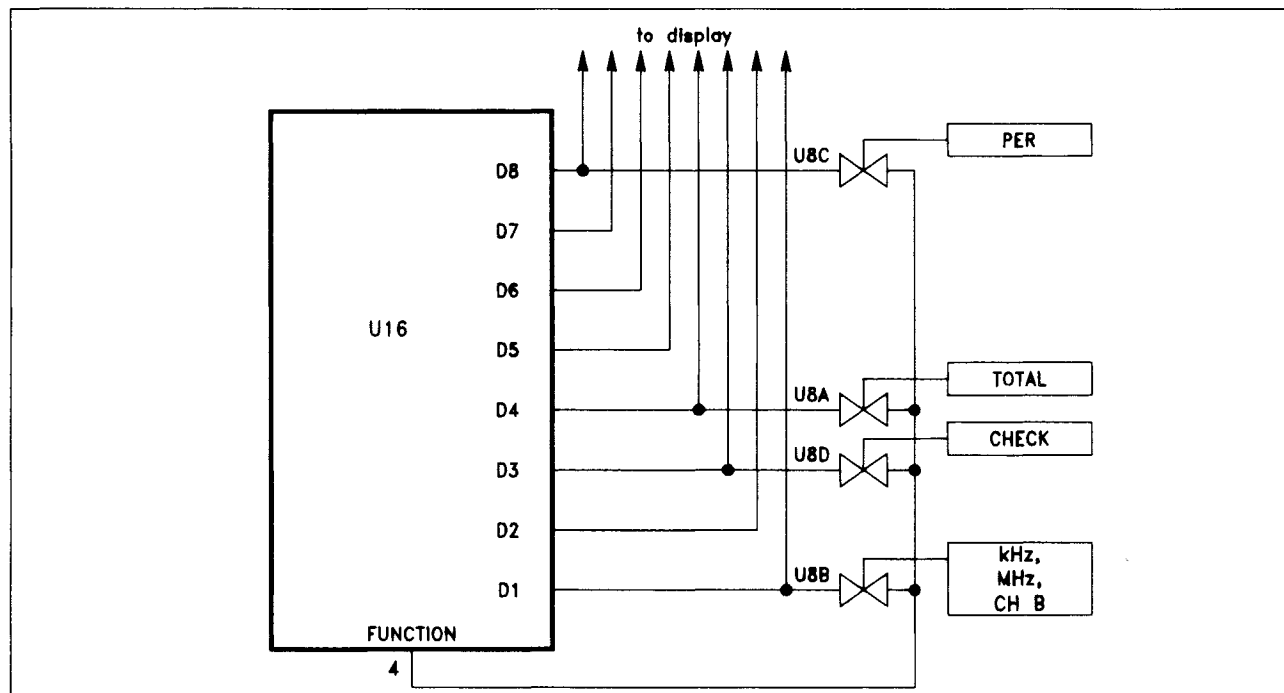


Figure 7-1. Function Selection 1.3 GHz

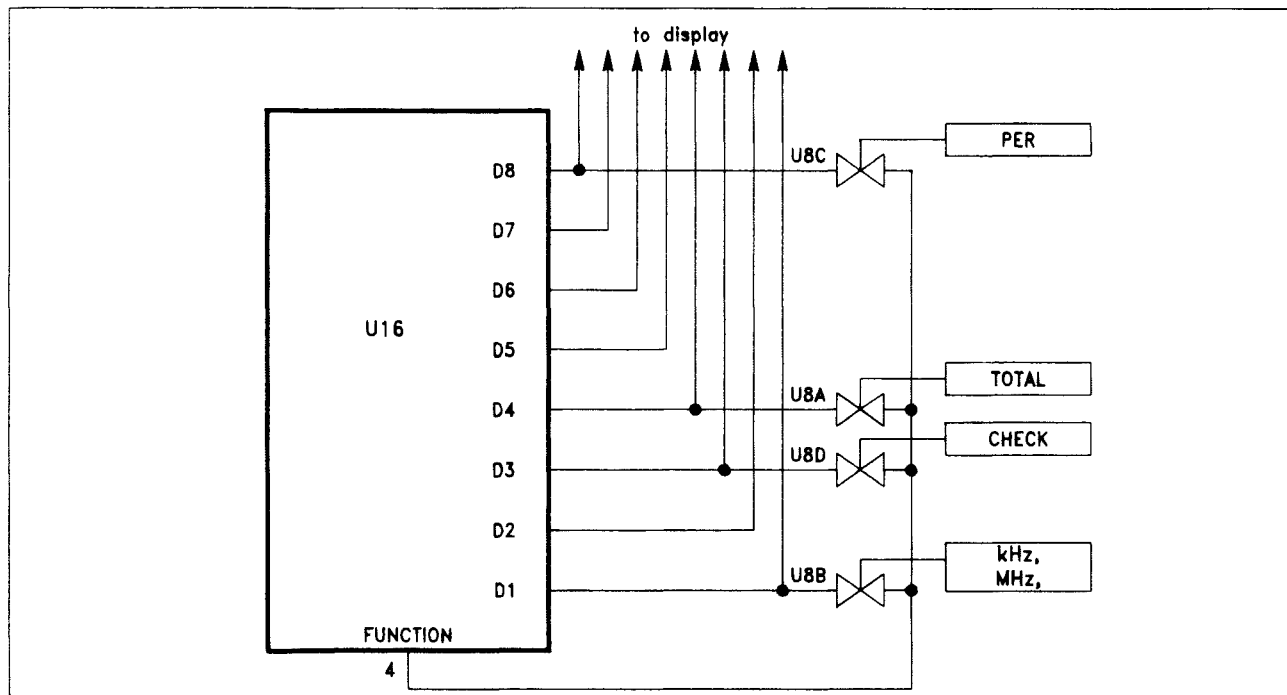


Figure 7-2. Function Selection 100 MHz

CIRCUIT DESCRIPTION

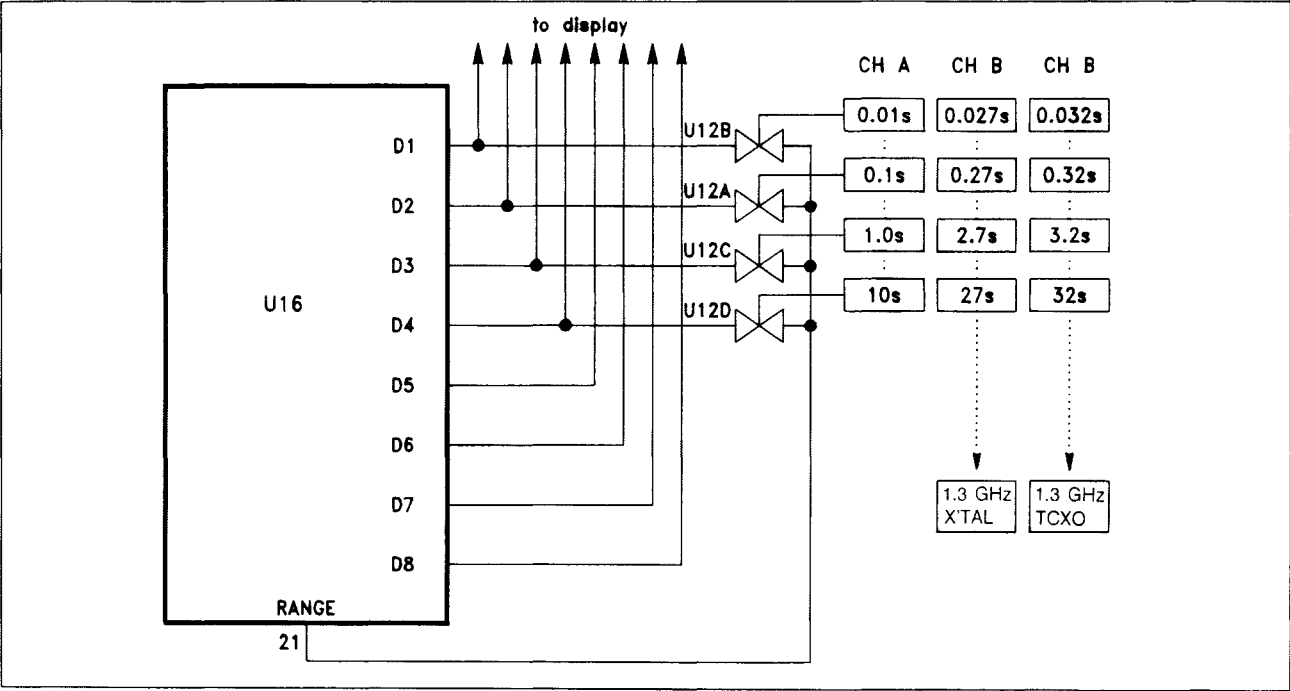


Figure 8. Gate Selection (Channel B for model 1.3 GHz only)

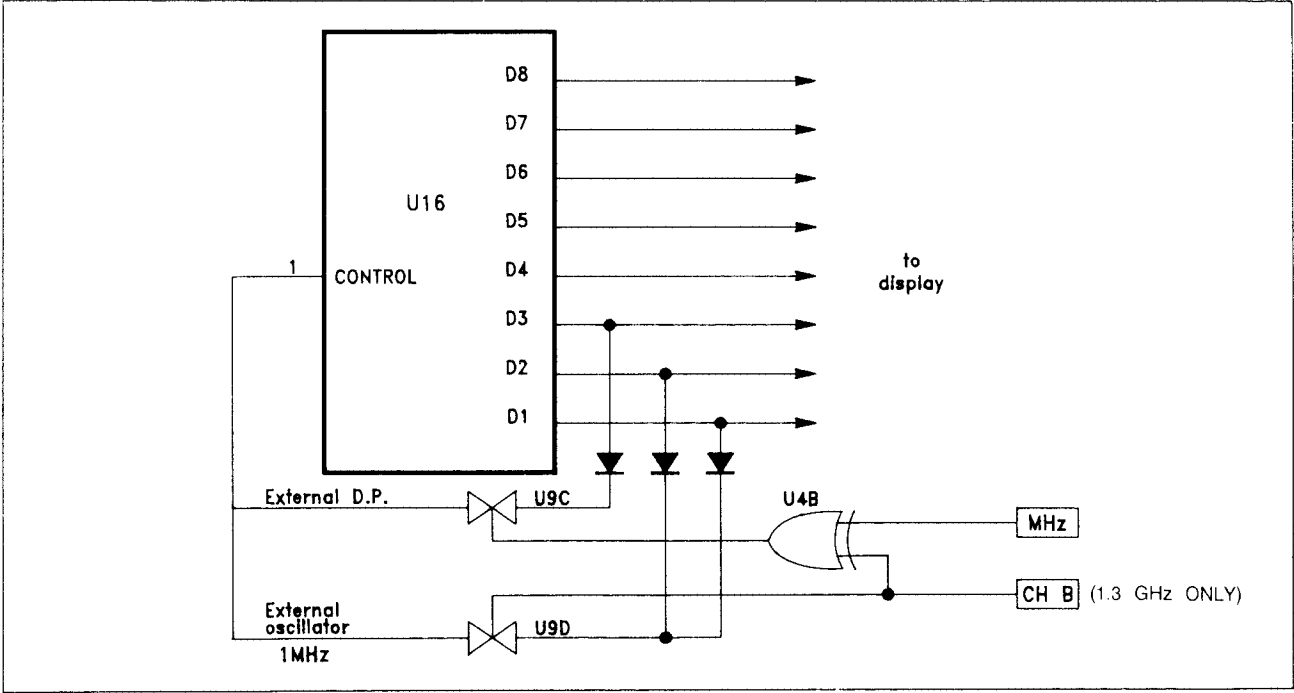


Figure 9. Additional Strobe Feedback; U16 Pin 1. (Model 1.3 GHz only)

CIRCUIT DESCRIPTION

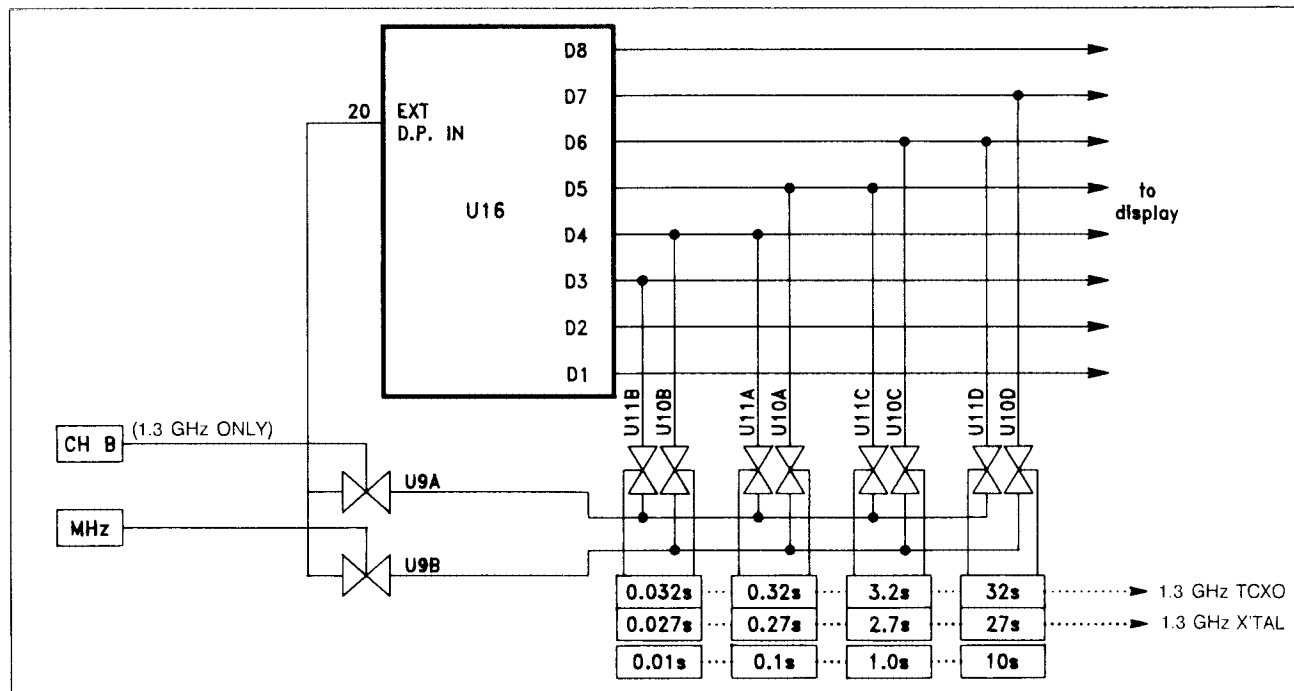


Figure 10. External Decimal point control (for made 1.3 GHz only)

the proper seven-segment and decimal point information for that digit is sent out at the same time on pins 8-11 and 13-16.

The digit strobes D1-D8 are also used to control the 7226A by selective feedback to four control pins, 1, 4, 20, and 21. Operating mode, resolution, and other parameters are determined by which strobe signal is present at each control input. Strobe feedback is controlled by the front panel settings through logic. Each control pin and its feedback network is discussed below.

Function Selection

Function selection is controlled by FUNCTION pin 4. As shown in Fig. 7, this pin is connected to one of digit strobes D1, D3, D4, or D8 through electronic switches U8B/U8D/U8A/U8C respectively via the FUNCTION mode logic circuits consisting of U2, U3C/U3D, and FUNCTION switch S3.

Gate Selection

Gate selection is controlled by RANGE pin 21. As shown in Fig. 8, this pin is connected to one of the digit strobes D1-D4 through electronic switches U12B/U12A/U12C/U12D respectively via the GATE mode logic circuits consisting of U6, U3A/U3B, and GATE switch S4.

Additional Control — Pin 1

Additional control of U16 is provided by feedback of strobes

D1, D2, and D3 to CONTROL IN pin 1. As shown in Fig. 9, this pin is connected through electronic switches U9C and U9D. Digit strobe D3 is gated by U4B pin 6, which goes high whenever either MHz or CH B is engaged, enabling the External Decimal Point.

Connection of strobe D1 to U16 pin 1 instructs U16 to ignore the normal time base input at pin 35 and instead use the input at pin 33. This pin is connected to the output of U17, a binary counter which divides the TCXO time base frequency (through U16 pin 38) by 32. This is required to offset the effect of dividing the input by 320 in the Channel B circuit.

The normal digit multiplex rate with a 10 MHz time base is approx. 500 Hz. Dividing the time base by 32 would normally produce an undesirable display flicker because of the slow multiplex rate (approx. 15 Hz). This is remedied by also feeding strobe D2 to U16 pin 1. This enables "1 MHz" mode in U16, which is normally used when a 1 MHz time base is substituted for 10 MHz. In this mode, U16 speeds up the multiplex rate by a factor of 10, for a 500 Hz rate at 1 MHz. In these two Models, they raise the rate from 15 Hz to approx. 150 Hz, which is acceptable.

Division of the time base and speed-up of the multiplex rate (strobes D1, D2 applied to U16 pin 1) are only enabled during CH B (1.3 GHz only) selection, since that is the only mode

CIRCUIT DESCRIPTION

which introduces the non-decade division of 320 in the input.

External Decimal Point

In kHz Frequency, PERiod, and TOTALize modes, the automatic decimal point placement is enabled in U16. However, when MHz or CH B Frequency is selected, application of D3 instructs U16 to place a decimal point at the display digit whose strobe appears at pin 20, EXT D. P. IN. Placement is determined as shown in Fig. 10, and depends on function and gate time selected.

Time Base

The time base utilized for the counter is a 10 MHz TCXO (temperature-compensated crystal oscillator) for increased temperature stability. As shown on the schematic diagram, the TCXO is connected directly to the oscillator input of U16 pin 35.

HOLD Switch

Refer to the schematic diagram. The HOLD switch, S2, is connected via U1A and U1B, which provides switch debounce, to U16 and U1D. The connection to U16 instructs that chip to enter the display HOLD mode whenever the switch is engaged. In TOTALize operation, however, U16 would freeze only the display but keep on counting; this is remedied by also connecting S2 to U1D/U1C pins 8-13. As described previously,

this cuts off the input from U16 (as does a low at the TOTALIZE START/STOP jack) and halts the counting process.

LED Indicators

The MHz indicator, D24, is connected to the output of U4B pin 6. This output, used in other sections as previously described, goes high when MHz or CH B Frequency is selected.

The kHz/ μ s indicator, D25, is connected to the output of U4A pin 3. It lights whenever kHz Frequency, PERiod, or CHECK function is selected.

The GATE indicator, D26, is connected via inverter U7F (pins 14 and 15) to U16 pin 3. This pin goes low whenever a measurement is in progress.

The OVERFLOW indicator, D27, is connected directly between U16 pins 22 and 8, and lights whenever a "9,9,9,9,9,9,9" count has been exceeded.

The FUNCTION indicators; kHz, MHz, CH B, PER, TOTAL, and CHECK are connected via inverters U5B/U5F/U5C/U5D/U5E/U5A respectively to the outputs of the Function counter U2. The FUNCTION switch S3 and flip-flop U3C/U3D determines the output of the Function counter. The power-on reset circuit consisting of R108, C102, D107 and U7D connected via D103 assures that U2 Pin 3 initially and the kHz Frequency indicator on.

The gate indicators; 0.032s/0.01s, 0.32s/0.1s, 3.2s/1.0s, and 32s/10s are connected via inverters U7B/U7C/U7A/U7E respectively to the outputs of the Gate counter U6. The GATE switch S4 and flip-flop U3A/U3B determines the output of the Gate counter. The power-on reset circuit connected via diode D106 assures that U6 pin 3 will be high initially and the 0.032s/0.01s indicator on.

Power Supply

The transformer is a universal type whose primary windings may be re-connected for various line voltages by replacement of fuse holder with voltage selector on the rear panel.

The outputs of the transformer secondary windings are fused separately for increased safety and then applied to the rectifier circuits.

The output of one secondary side rectified by D110 and D111 and filtered by C119 and C120. Voltage Regulator Q9 provides + 5 volts (VA) with good regulation and adequate power for the digital portion of the instrument.

The other secondary is rectified by D113 and D114, and filtered by C123 and C124. Voltage Regulator Q10 provides + 5 volts (VB) for powering the Channel A and B Input circuits.

Section VIII

MAINTENANCE AND CALIBRATION



WARNING

The following instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing other than contained in the operating instructions unless you are qualified to do so.

FUSE REPLACEMENT

If the primary line fuse FS5 blows, the display and the FUNCTION or GATE LED indicators will not light and the counter will not operate. The fuse should not normally open unless a problem has developed in the unit. Try to determine and correct the cause of the blown fuse, then replace only with a fuse of the correct rating. For 100 or 120 V operation a 0.2 A, 250 V, 3AG fuse should be used and for 220 or 240 V operation a 0.1A, 250 V, 3AG fuse should be used. The primary line fuse, FS5, is located on the rear panel (see Fig. 2).

If replacement of the primary line fuse does not alleviate the problem, then one of the four transformer secondary fuses, FS1/FS2/FS3/FS4, may be open. The four fuses are located

on the main circuit board (see Fig. 11). Replace only with a 0.5A, 125 V or 250 V 5x20 mm for each.

LINE VOLTAGE CONVERSION

The primary winding of the power transformer is tapped to permit operation from 100, 120, 220, or 240 VAC, 50/60 Hz line voltage. Conversion from one line voltage to another is done by simply replacing the fuse holder with voltage selector located on the rear panel (see Fig. 2-12).

To convert to a different line voltage, perform the following procedure:

1. Make sure the power cord is unplugged.
2. Reset the Fuse holder with voltage selector for the desired line voltage as shown on the rear panel.
3. A change in line voltage may also require a corresponding change of fuse value. Install the correct fuse value as listed in the **FUSE REPLACEMENT** section.

ADJUSTMENTS

This unit was accurately adjusted at the factory before shipment. Readjustment is recommended only if repairs have been made in a circuit affecting adjustment accuracy, or if you have a reason to believe the unit is out of adjustment. However, adjustments should be attempted only if the following equipment is available:

1. 10MHz Standard with an accuracy of at least ± 0.1 PPM (1×10^{-7}) and an output level of at least 100 mV rms.
2. RF Generator (Wavetek 3001 or equivalent).
3. RF Millivoltmeter (Booton 92BD or equivalent).

The following adjustments require the removal of the case top; unplug the power cord, turn the unit over and remove the four Phillips screws, two holding the rear rubber feet and the two next to the front rubber feet. Locations of the electrical adjustments are shown in Fig. 11.

ADJUSTMENT	FUNCTION OF ADJUSTMENT
TCXO	Time Base Frequency
R10	Channel A Sensitivity
R118	Totalize Sensitivity

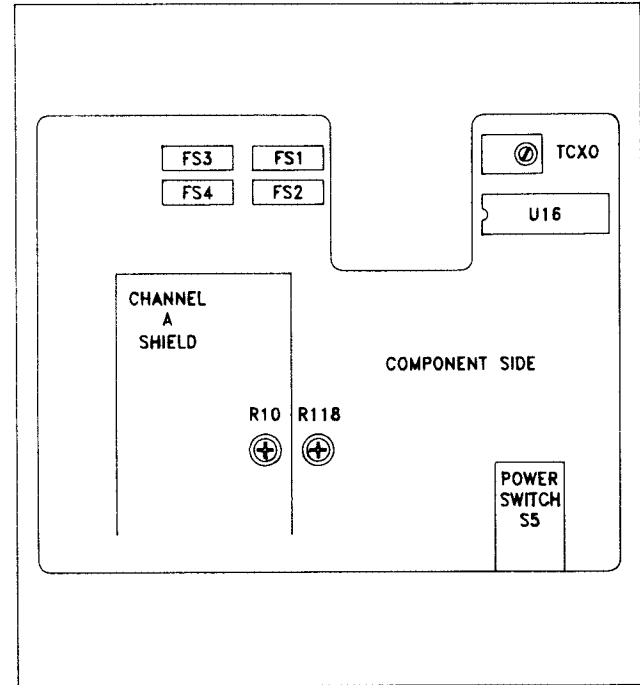


Figure 11. Main board Adjustments, Component Side View.
1.3 GHz (TCXO), 100 MHz (TCXO)

MAINTENANCE AND CALIBRATION

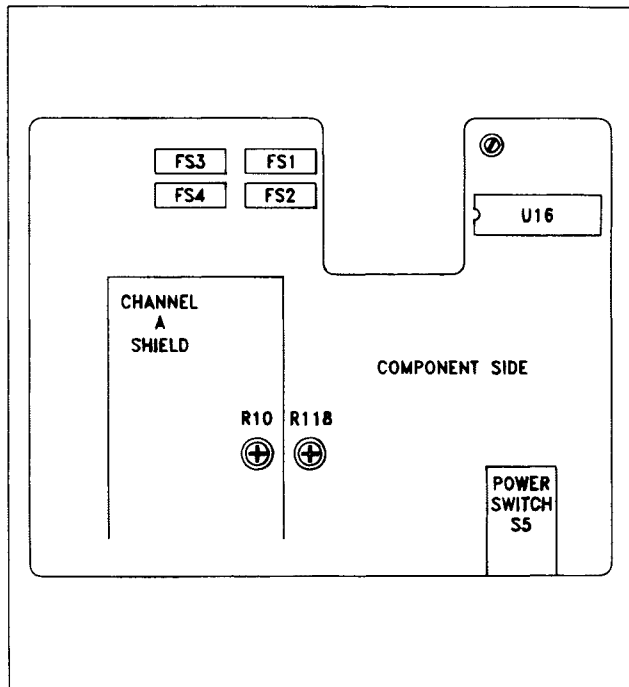


Figure 11-1. Main board Adjustments, Component Side View.

100 MHz (X'TAL)

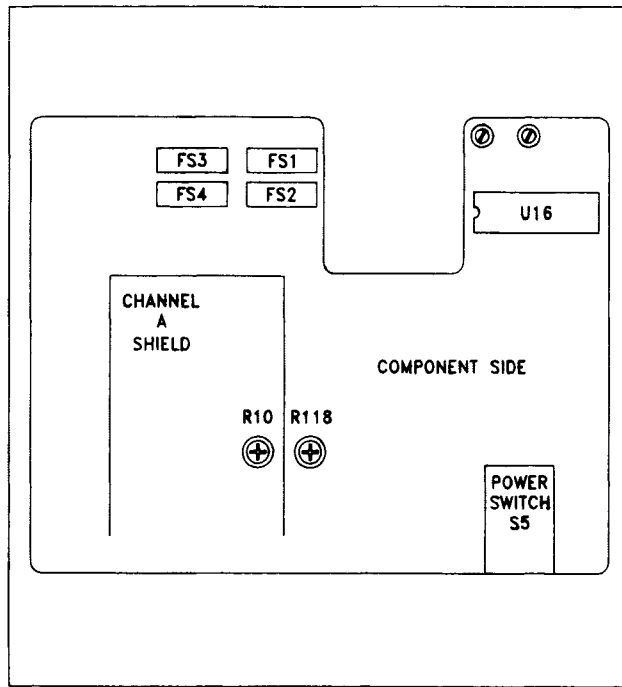


Figure 11-2. Main board Adjustments, Component Side View.

1.3 GHz (X'TAL)

MAINTENANCE AND CALIBRATION

Time Base Adjustment

This adjustment should be performed after a one hour warmup with the top case on but not screwed down, allowing the heat rise inside the unit to stabilize. The top case is then lifted off and the adjustment made.

1. Set the unit for **kHz** mode with the **FUNC** switch and **1.0s** Gate Time with the **GATE** switch.
2. Connect the 10 MHz standard frequency source to **Channel A Input**.
3. Using a small non-metallic slotted screwdriver, adjust the TCXO for a reading of $10000.000 \pm 1 \text{ Hz}$ on the unit display.

Channel A Sensitivity Adjustments

1. Set the unit to **MHz** mode with the **FUNC** switch and **0.01s** Gate time with the **GATE** switch.
2. Connect the RF Generator and the RF Millivoltmeter with a BNC Tee to the **Channel A Input**. Set the RF Generator frequency output to read 100.000 MHz and set its level for a reading of 50 mV rms on the RF Millivoltmeter. The counter display should read 100.000 ± 1 count.
3. Slowly decrease the RF Generator output level until the

counter's least significant digit varies by more than 3 counts. The counter will typically start to read lower.

4. Adjust the **Channel A Sensitivity Trimmer R10** (through the hole in the metal shield) so that the counter display reads $100.000 \text{ MHz} \pm 1$ count.
5. Repeat steps 3 and 4 until trimmer **R10** no longer can give a stable $100.000 \text{ MHz} \pm 1$ count on the display. The typical range of the RF level required would be approximately 20 mV to 30 mV rms.

TOTALIZE Adjustments

1. Set the unit for **TOTAL** mode with the **FUNC** switch.
2. Connect the RF Generator and RF Millivoltmeter with a BNC Tee to the Channel A input. Set the RF Generator frequency output to 10.000 MHz and its level for a reading of 15.0 mV rms on the RF Millivoltmeter.
3. Adjust **Trimmer R118** until the display just starts to change the second digit from the left.

Section IX

TROUBLESHOOTING

The following troubleshooting steps provide a logical procedure for fault isolation. If the procedure cannot, of course, guarantee to pinpoint every possible problem, it will in most cases localize the problem to a certain area.

Most of these troubleshooting steps require removal of the top cover as described previously.

General Fault Isolation

1. **Performance test** Test each operating mode by applying an appropriate signal to Channel A and Channel B as directed in Table 4. Frequency accuracy of the signal isn't critical, but amplitude should be adequate to produce stable readings (use caution not to exceed the maximum Channel B input ratings). On Channel A, the filter, and/or attenuator may be used to stabilize the reading.
2. **Fault Isolation** Proceed as follows according to the results of the test:
 - a. If no display can be obtained at all, follow the procedure for **"No Display"**.
 - b. If display shows abnormalities such as missing decimal

points or unlit segments or digits, follow the procedure for **"Abnormal Display"**.

- c. If display appears normal, but value is incorrect or unstable (in Channel B, Channel A, or both), follow the procedure for **"Incorrect or Unstable Display Value"**.
- d. If problem is not adequately described by any of the above, start at **"No Display"** and proceed through each step until the difficulty is isolated.

TROUBLESHOOTING

Table 5 Operational Test

Input Frequency	Operation Mode	RESOLUTION	Normal (Ideal) Display
10 kHz	FREQUENCY kHz	100 Hz 10 Hz 1 Hz .1 Hz	10. 10.00 10.000 10.0000 **
10 kHz	FREQUENCY MHz	1 kHz 100 Hz 10 Hz 1 Hz	.010 .0100 .01000 .010000 *
100 MHz	FREQUENCY CH B 1.3 GHz only	10 kHz 1 kHz 100 Hz 10 Hz	100.00 100.000 100.0000 100.00000 **
10 kHz	PERiod	.1 μ SEC .01 μ SEC .001 μ SEC .0001 μ SEC	100.0 100.00 100.000 100.0000
10 kHz	TOTALize	not applicable	Display a accumulates, with fifth digit from right changing at approximately 1 Hz.
not required input	CHECK	100 Hz 10 Hz 1 Hz .1 Hz	10000.0 10000.00 10000.000 0000.0000* over lit

Input Frequency	Operation Mode	RESOLUTION	Normal (Ideal) Display
Less than 100 Hz	PERiod	.0001 μ SEC	over lit ***

NOTE:

* :Measurement delay of 10 seconds.

** :Measurement delay of 27 seconds. (1.3 GHz/crystal)

*** :Measurement delay of at least ten seconds.

NO Display.

1. Check supply voltage at U16 pin 25 for approximately + 5 volts. If this voltage isn't present, check ac input, fuse and + 5V (VA) power supply circuit (D110, D111, C120, Q9). Otherwise proceed to "**Abnormal Display**".

Abnormal Display.

1. **Digit Strokes and time base** Set the unit to any operating mode and check for the digit stroke waveforms of page 8 at U16 pins 22-24 and 26-30. If these are normal, proceed to step 2. If not, check the output of the time base oscillator at pin 38 for a waveform of frequency 10 MHz and peaks of 0 and 2.4 V. If normal, check U16 and display digits; if no output is obtained, check oscillator components, U16 and + 5V (VB) power supply (D113, D114, C124, Q10).
2. **Display test** Enable display self-test by connect U16 pins 1 and 22 to each other via a 1N4148 diode (anode to pin 22). Display should be all "eights" with all decimal points and OVERFLOW indicator on. If not, check displays and U16 segment driver pins 8-11 and 13-16. Waveform at each of these pins should approximate a dc level of about 1.0 V, with negative spikes of about 4 kHz. Waveforms

shown are with display digits connected.

3. **Decimal points** If the problem involves decimal points in MHz or Channel B modes, check the mode selection logic as in "step 5" of "**Incorrect or Unstable Display Value**".
4. **MHz or kHz/ μ SEC indicators** For problems involving these (D24, D25), check the mode selection logic as in "**Incorrect or Unstable Display Value**", step 5.
5. **GATE indicator (1.3 GHz/crystal)** If the GATE indicator, D26, does not function properly, check D26, U7 and U16 pin 3. D26 is connected via U7 to pin 3, which goes low whenever a measurement is being taken. (If this pin shows no activity, check for proper mode selection as in "**Incorrect or Unstable Display Value**", step 5).
6. **Function indicator** If the Function indicators kHz, MHz, CH B, PER, TOTALize, and CHECK square LEDs, does not function properly, check LED1-LED6, U5 and U2.
7. **Gate time indicator (1.3 GHz/crystal)** If the Gate time indicator .01/.027S, .1/.27S, 1/2.7S, and 10/27S square LEDs does not function properly, check LED7-LED10, U6 and U7.

TROUBLESHOOTING

Incorrect or Unstable Display Value.

1. **Half-splitting: Channel A** Apply an appropriate signal to Channel A and check the waveform at the collector of Q6. Waveform should be a square wave (0-2.8V) of same frequency and polarity as the Channel A input signal. If the waveform is normal, proceed step 3; otherwise, check for a problem in the Channel A analog circuitry; see the next step.
2. **Channel A analog circuits** Table gives waveforms for the Channel A input buffer and signal shaping circuits, along with input conditions required for obtaining them. The order of table entries is from input to output, permitting either sequential or half-splitting trouble-shooting techniques, as desired by the user.
3. **Half-splitting: Channel B (1.3 GHz only)** Apply an appropriate signal to the Channel A jack. Check the output of the ECL-to-TTL converter, collector of Q7. A TTL level waveform should be observed; its frequency should be 1/256 of input frequency. Note that because of the high frequency, shape irregularities in this waveform can be expected.

If the waveform is correct, proceed to step 5. If not, check the Channel B circuits.

4. **Channel B input amplifier (1.3 GHz only)** With signal still applied at the Channel B input, check for presence of signal at the input of IC4, and the output of Q7 and Q8. If not detected, check IC4 and associated components.

Table 6 Channel a analog circuit waveform

Test Point	Waveform (See Note 1 next page)
A. Gate of Q3.	Identical to input.
B. Gate of Q3, but with ATTN set to x10.	1/10 amplitude of input.
C. Source of Q3. Connection point of C8, C9, C11, R9.	1 Vp-p, 10 kHz sine wave centered at + 1.3 V. (see Note 2 next page)
D. IC1 pin 10.	1 Vp-p, 10 kHz sine wave centered at + 3.8 V.
E. IC1 pin 9, 11.	DC level of + 3.8 V.
F. IC1 pin 4 or 7.	1 Vp-p, 10 kHz rounded square wave centered at + 3.8 V.
G. IC1 pin 5 or 6.	Same as F, but inverted.
H. IC1 pin 3 or 12.	Same as F, with squarer edges.
I. IC1 pin 2.	Same as H, but inverted.
J. IC1 PIN 13.	0.7 Vp-p, 10 kHz square wave centered at + 3.8 V.
K. IC1 pin 15, or base of Q5.	1 Vp-p, 10 kHz square wave centered at + 3.8 V.
L. IC1 pin 14, or base of Q6.	Same as K, but inverted.

TROUBLESHOOTING

Note 1. Counter input of 10 kHz, 1 Vp-p sine wave for all measurements except point C; see Note 2 below. All measurements made with ATTenuator set to x1, except point B. LPF may be engaged to eliminate input noise, except point C; see NOTE 2 below.

Note 2. Counter input for point C test is 100 kHz, 1 V pk-pk. With LPF switch off, point C waveform should be approximately 1 V pk-pk; with LPF on, it should diminish to about 0.7 Vp-p.

5. **Mode selection logic** Operating mode, resolution, and other factors are determined by feedback of the U16 digit strobes D1-D8 to various control pins of this same chip. This feedback is controlled, either directly or through logic, by the front panel switches. Tables 3 and 4 give normal logic conditions in these feedback connections.

6. **Channel A kHz/MHz select** The gates of U13, select either the kHz or MHz signal, according to the logic state of a line from U2 pin 2 to U13 pin 9 and a line from U4 pin 6 to U13 pin 4 and 5. as follow:

- a. When the line from U2 pin 2 is high, U19 pin 2 should have a TTL waveform of same frequency as the MHz output.
- b. When the line from U4 pin 6 to U13 pin 4 and 5 is low, the TTL frequency at U19 pin 2 should be same as the

kHz input. If the waveform is abnormal, check U13 pin 1-6, pin 8-13.

c. Divide-by-ten. U14 and U13 form a circuit which divided the signal at U13 pin 3 by 10 and selects either the divided signal or the direct signal for application to U6.

d. The U14 output frequency at pin 2 should be 1/10 that of the input at pin 8 (U13 pin 3). If not check U14.

Table 7 Check of different gate time

Front Pannel Gate Engaged	Test Points	Waveform
Gate Time .01 Sec	U16 pin 21 U9 pin 4 U9 pin 1	U16 strobe D1 (pin 30). U16 strobe D4 (pin 27). U16 strobe D3 (pin 28).
Gate Time .1 Sec	U16 pin 21 U9 pin 4 U9 pin 1	U16 strobe D2 (pin 29). U16 strobe D5 (pin 26). U16 strobe D4 (pin 27).
Gate Time 1.0 Sec	U16 pin 21 U9 pin 4 U9 pin 1	U16 strobe D3 (pin 28). U16 strobe D6 (pin 24). U16 strobe D5 (pin 26).
Gate Time 10 Sec	U16 pin 21 U9 pin 4 U9 pin 1	U16 strobe D4 (pin 27). U16 strobe D7 (pin 23). U16 strobe D6 (pin 24).

TROUBLESHOOTING

7. Channel A/Channel B Select (1.3 GHz only)

- a. The selection in U19 is controlled by a line from U2 pin 4 (see Table), which goes high whenever CH B mode is engaged. When it is high, the output of U1 pin 8 should be selected CHB mode.
- b. When the line from U2 pin 4 is low (meaning some mode other than Channel A or B is selected), the frequency at U1 pin 8 should be the same as that at U19 pin 18, except in TOTAL mode, as described in step c.
- c. Gating of the direct signal from U19 pin 18 is also controlled by the input to U19 pin 5,6 which goes high in all modes except TOTALize. In that mode, U19 pin 8 is connected to the output of U19 pin 6. This output should be high when the HOLD switch S2 is disengaged, and no input is applied to rear panel jack. A TTL low is applied to this jack, or if S2 is engaged, U19 pin 6 should go the low, disabling U19 pin 18 (constant low output). In that event, output at U1 pin 8 should be a constant low. If these conditions are not normal, check U19, U1, U2 and S2.

8. **Reset** Check that all readings are cleared to zero when RESET switch is pushed. If not, check S1.

Table 8 Check of Function Logic

Function Engaged	Test Points	Waveform
Frequency kHz	U16 pin 4 U4 pin 1, 3 D25 U2 pin 3	U16 strobe D1 (pin 30). Logic high. Lit. Logic high.
Frequency MHz	U16 pin 4 U9 pin 5 U9 pin 3 U16 pin 20 U4 pin 4 U2 pin 2	U16 strobe D1 (pin 30). Logic high. Same as U9 pin 4 (U16 digit strobe selected by Gate switch, see Table 3). Logic high. Logic high (see other entries for U4 pin 6).
Frequency CH B (1.3 GHz only)	U16 pin 4 U9 pin 12,13 U9 pin 2 U16 pin 20 U9 pin 9,10 U4 pin 5 U4 pin 6 U19 pin 4 U2 pin 4	U16 strobe D1 (pin 30.) Logic high. Same as U9 pin 1 (U16 digit strobe selected by Gate switch, see Table 3). See last entry in this table. Logic high. Logic high (see other entries for U4 pin 6). Logic high (see step 6 of "Incorrect or Unstable Display Value" procedure). Logic high.

TROUBLESHOOTING

Function Engaged	Test Points	Waveform
PERiod	U16 pin 4 U4 pin 11,12 D25 U2 pin 7	U16 strobe D8 (pin 22). Logic high. Lit. Logic high.
TOTALize	U16 pin 4 U19 pin 6 U2 pin 10	U16 strobe D4 (pin 27). Logic high.
CHECK	U16 pin 4 U4 pin 13 U2 pin 1	U16 strobe D3 (pin 28). Logic high. Logic high.
Either Frequency MHz or Frequency CH B	U4 pin 6 D24 U9 pin 6	Logic high. Lit. Logic high.

Section X FUSE REPLACEMENT AND VOLTAGE SELECTION

This instrument is the universal line voltage operation; 100V, 120V, 220V and 240V. The below is explaining the user how to replace fuse.

1. Extract the fuse drawer from the AC socket with the aid of a screwdriver (The extra safe fuse drawer can only be extracted with the aid of a tool. Eg. screwdriver.)
2. Only then the fuse holder with voltage selector can be removed from the fuse holder.

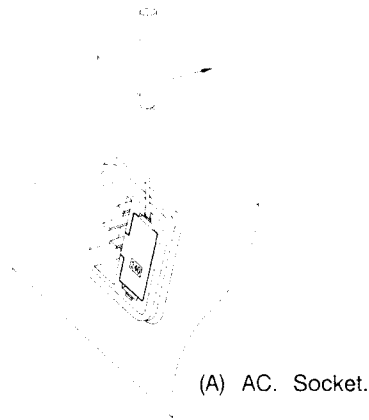


Figure 12-1. Fuse replacement and voltage selection

3. Pull out the fuse link from the fuse holder with voltage selector and then replace a new fuse rated voltage in accordance with specific required fuse or select the voltage according to the user's local line source.
4. When finish the replacement, install the equipments follow up as figured steps D,C and B. The equipments can be easily installed by hands.

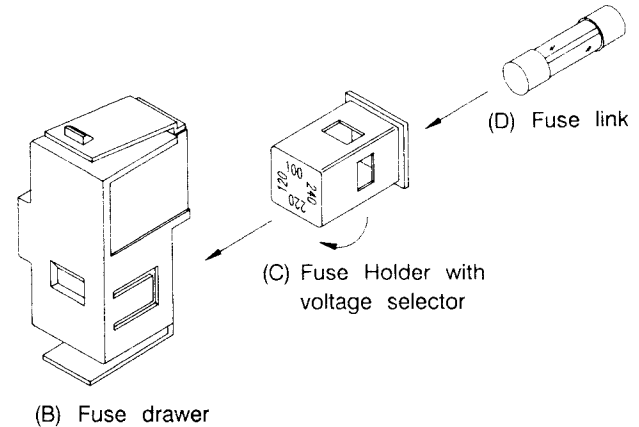


Figure 12-2. Fuse replacement and voltage selection

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