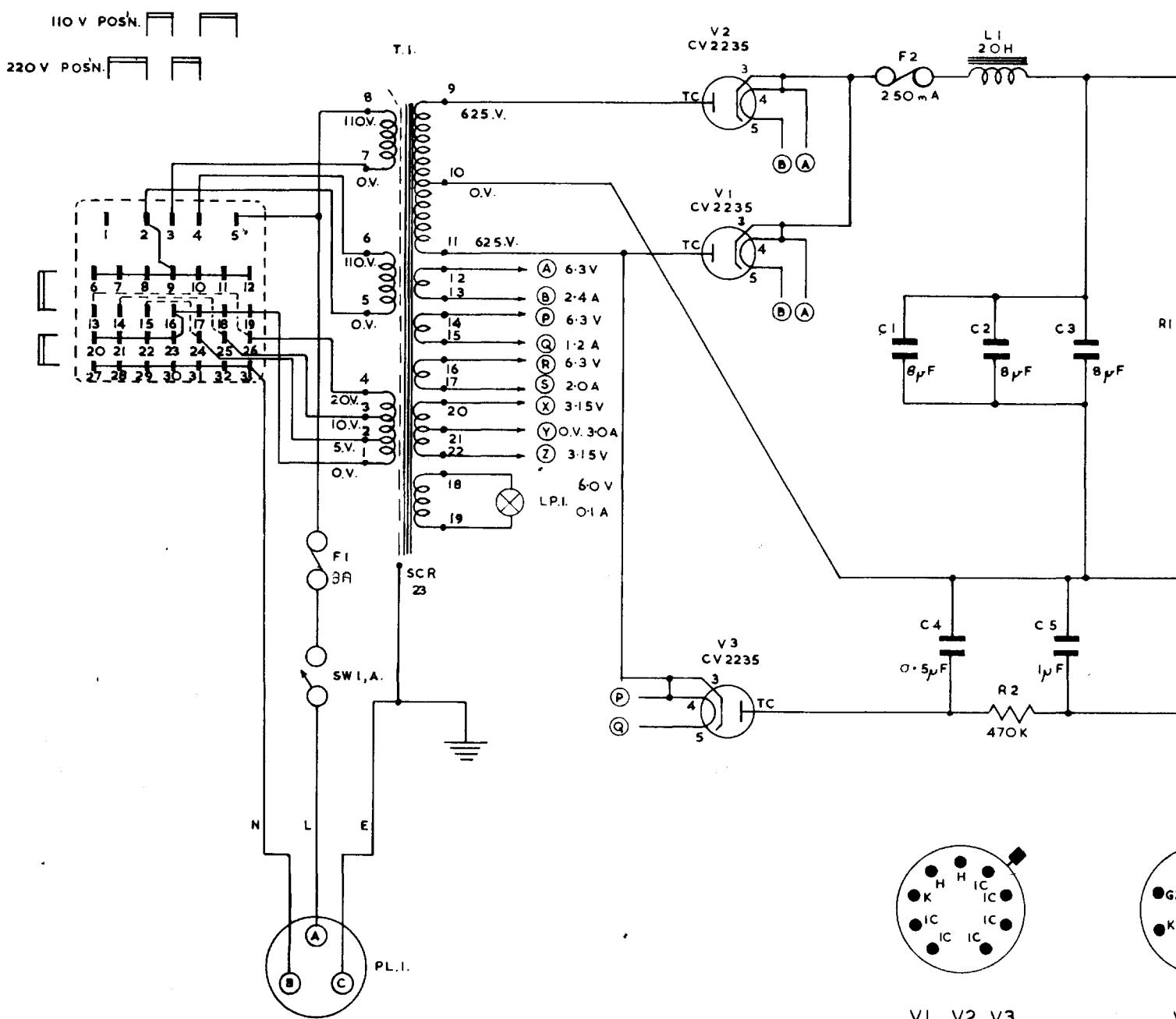


R					R2	
C					C1 C4 C2 C3	
MISC.	F1 SW I.A. PL.I.	T1 PL.I.	L.P.I.	V2 V1 V3	F2 L1	C5



V1 V2 V3

Fig. 5

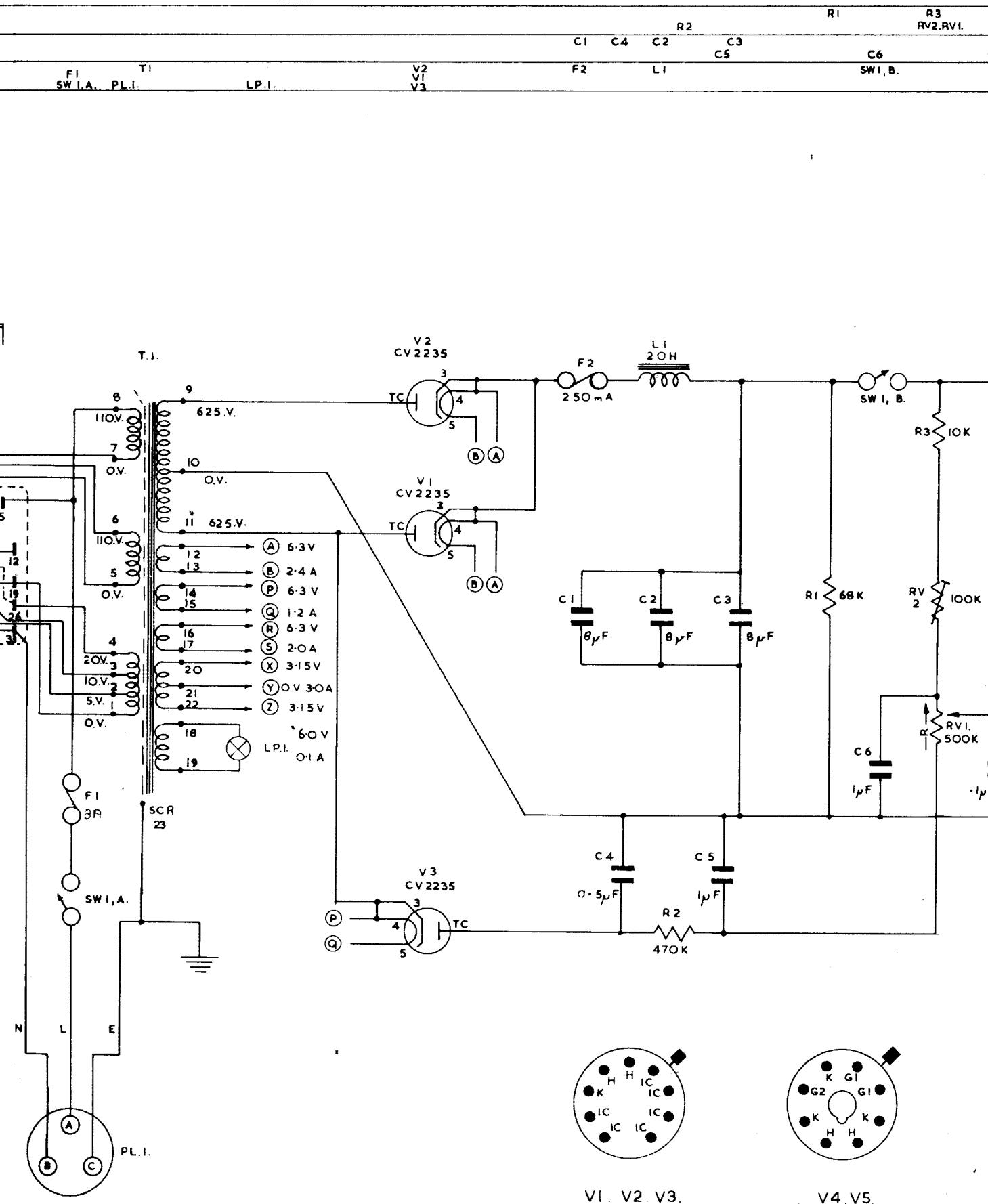


Fig. 5

Circuit Diagram

R3 RV2.RV1.	R6	R5 R4 R7	R9 R8 R10 R11 R12	R13
C8		C 7	V 5	M I
V 4				S W 2
				T L 1 - 6

