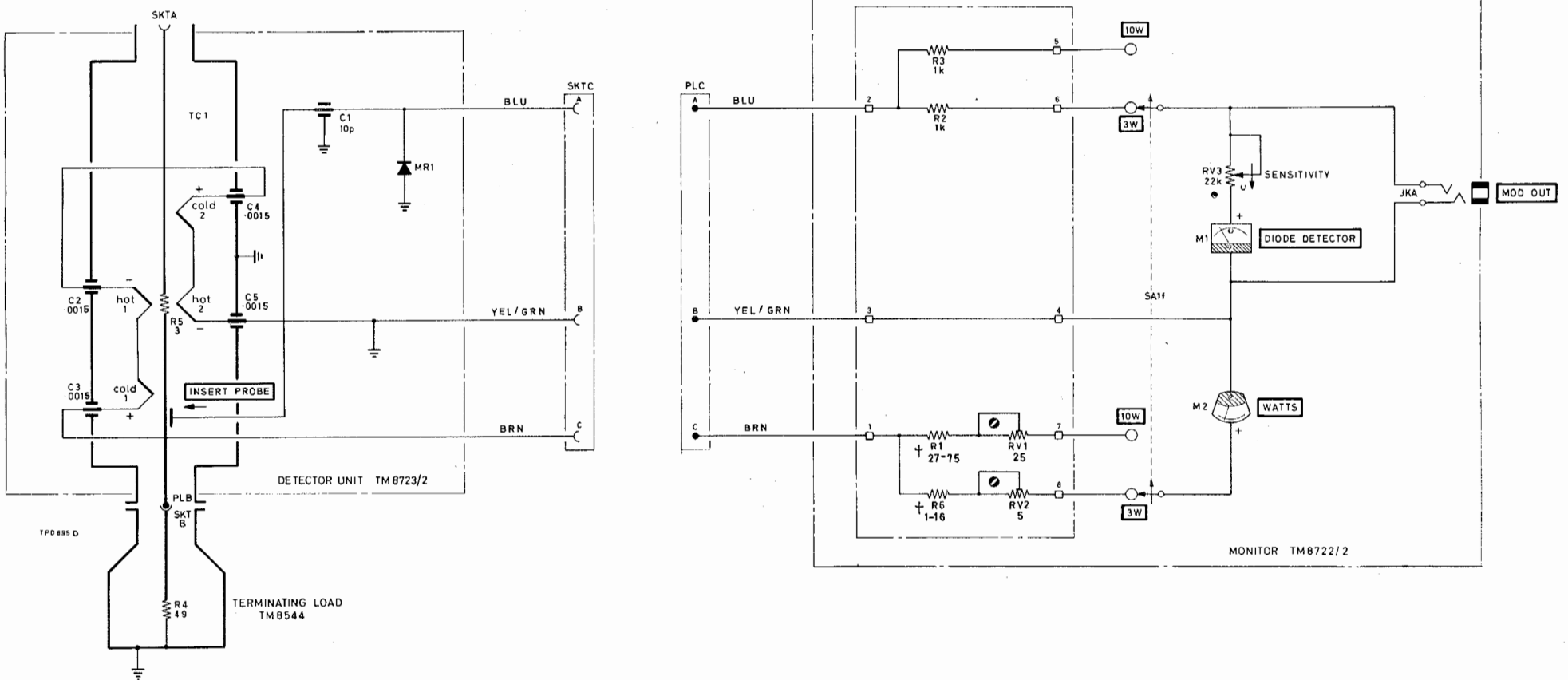

Fig. 7.1 Circuit diagram