Printed: JUN. 1968

—TR—3788C

FREQUENCY COUNTER

INSTRUCTION MANUAL

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PRINTED IN JAPAN

Table of Contents

1. DESCRIPTION

1.1 General

This instruction manual covers the specifications, operating procedure, theory, and maintenance of the -TR-3788C FREQUENCY COUNTER.

1.	DESCRIPTION	A description of the counter and its features.
2.	SPECIFICATIONS	A detailed description of the counter's functions and specifications.
3.	OPERATING PROCEDURE	Preparation and precautions prior to operating the counter, panel description (with the aid of illustrations), associated equipment and their connection, and operating procedures.
4.	THEORY OF OPERATION	Principles of construction centered around block diagrams, theory of basic circuits, etc. (with the aid of diagrams).
5.	MAINTENANCE AND INSPECTION	Instruments necessary for maintenance and inspection and troubleshooting procedures if malfunctions should occur. The circuit diagrams and parts list at the end of this section should be referred to during troubleshooting, maintenance, and inspection.

The -TR-3788C FREQUENCY COUNTER is completely transistorized, compact, and lightweight frequency counting equipment capable of frequency measurement in the 10 Hz ~ 500 MHz range. Up until now, measurements in the 500 MHz frequency band required a frequency converter or other similar equipment; however, this requirement does not exist with this counter (direct display of the count is possible).

Since the counter possesses a function which permits variation of the input level as desired, frequency measurement is possible even if the level of the measured signal varies. A specifl feature of this counter is the high reliability of its crystal oscillator. The oscillator has a stability of 3×10^{-9}/day under aging conditions and is installed in the counter only after subjection to various severe tests and aging data checked against a strictly managed standard frequency, as well as exhaustive quality control.

The operation of these counters is fast, simple, and accurate. Measurement is automatically performed and the measured result displayed in bright, clear digits.

The -TR-3788C employs TAKEDA RIKEN's original memory display system and its rationally designed controls and automatic switching of the units and decimal point by means of a switch make it extremely easy to use. In addition, the use of all silicon semiconductor components and integrated circuits not only facilitates maintenance and inspection but also makes the counter highly resistant to such ambient conditions as humidity, temperature and external noise.

The major features of the -TR-3788C ELECTRONIC COUNTER are as follows:

a) Frequency measurement up to 500 MHz.

b) 8 digit decimal numerical display tube registration.

c) Gate times of 4 mS, 40 mS, 0.4 S, and 4 S.

d) Internal time base frequency having extremely high accuracy (better than 3×10^{-9}/day).

e) Memory display possible by means of simple switch operation.

f) Units display and decimal point automatically set by ganging to various switches.

g) Small, lightweight.

2. SPECIFICATIONS

2.1 Specifications

Measuring system	Prescaler, direct reading decimal display system
Frequency measurement (Input)	
Measuring range	10 Hz ~ 500 MHz
Gate time	4 mS, 40 mS, 0.4 S, 4 S
Accuracy	$\pm \frac{1}{f.G} \pm$ internal time base accuracy (f: measured frequency, G: Gate time)
Read in	kHz, MHz Decimal point automatically set when gate time switched.
Min. read in frequency	1 kHz, 100 Hz, 10 Hz, 1 Hz
Signal input	Front panel BNC connector
Time Base	
Internal time base frequency	1 MHz
Frequency stability	3×10^{-9}/day (constant ambient conditions, after 48 hours of continuous operation)
Time base adjustment	Rear panel adjustment Adjustable range: 5×10^{-8}
Internal time base output	
Frequency	1 MHz
Output level	1 Vp-p ~ 6 Vp-p (unloaded)
Output impedance	Below 1 kΩ
Connectors	BNC type (rear panel)
Signal stability	Corresponds to internal time base accuracy

External time base input

Frequency	1 MHz
Input voltage	1 Vrms ~ 10 Vrms
Input impedance	Greater than 10 kΩ
Connectors	BNC type (rear panel)

General specifications

Counting capacity	8-digit decimal
Counting speed	500MHz, 2 nS resolution
Display system	Numerical display tube registration Count display and memory display (can be switched at the rear panel)

Display time

Count display	Min. longer than 80 mS, max longer than 5 S. Continuously variable and infinite.
Memory display	(Count display time + gate time) and infinite
Infinite	Measurement made once and continuously displayed until manually reset

INPUT

Input level	Level continuously variable
Input mode	AC
Input impedance	Approximately 50 Ω
Max. input sensitivity	100mVrms (10 Hz ~ 100 Hz) 10 mVrms (100 Hz ~ 500 MHz)
Trigger level variation range	±15 mV
Max. input voltage	2 Vrms
Safe input voltage	±2 V
Pulse input	Resolution 2 nS, sensitivity ±50 mVp

Self-check	The time base circuit, counting circuit, and various gates can be checked at a count (gate) time of 0.4 S and 1 MHz internal time base.
Operating temperature range	0°C ~ +40°C
Storage temperature range	-20°C ~ +70°C
Power supply	
Voltage	220 VAC, ±10%, 50/60 Hz Can be modified for 100, 115, 230 V (optional)
Power	Approx 65 VA
Insulation resistance	Between one AC input terminal and case Greater than 50 MΩ (100 VDC)
Dimensions	Approx 250 (wide) x 149 (high) x 345 (deep) mm (Does not include stand, rubber feet at the rear panel, and front panel cover)
Front panel cover	Approx 250 (wide) x 149 (high) x 93 (deep) mm

2.2 Components

The -TR-3788C consists of the following components:

1)	-TR-3788C FREQUENCY COUNTER	1
2)	AC power cord	1
3)	Input cable	2
4)	Ground cable	1
5)	Tubular glass fuse (1 A)	3
6)	Screwdriver (3 mm)	1
7)	Allen wrench (3 mm, 4 mm)	2 each

8)	Instruction manual	2
9)	Test report	2
10)	Attenuater (20 dB)	1

3. OPERATING PROCEDURE

3.1 General

This section covers preparations and precautions prior to operating the counter, panel description (with the aid of illustrations), and operating procedure.

3.2 General Preparations and Notes

1) Use an AC power source within the rated 220 V ±10%.
2) Since a ventilation fan is not employed, pay careful attention to ambient air flow.
3) Ambient operating temperature range is 0°C ~ 40°C.
4) Absolute storage temperature range is -20°C ~ +70°C.
5) Since a crystal oscillating element is employed, do not subject the counter to extreme mechanical shock. Handle the counter carefully.
6) If considerable power line noise is present, use a noise filter.
7) Since the internal signal may leak out, ground the counter.
8) When highly accurate measurements are necessary, calibrate the internal crystal oscillator. (Refer to the precautions pertaining to maintenance of TAKEDA RIKEN Counters)
9) All functions begin to operate as soon as power is applied.
10) The constant temperature oven heater operates, even if the power switch is turned off, unless the power cord is unplugged. (Since 48 hours after the OVEN heater is set to ON is required before the crystal oscillator reaches its rated stability. It is recommended that the power cord remain connected when making highly accurate measurements over a long period of time.

3.3 Panel Description (Refer to Fig. 3.1.)

-Front Panel-

1) GATE IND

This neon tube indicates the opening and closing of the gate. The lamp lights when the gate opens.

2) SAMPLE RATE

a) The time between counting operations can be varied from 80 mS to more than 5 S by turning this control clockwise.

b) Manual counting can be performed by depressing the RESET button (4) with this button set to HOLD.

3) POWER - OFF

Controls the power to all circuits except the OVEN heater of the crystal oscillator. Power is applied when this switch is set to the POWER side and removed when set to the OFF side.

4) RESET

The primary counting circuit and time base are set to the zero state and counting operation immediately performed at the next GATE signal when this button is depressed.

5) GATE TIME

Switches the counting time when making frequency measurements or performing the CHECK operation. When set to CHECK, the counting time is constant at 0.4 A. When making frequency measurements, this control is used to select the desired gate time (4 mS, 40 mS, 0.4 S, or 4 S can be selected).

6) PROBE POWER

Power supply connection when using a high input impedance probe. The input impedance of INPUT is 1 MΩ.

7) INPUT

Input terminal for frequency measurement.

8) LEVEL

Varies the input signal trigger level. Its variation range is ±15 mV.

-Rear Panel-

9) NON-STORAGE/STORAGE

When this switch is set to STORAGE, the count display is accumulated and the previous counted results continuously displayed up to the end of the next counting operation. Only those digits of the previous display which differ from the results of the following count change.
When set to NON-STORAGE, the accumulating function is lost. The displayed results are reset to "0" prior to initiation of the next counting operation, and the next counting operation performed.
When reading the counted results and this switch is set to STORAGE, SAMPLE RATE is turned fully counterclockwise.
When set to NON-STORAGE, set SAMPLE RATE to a middle position and then make the reading.

10) GROUND

Ground terminal for the counter case, when external noise, induction, etc. are considerable, connect this terminal to an earth ground with the cables supplied.

11) FREQ STD ADJ

This screw is used to adjust the internal time base (crystal oscillator).

12) EXT and INT

When set to INT, all the gate functions are performed by the crystal oscillator housed inside the counter. At this time, a 1 MHz time base signal appears at terminal (13). When set to EXT, the gate functions of the internal crystal oscillator are lost. The gate functions are performed by applying an external time base signal (1 MHz) to terminal (13).

13)

14) FUSE 1 A

Power fuse for the counter. A 1 A fuse is required.

15) AC 220V

AC power connector. Rated power is 220 VAC ±10%, 50/60 Hz. The counter can be modified for use with 100, 115, or 230 VAC by changing the internal connections.

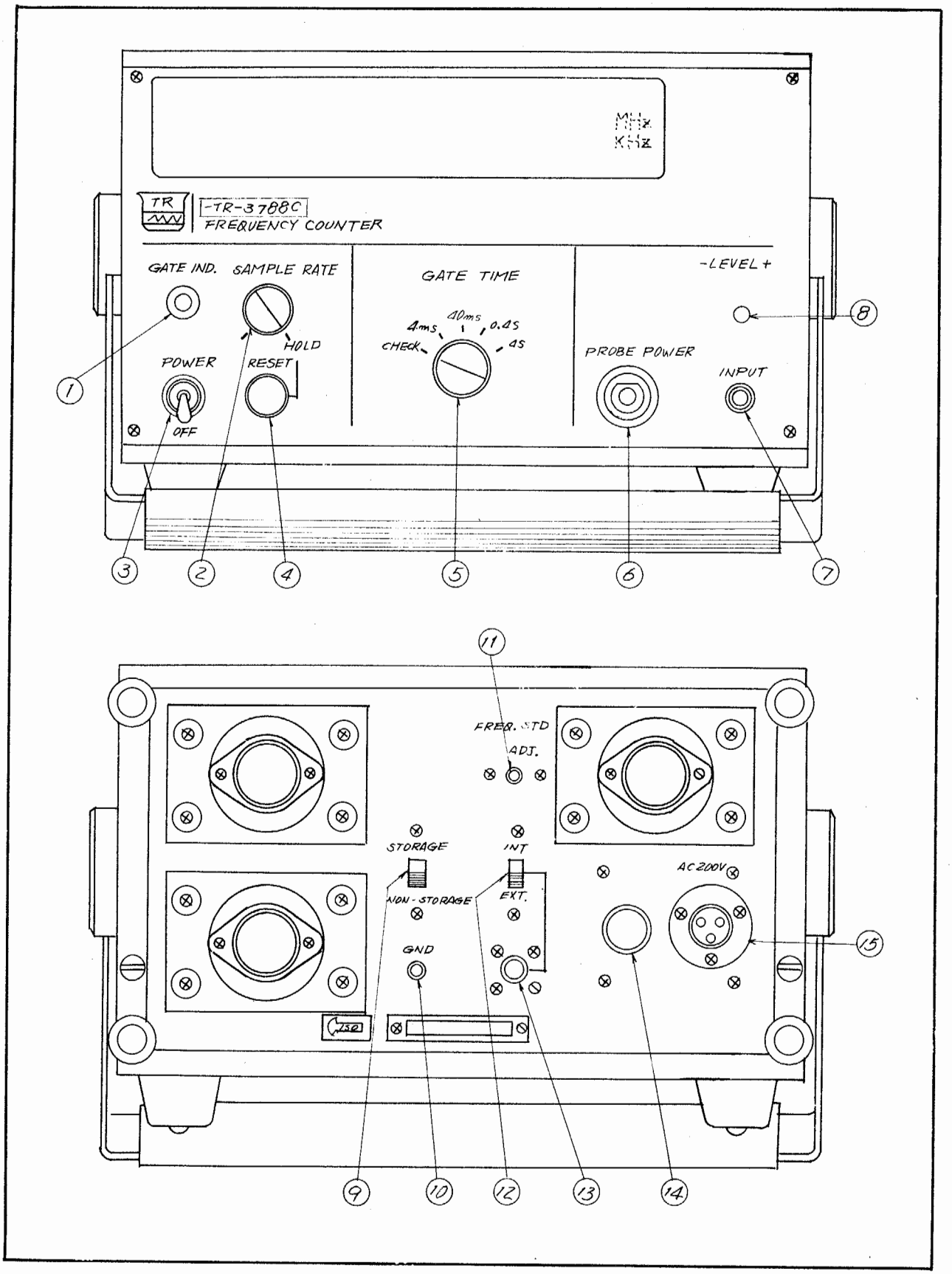


Fig. 3.1 Panel description

3.4 Self-Check Operation

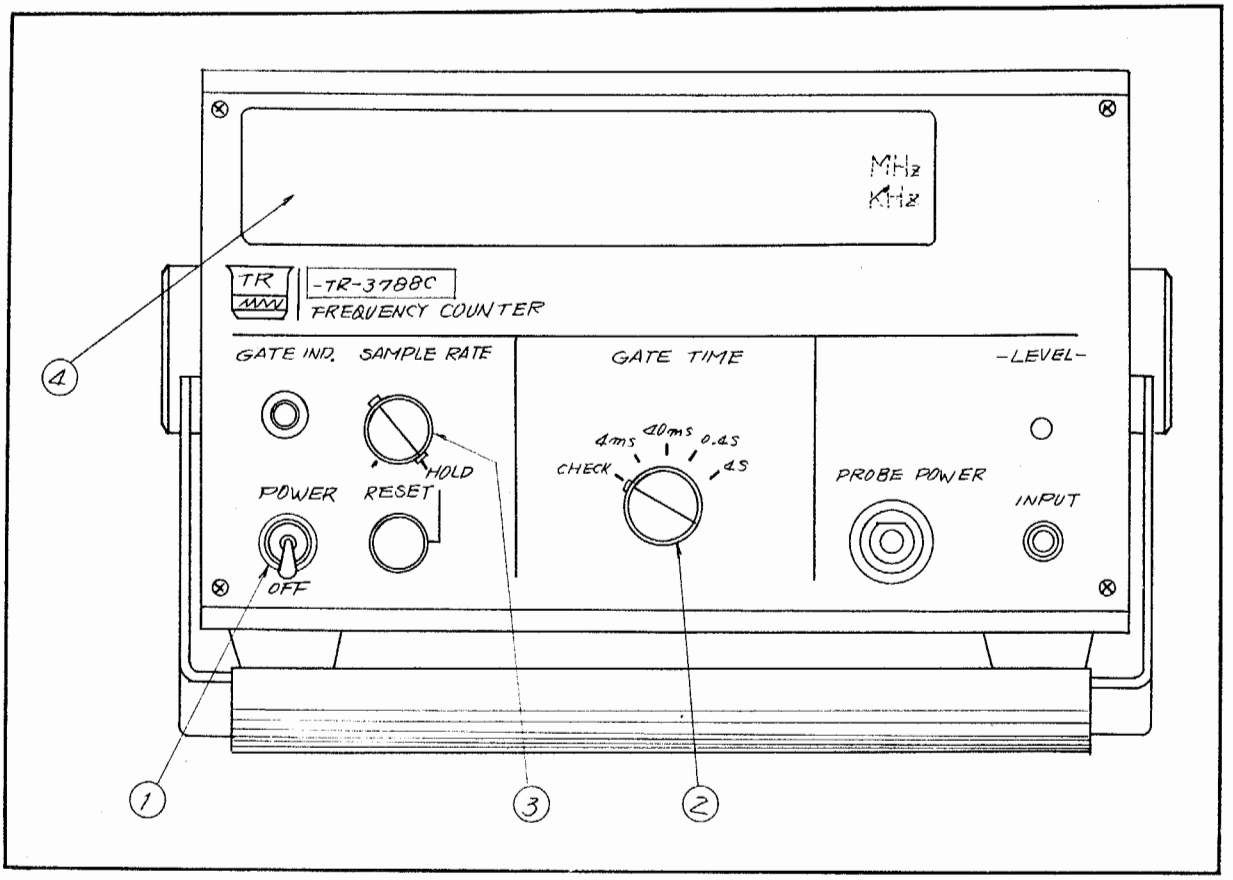


Fig. 3.2 Self-check operation

Conduct the self-check operation by referring to the numbers in Fig. 3.2 and those below.

(1) Set POWER - OFF to OFF.

NOTE: Connect the power cord to the AC connector only after confirming that the POWER switch is set to OFF.

Pay careful attention to power cord to the power supply voltage; the rated value is 220 VAC ±10%, 50/60 Hz.

(2) Set GATE TIME to CHECK.

(3) Turn SAMPLE RATE fully counterclockwise.

At this time, set STORAGE/NON-STORAGE at the rear panel to STORAGE.

(4) Check to see if the displayed value is 001000.00 kHz or not.

(5) Change STORAGE/NON-STORAGE at the rear panel and check if the display value changes or not.

3.5 Frequency Measurement

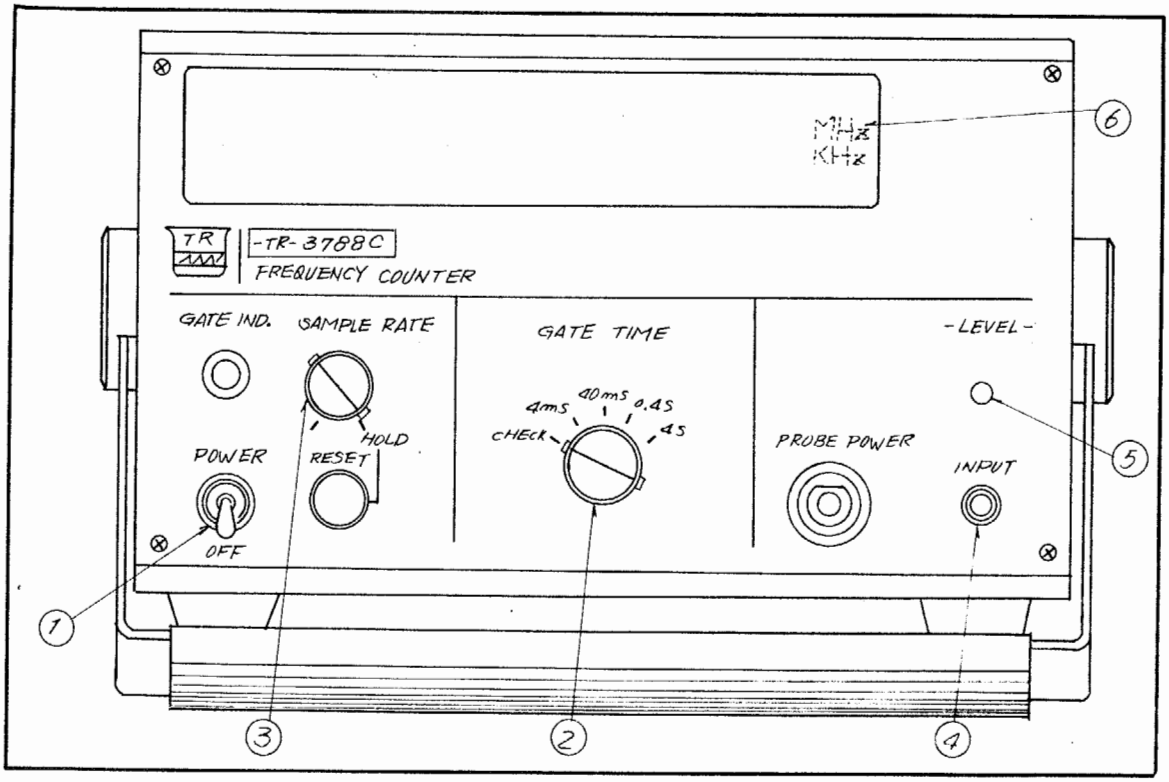


Fig. 3.3 Frequency measurement

Conduct frequency measurement by referring to the numbers in Fig. 3.3 and those listed below.

1) Set POWER - OFF to POWER.

NOTE 1: Connect the power cord to the AC connector only after confirming that POWER - OFF is set to OFF.

2: Pay careful attention to the power supply voltage. The rated value is 220 VAC ±10%, 50/60 Hz.

2) Set GATE TIME to 0.4 A.

Set STORAGE/NON-STORAGE at the rear panel to STORAGE.

3)

4) Apply the signal to be measured to the INPUT terminal.

NOTE: Apply the input signal only confirming that it is within the rated value of 10 mV ~ 2 Vrms.

5) Adjust LEVEL (8) in accordance with the waveform. When the waveform is a pulse, adjust the level to correspond to its polarity.

When it is a dc signal, operation will be performed if the level is set to a nearly middle position; however, there are times when the operating point will be changed a little by noise, waveform distortion, etc.

6) Read the counted value. The decimal point position is kHz or MHz units. Measurement accuracy will be increased 10 times if GATE TIME is set to 4 S.

When GATE TIME is set to 0.4 mS, measurement accuracy is low but measuring speed fast. When STORAGE/NON-STORAGE switch is set to NON-STORAGE, make measurements by turning SAMPLE RATE fully clockwise.

When making highly accurate measurements, set INT - EXT at the rear panel to EXT and apply a highly accurate 1 MHz external clock signal to the terminal.

3.6 Guaranteed Measurement Accuracy and Product Quality

Generally, there are two factors which limit the measurement accuracy of frequency counters. One is the accuracy of the 1 MHz crystal oscillator used to produce the internal time base (in the case of the -TR-3788C this is $\pm 3 \times 10^{-9}$/day) and the other the inherent ±1 count error of counter systems.

Measurement error due to the crystal oscillator accuracy can be reduced to a small value; however, the ±1 count error is caused by the comparative phase relationship between the measured signal and the gate time and is an error inherent in counter systems. (Refer to 4.3.)

The relationship between the measured signal and measurement accuracy is shown in Fig. 3.4 (for the -TR-3788C).

Measurement accuracy in frequency measurement is expressed by the following formula:

$$\text{Measurement accuracy} = \pm \frac{1}{f \cdot G} \pm \text{internal time base accuracy}$$

where: f = measured frequency

G = Gate time

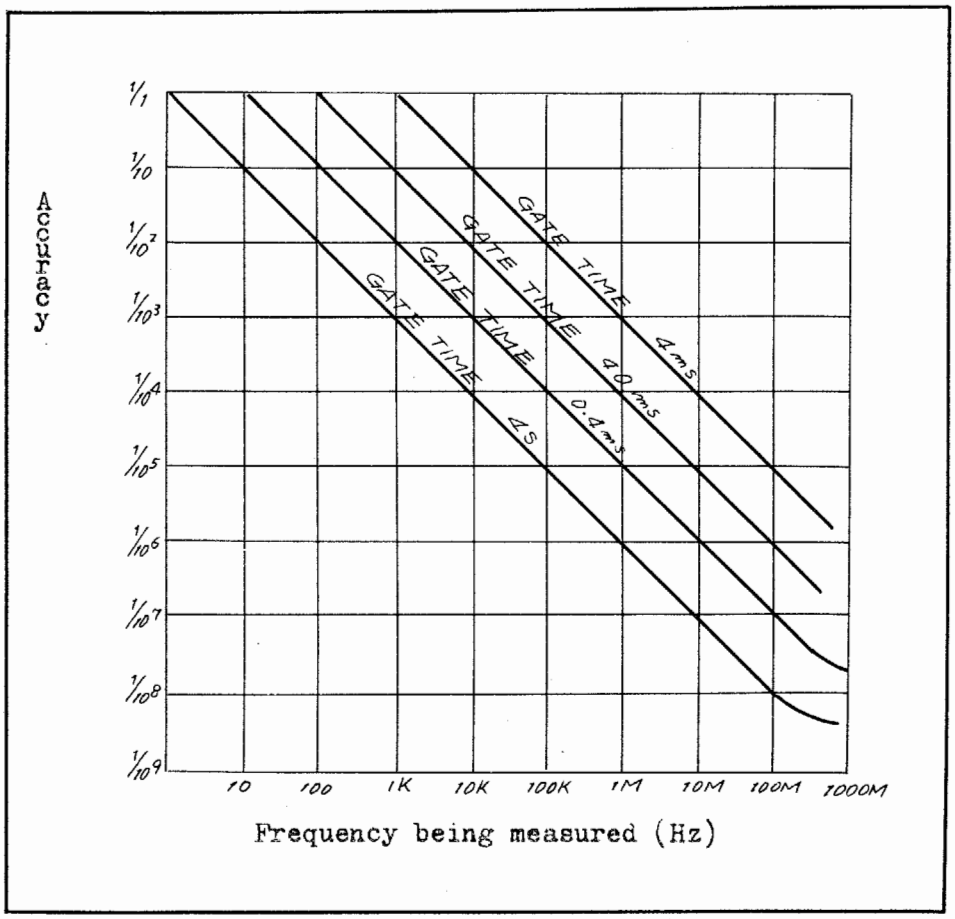


Fig. 3.4 Frequency measurement accuracy (typical characteristics)

The accuracy of -TR-3788C frequency measurements gradually deteriorates in the neighborhood of approximately 100 MHz. When the measured frequency reaches a certain high frequency, the $\pm 1/f \cdot G$ in the formula in section 1 can be almost completely disregarded; however, the accuracy of the internal time base has a considerable affect on the counted results. Therefore, since the -TR-3788C has an accuracy of 3×10^{-9}, accuracy cannot be greater than 3×10^{-9} even at a 4 S GATE TIME.

High measurement accuracy can be obtained in high frequency measurements by using an internal time base (crystal oscillator) having high accuracy. At TAKEDA RIKEN, the accuracy of the internal time base of all digital counter series is guaranteed by an atomic standard frequency using the resonant frequency of cesium atoms.

Highly accurate frequency standards are emitted as general radio waves as national standards.

The national standard in Japan is JJY whose accuracy is maintained to within 3×10^{-9}. Moreover, if astronomical time is demanded of the standard, accuracy becomes $1 \times 10^{-7} \sim 1 \times 10^{-8}$ due to multiple transmission paths, doppler effect, and fading. The TAKEDA RIKEN cesium atom frequency standard has a permanent stability of $\pm 1 \times 10^{-11}$ and an absolute cesium time accuracy of $\pm 1 \times 10^{-10}$. This standard is used as a primary standard to guarantee the accuracy of the crystal oscillator used as a secondary standard to guarantee the accuracy of the internal time base of digital counters.

4. THEORY OF OPERATION

4.1 Basic Theory

Electronic counters generally have the basic construction shown in Fig. 4.1.

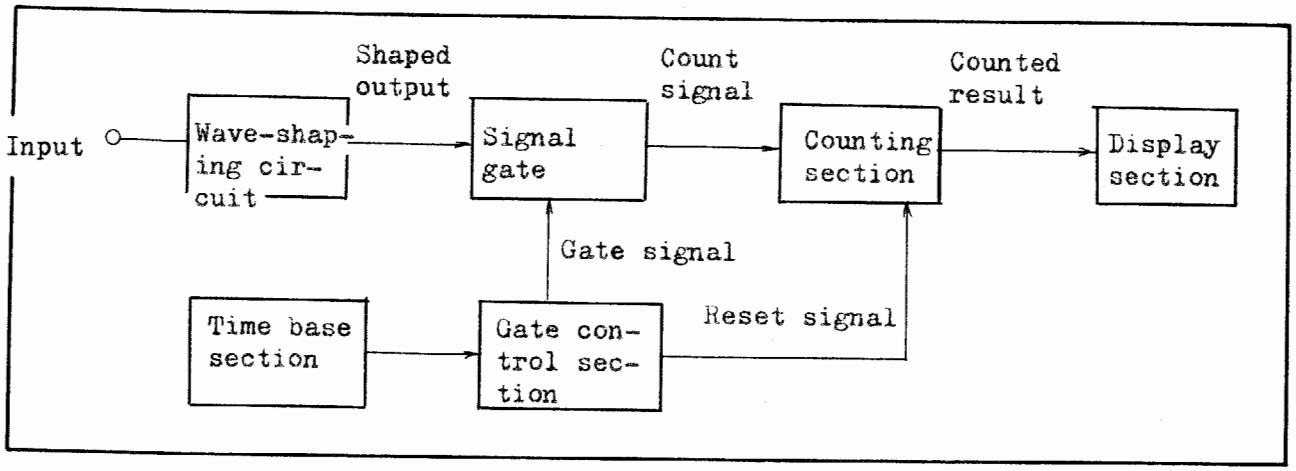


Fig. 4.1 Basic electronic counter construction

The input signal is shaped into a signal having a constant waveform, passed through the signal gate at a set time (count time), counted by the counting section, and the counted result displayed. This relationship is shown in Fig. 4.2. The 100 Hz, 10 Hz, and 1 Hz gate signal (counting signals) are obtained by dividing the accurate 1 MHz from the internal time base crystal oscillator by 10:1, 100:1, etc. and opens/closes the signal gate by controlling the gate control section with these signals.

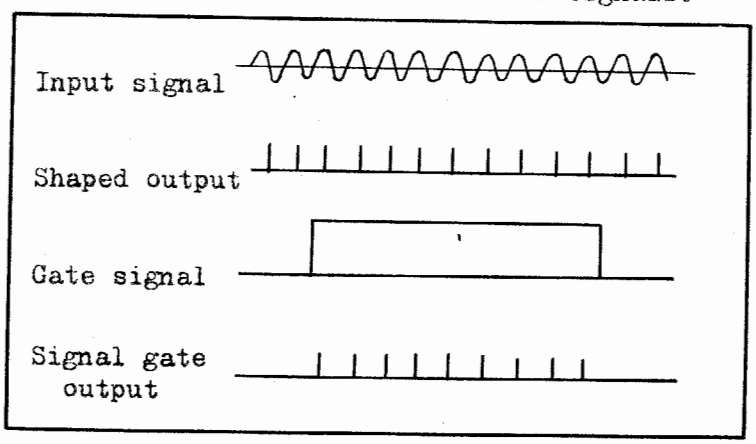


Fig. 4.2 Time chart

The 500 MHz input frequency is reduced to 125 MHz by dividing it by 4 and the 125 MHz then employed in the decimal counting circuit.

The counted results are not displayed as 1.4, even though the input frequency is divided by 4. Direct readout of the frequency is obtained by multiplying the counting time by 4.

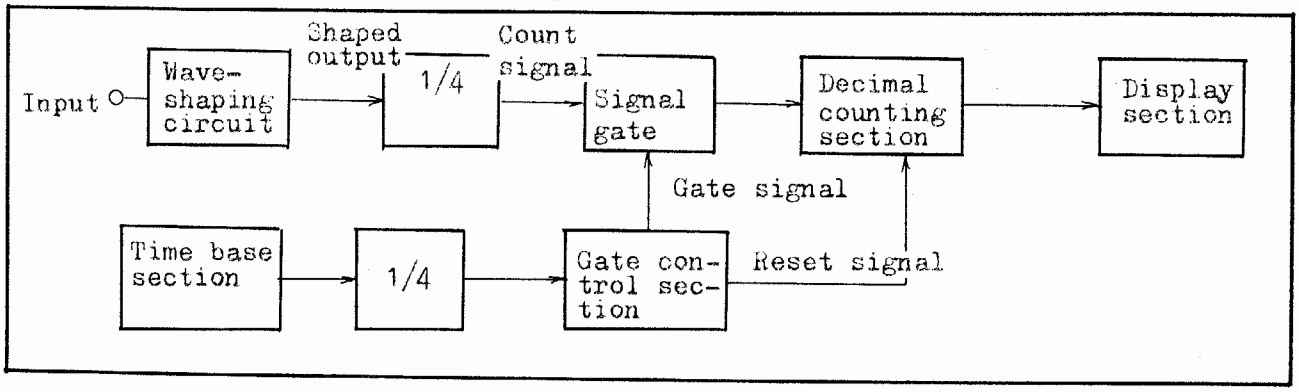


Fig. 4.3 Basic construction of the -TR-3788C

At this time, the clock signals are 25 Hz, 2.5 Hz, and 0.25 Hz in respect to 100 Hz, 10 Hz, and 1 Hz.

The operation cycle is; the gate opens once, the count is made, the counted value is fed to the display section, and all circuits except the display section then reset and returned to the next measurement state. The repetition speed of this operation is varied by adjusting SAMPLE RATE on the panel. Both automatic and manual sampling are possible.

4.2 Frequency Measurement

The accurate 1 MHz signal from the crystal oscillator is amplified, shaped, and then divided by the divider to product the clock signal.

The accurate 4 mS (250 Hz), 40 mS (25 Hz), 0,4 S (2.5 Hz), and 4 S (0.25 Hz) clock signals produced in this manner are selected by means GATE TIME on the front panel, fed to the counting control circuit as the gate time, and used to control the opening/closing of the signal gate.

The signal to be measured is applied to the INPUT terminal on the other panel, amplified, shaped, and fed to the signal gate. The signal is then fed to the counting circuit (SCALER) only during the count time selected at GATE TIME. The counted result is displayed simultaneously with counting.

When the gate is closed, the gate signal is fed to the sample rate control circuit. This circuit is delayed by this signal for the desired period of time selected by means of SAMPLE RATE on the panel. A different date signal is fed to the gate control circuit to open the gate.

The above has been a description of this counter's automatic sampling operation at the same time the gate opening signal is produced, all circuits are reset and the next count performed. During memory display (set to STORAGE), the previously counted value is continuously displayed during the next count operation. The results of the next counting operation are then displayed after the gate closes and the count completed. In this process, only those digits of the following counted results which differ from the display of the previous count changed. The display does not flicker but remains steady.

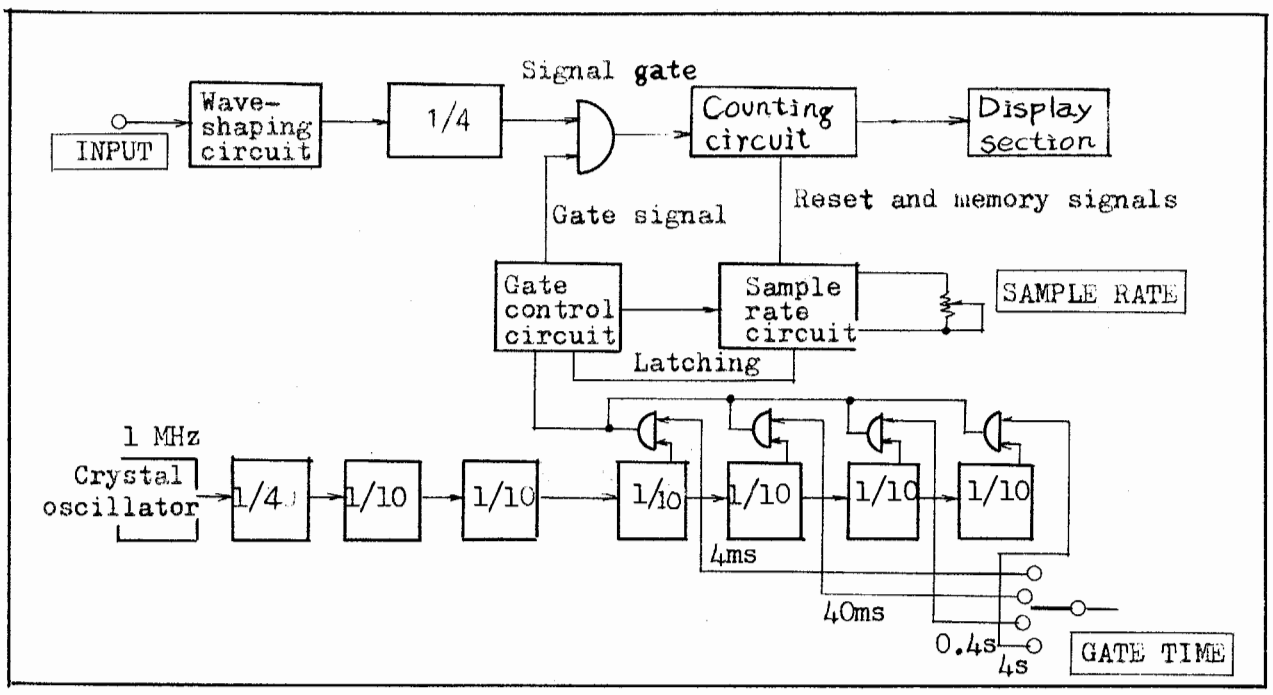


Fig. 4.4 Block diagram of frequency measurement

4.3 Frequency Measurement Accuracy

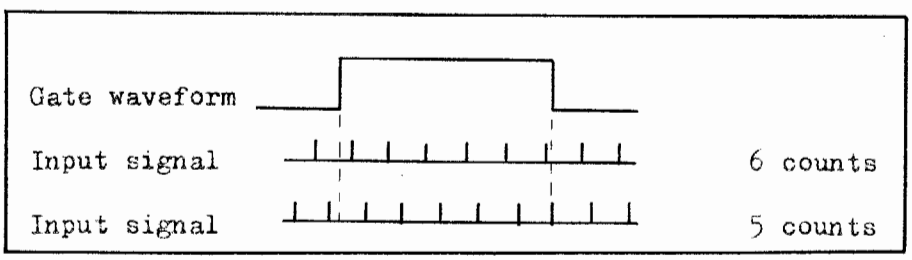
Frequency measurement accuracy is determined by the ±1 count error inherent in the digital system and the accuracy of the internal time base.

Error is also generated when noise is included in the signal; however, when making frequency measurements by counting the input signal pulse pulses, error will not occur if the noise is lower than the trigger level (input sensitivity). Frequency measurement accuracy can be obtained with the following formula when the gate time is added.

$$\text{Frequency measurement accuracy} = \frac{1}{\text{full count}} \pm \text{internal time base accuracy}$$

However, the full count is [Measured frequency x gate time].

The ±1 count error inherent in digital systems cannot be avoided, and is caused by the increase or decrease of the full count by 1 count due to the phase relationship between the signal pulse (measured signal after shaping) and the gate waveform as shown in Fig. 4.5.



When conditions are as shown in Fig. 4.5, the count should be 5.7 if measured with an analog system; however, due to the inherent quantization in the digital system, the 0.7 component will be either discarded or raised and the count will become either 5 or 6.

The 1 MHz internal time base signal is obtained by means of a crystal oscillator. All of the internal time base times are produced from this signal. For this reason, since the 1 MHz output of the crystal oscillator is an important factor controlling the measurement accuracy of the counter, it is necessary to maintain it at a high accuracy. Therefore, timely calibration is necessary.

4.4 Self-Check

The 1 MHz crystal oscillator output is amplified, shaped, and fed to the divider to produce the 250 kHz, 25 kHz ... 2.5 Hz, and 0.2 Hz clock signals.

The 0.4 S (2.5 Hz) clock signal produced in this manner becomes the signal which opens/closes the gate. The signal pulse of the measured signal is fed to the counting section only when this signal is present. At this time, if the clock signal is applied instead of the signal to-be-measured, the counted results can be anticipated if the gate time is set because the time or frequency of the gate time and counted signal are known.

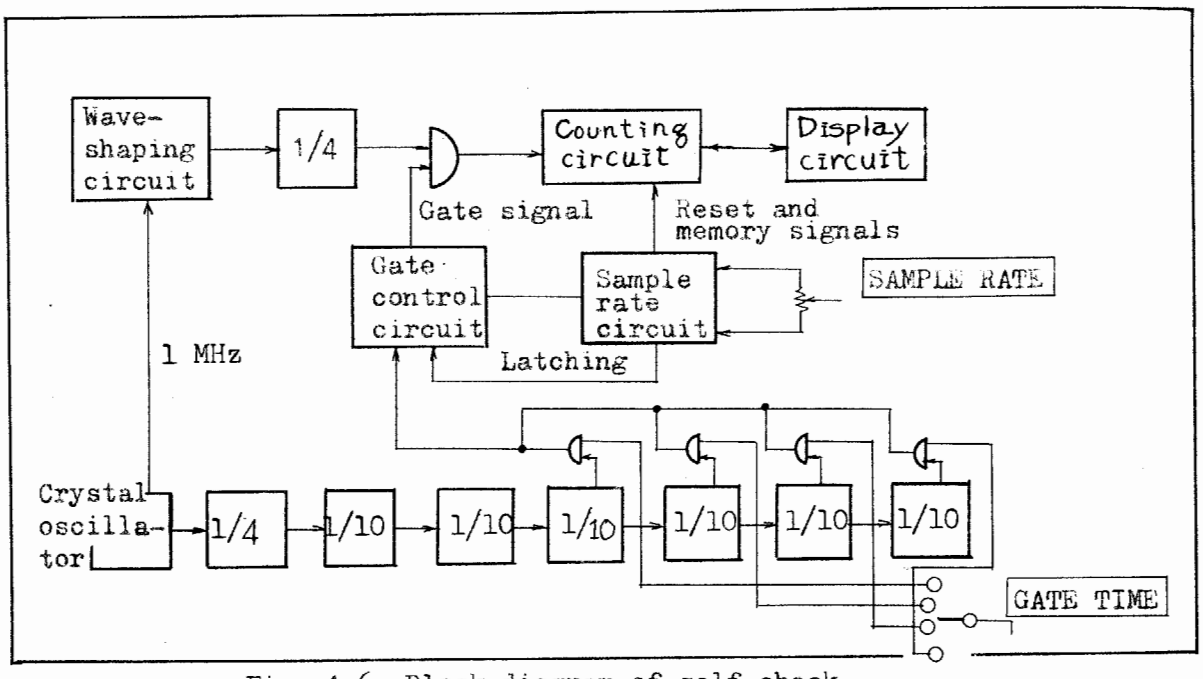


Fig. 4.6 Block diagram of self-check

4.5 Active Elements and Their Construction

The basic circuit construction of the counter will be described by describing the active elements. This will make it easier to fully understand its theory of operation and circuit construction.

This counter employs all semiconductor components as active elements. Various semiconductor diode and transistors, as well as integrated circuits, are employed in the counter.

(A) Diodes

Semiconductor diodes are employed in the counter for power supply recrification and constant voltage applications, as well as in various gate circuits, trigger circuits, clamping circuits, and wave-shaping circuits. Typical examples of their use in gate circuits, trigger circuits, and constant voltage circuits will be given here.

Refer to (B) for information concerning wave-shaping circuits. Fig. 4.7 is a typical gate circuit.

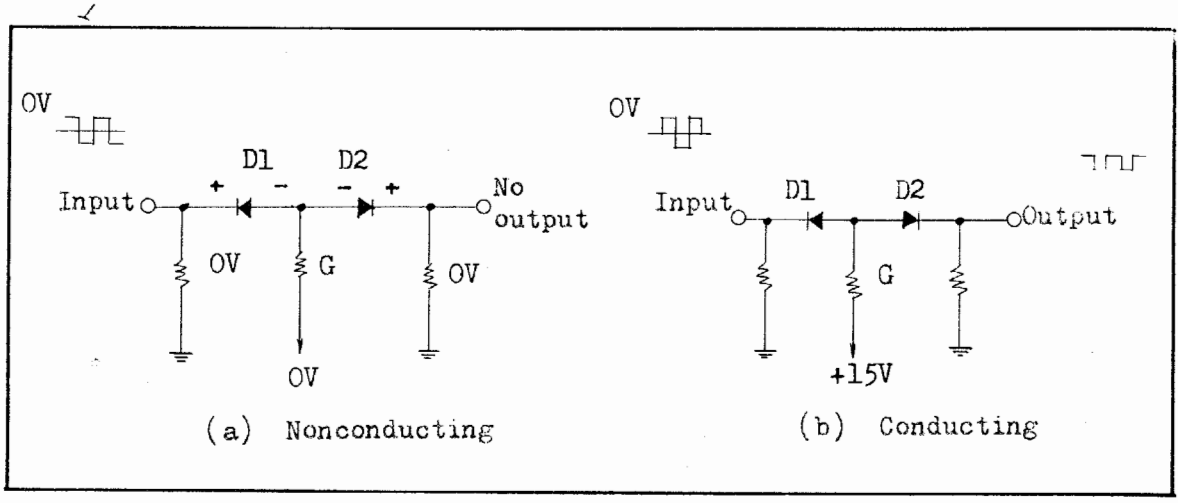


Fig. 4.7 Typical gate circuit

When point G in Fig. 4.7 (a) is 0 V (ground), D1 is in the conducting state (ON) in respect to the input voltage load and D2 is not conducting (OFF). In respect to a positive input D1 is OFF (nonconducting) and no output appears at the output terminals. When point G is clamped at -15 V as shown in (b), there is a range of voltage at which D1 and D2 are both ON (conducting) and the input signal passes through.

A gate which opens and closes is formed by the circuit shown in Fig. 4.7. Since gate circuit controls the amplitude of the input signal, it is called a limiter (or clipper) circuit.

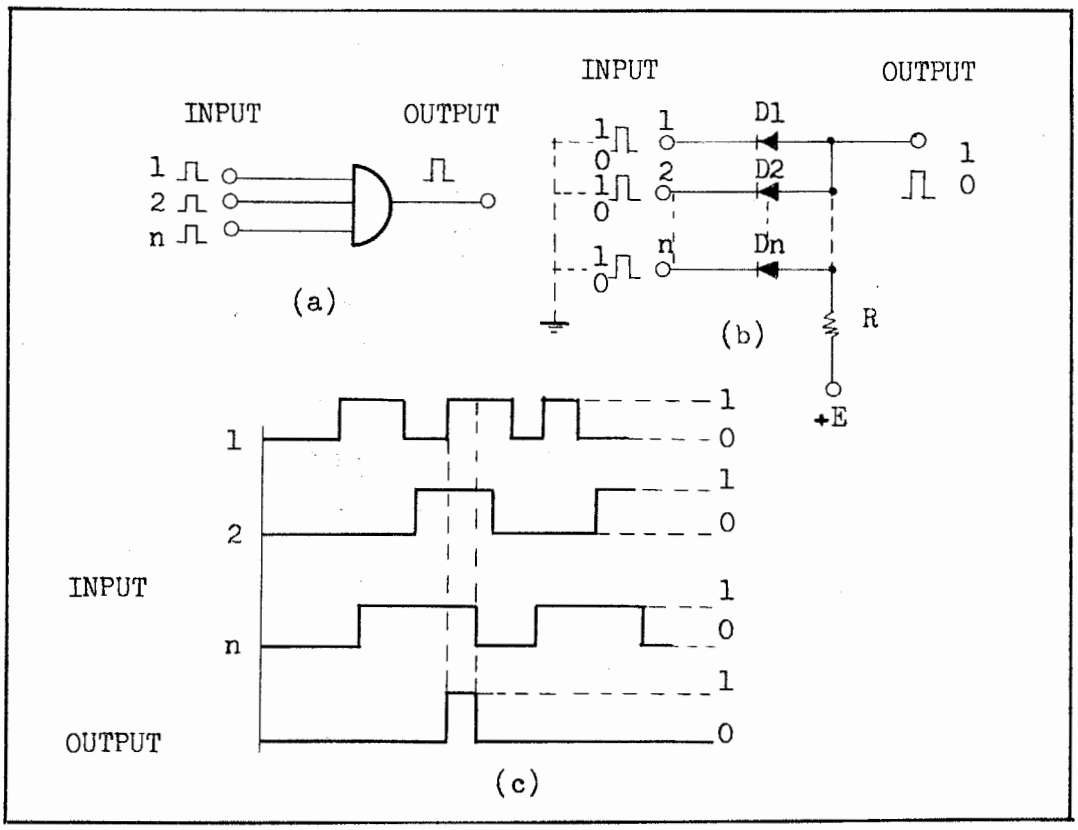


Fig. 4.8 Diode AND circuit

A circuit in which a "1" signal is generated at the output terminals only when there is a "1" (+ voltage) signal at 2 or n input terminals, as shown in Fig. 4.8, is called an AND circuit. The symbol generally used to denote and AND circuit is shown in (a). An example of an actual diode AND gate is shown in (b). Terminals 1, 2, ... n in the figure are grounded through the pulse source.

If a "0" (zero voltage) signal is simultaneously applied to terminals 1, 2, ... n, the dc source circuit is R → D1, D2, ... Dn → internal impedance of the pulse source, a positive bias is applied to the diodes and forward current flows.

If R is large compared to the impedance of the pulse source and the forward resistance of the diodes, OUTPUT is nearly at ground potential and an output does not appear.

When a "1" (+ voltage) is applied to INPUT, the diodes will conduct even if the "1" voltage is lower than +E; however, since the internal impedance of the pulse source is low, the OUTPUT will generally be almost the same as the INPUT voltage.

When the "1" voltage is greater than +E, the output will be +E regardless of the input voltage since the diodes are then cutoff.

Since output only appears when all the inputs are "1", this circuit is called an AND gate.

The waveforms of this circuit are shown in Fig. 4.8 (c).

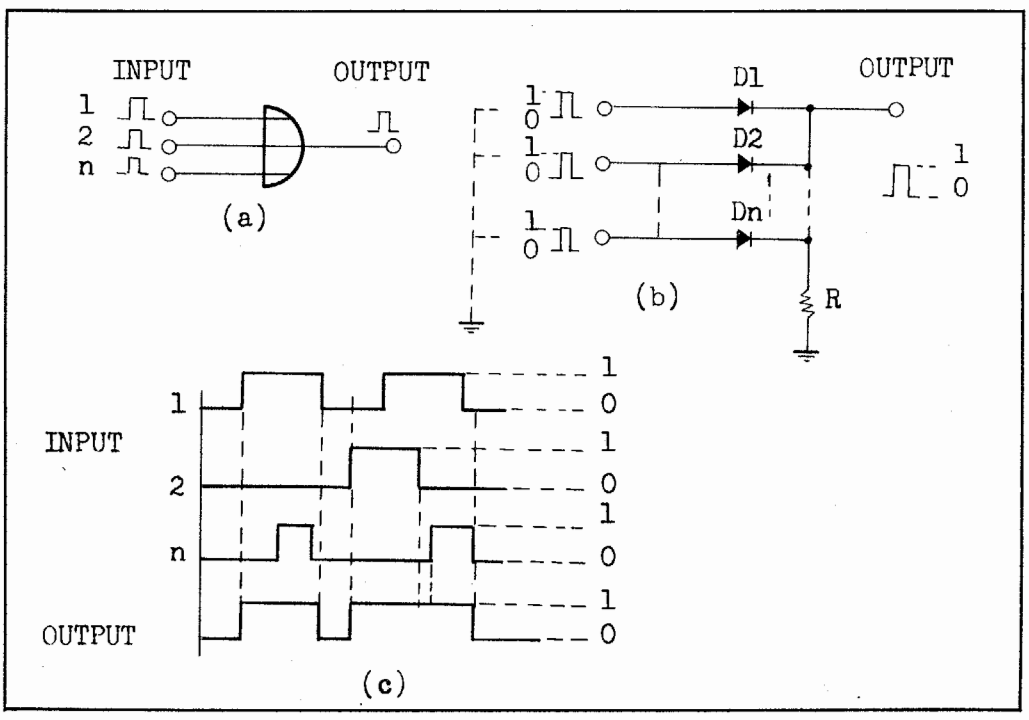


Fig. 4.9 Diode OR circuit

A diode OR circuit is shown in Fig. 4.9. The circuit in Fig. 4.9 is called an OR circuit because a "1" output is generated if a "1" signal is applied to any one of the input terminals (1, 2, or n).

The symbol generally used for the OR circuit is shown in Fig. 4.9 (a). An example of an actual OR circuit is shown in (b).

Terminals 1, 2, ... n in Fig. 4.9 (b) are grounded through the pulse source. When terminals 1, 2, ... n are all "0", the diodes are reversed biased and, since all the diodes are cutoff, an output does not appear at OUTPUT. If a "1" signal is applied to any one of the terminals, an output will appear at OUTPUT during the time that the signal is applied since that diode will be forward biased during the period the signal is applied. Since an output will appear at OUTPUT if a "1" signal is applied to any of the input terminals, this circuit is called an OR circuit. When a signal appears at the output terminal from one of the input terminals, the other terminals are not affected since all the terminals are independent.

Fig. 4.10 is a comparison of a limiter type differentiator circuit employing a diode and conventional RC differentiator circuit.

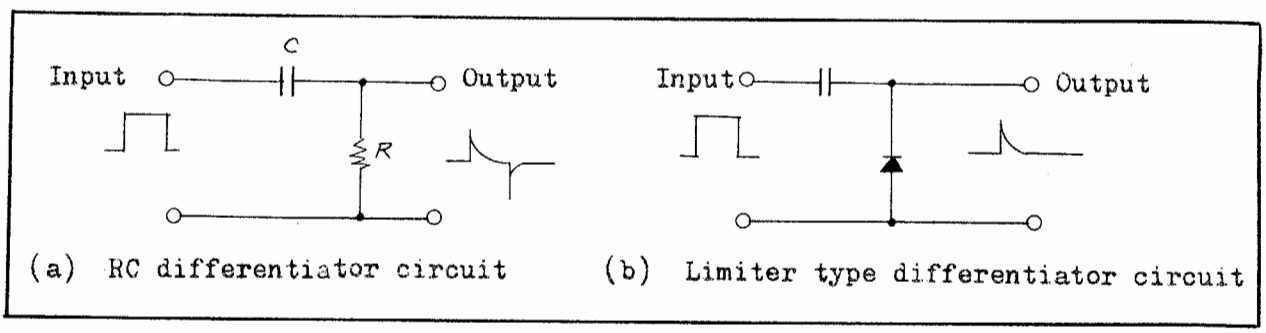


Fig. 4.10 Limiter circuit

When a square-wave is differentiated with a conventional RC differentiator circuit as shown in (a), positive and negative differentiated waveforms appear. This is not favorable for use in counters. When a diode is used as in (b), it is a limiter differentiator circuit and either the positive or negative waveform, whichever is unnecessary, is eliminated. Wide use is made of limiter differentiator circuits in this counter to prevent

erroneous counting and division in the counting circuits, dividing circuits, etc.

When a diode is used as a constant voltage circuit, both its forward voltage drop and its reverse zener voltage (zener diode) can be employed. A constant voltage circuit employing a zener diode is shown in Fig. 4. 11.

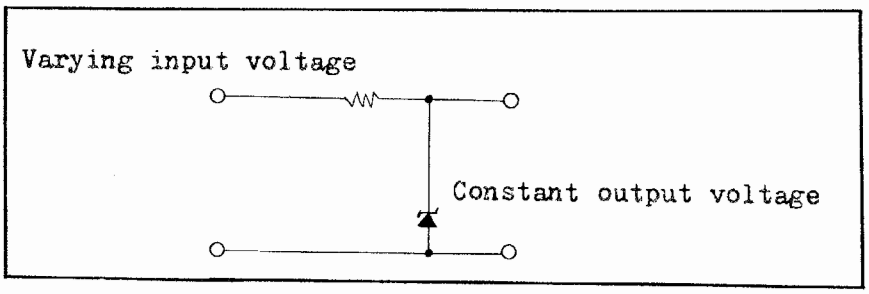


Fig. 4. 11 Constant voltage circuit employing a zener diode

The voltages of the various power supplied in this counter are made constant by a combination of zener diodes and transistors.

A circuit employing the forward direction of a diode is employed to make low voltages constant since voltages of 0.5 ~ 0.8 V can be obtained if a silicon diodes is used.

(B) Transistors

This counter employs various types of transistors in the wave-shaping circuit and as Schmitt circuits, flip-flop circuits, and amplifier circuits corresponding to the purpose of the circuit.

There are three basic transistor configurations, grounded emitter, grounded collector, and grounded base as shown in Fig. 4.12.

The features of these basic configurations are listed in Table 4.1.

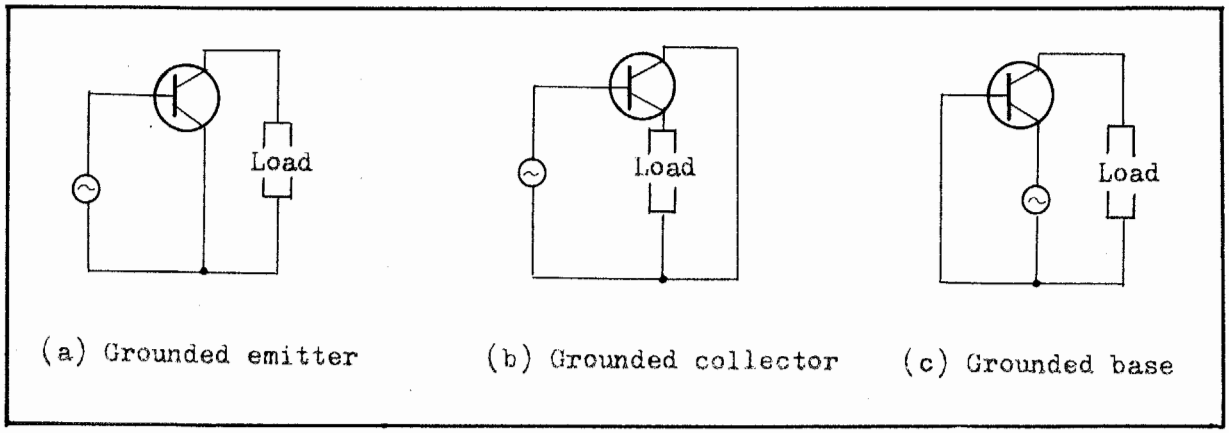


Fig. 4.1 Features of basic transistor configurations

Configuration	Input impedance	Output impedance	Voltage gain
Grounded emitter	Medium	Medium	High
Grounded collector	High	Low	None
Grounded base	Low	High	Medium

The above is for NPN type transistors; however, everything is the same for PNP type transistors except that current flow is in the reverse direction.
This counter employs the grounded emitter in the majority of circuits; only a very small portion employs the grounded collector.
The grounded collector has no voltage gain; however, since its input impedance is high and it output impedance low it is used as an impedance converter. This type of circuit is called an emitter follower.

1) Amplifier

Circuit board WA92 is a 10 Hz ~ 500 MHz wideband, fixed gain amplifier. For this reason, transistors having superb high frequency characteristics are employed.

2) Wave-shaping circuit

When counting, it is necessary to shape the input signal and other signals into a waveform having short raise and fall times in order to amplify, transfer, count, and divide them.

The wave-shaping circuit widely employed to accomplish this is the emitter coupled binary circuit. This circuit is called a Schmitt circuit after the inventor.

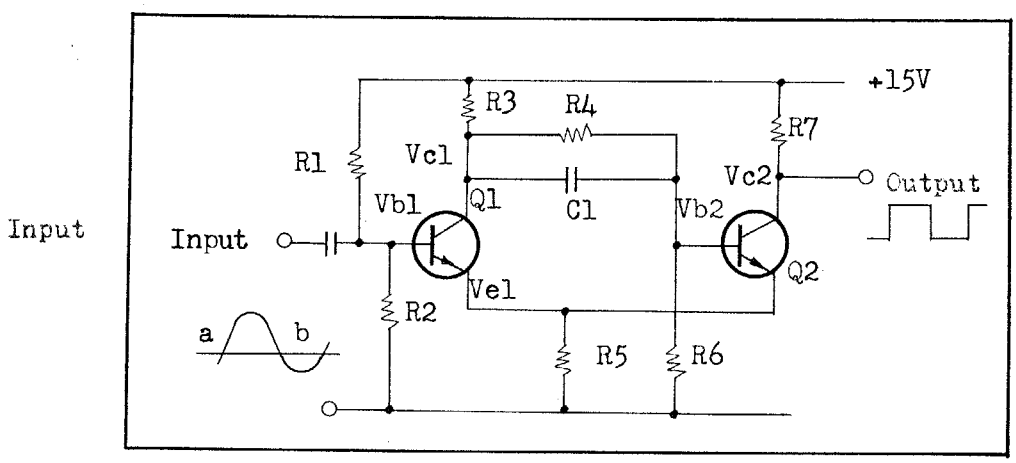


Fig. 4.13 Typical Schmitt circuit

An example of this circuit is shown in Fig. 4.13. If R1 and R2 are selected so that Q1 base voltage Vb1 is lower than the voltage drop across R5 (Q1 emitter voltage Ve1), bias voltage Vb1 will be applied.
This cuts off Q1. If R4 and R6 are large, Q1 collector voltage Vc1 will be almost equal to the +15 V supply voltage.
If R4 and R6 are selected so that Q2 base voltage Vb2 is slightly higher than Ve1, Q2 conducts (ON) and the output voltage at Q2 collector Vc2 will be almost proportional to the values of R5 and R7.

This stable state will continue (Q1 OFF and Q2 ON) until an input signal is applied. The input signal applied is shown in the figure. When the input signal is large (as shown by (a) in the figure), Bb1 exceeds Ve1 and Q1 conducts (ON state). In this state, Q1 current starts to flow, Vc1 drops, Vb2 rises, and Ve1 drops. The base to emitter voltage of Q1 becomes large, Vc1 steadily

drops, and Vb2 drops. The loop gain becomes greater than 1 by this action, and positive feedback is present until Q2 suddenly turns OFF (Q1 and Q2 OFF).

Next, the input voltage starts to drop as shown by (b) in the figure.

Vb1 drops, the current flowing through Q1 decreases, and Vc1 starts to drop.

When Vb1 rises, it eventually turns Q2 ON.

When Q2 is on, current starts to flow through it, Ve1 becomes high, and, as a result, the base-to-emitter voltage of Q1 drops, Vc1 steadily rises, and Bb1 becomes high.

In this way, positive feedback is applied, Q1 suddenly turns OFF, and the original stable state is reached (Q1 OFF and Q2 ON).

The above was a description of the theory of operation of the Schmitt circuit. Since a fixed output having a rise time, fall time, and amplitude, in respect to various input signals can be obtained, it is used as a wave-shaping circuit.

One characteristic of a Schmitt circuit is that input voltage E^+ (when Q1 is ON and Q2 is OFF) and input voltage E^- (when Q1 is OFF and Q2 ON) do not coincide. E^+ is higher than E^-; $E^+ - E^- = Eh$, called the hysteresis voltage, becomes the input sensitivity of the Schmitt circuit. The cause of hysteresis is that after Q1 turns ON and Q2 turns OFF, E^+ exceeds the input voltage and Q2 does not turn on since voltage Vb2 becomes extremely low despite the fact that Ve1 is the same as the original voltage even when E^+ drops below the input voltage. It is necessary to make Vb2 large by dropping the input voltage in order to turn Q2 ON and E^- becomes lower than E^+.

The above is shown in diagram form in Fig. 4.14. Since erroneous operation will occur if noise in the signal is greater than Eh, careful attention is required. (Refer to Fig. 4.15.)

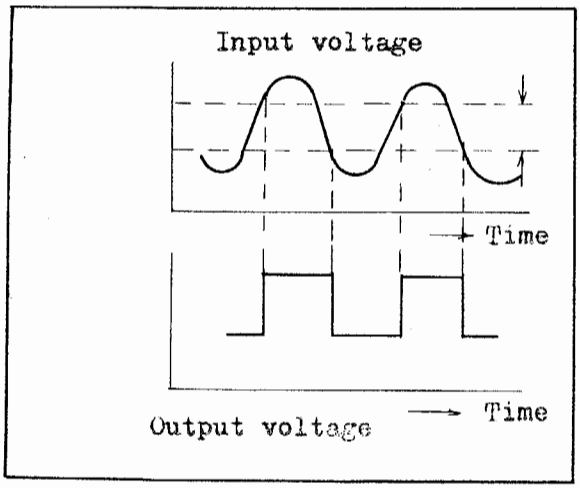


Fig. 4.14 Schmitt circuit output voltage

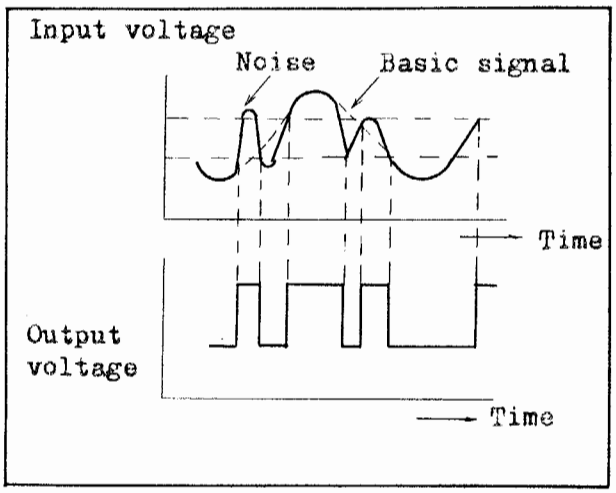


Fig. 4.15 Erroneous operation due to noise

3) One-shot multivibrator

When counting, the accurate internal time base must be divided to a low frequency in order to be used as a TIME UNIT and TIME GATE. Phantastron circuits, one-shot multivibrator circuits, and flip-flop circuits are typical system widely employed to accomplish this.

A description of the one-shot multivibrator will be given here. Unlike the Schmitt circuit described previously and the flip-flop circuit to be described later which have two stable states, this circuit has only one stable state.

The major point of difference between this circuit and Schmitt and flip-flop circuits is that the output waveform can be changed to have any desirable pulse amplitude even when the amplitude of the trigger pulse is small.

A typical one-shot multivibrator is shown in Fig. 4.16.

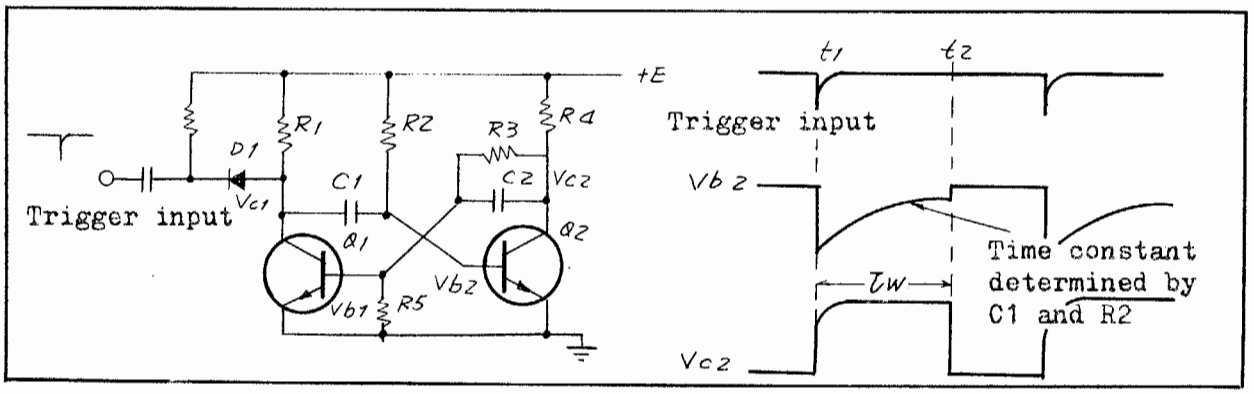


Fig. 4.16 One-shot multivibrator

When +E is applied in Fig. 4.16, Q1 is cutoff (nonconducting) and Q2 conducts (ON state). That is, current flows through Q2 and R2 turns ON, and, as a result, Q1 base voltage (Vb1) drops and Q1 turns OFF.
This is the state prior to t1. If a negative trigger pulse is applied at t1, the base of Q2 is triggered through D1.
This makes voltage Vb2 drop, Vc2 rise, and Vb1 rise. Vc1 drops due to the rise in Vb1, and Vb2 rises through C1.
The t1 state in (b) is the result of this regenerative action. The stable state continues through this period; however, since Vb2 is the voltage charged across C1, C1 discharges through this period; however, since Vb2 is the voltage charged across C1, C1 discharges through R2 (time constant of C1 and R2), as time approaches t2 from t1, Q2 shifts from the OFF state to the ON state at exactly t2, Vb1 drops through R3 and C2, and Vc1 rises. The circuit is shifted to the Q1 OFF, Q2 ON stable state during this instant at t2 by means of this regenerative action. The pulse width τ W at this time is essentially determined by the time constant of C1 and R2 and can be expressed as τ W = 0.7 C1 . R2.
The above has been an explanation of the theory of operation of the one-shot multivibrator. Since any desired pulse width can be obtained by changing the time constant of C1 and R2, this circuit is employed for time division, in addition to circuit delay and voltage control.

3) The flip-flop circuit is the same as the previously described Schmitt circuit in that it is a binary circuit having two stable states.

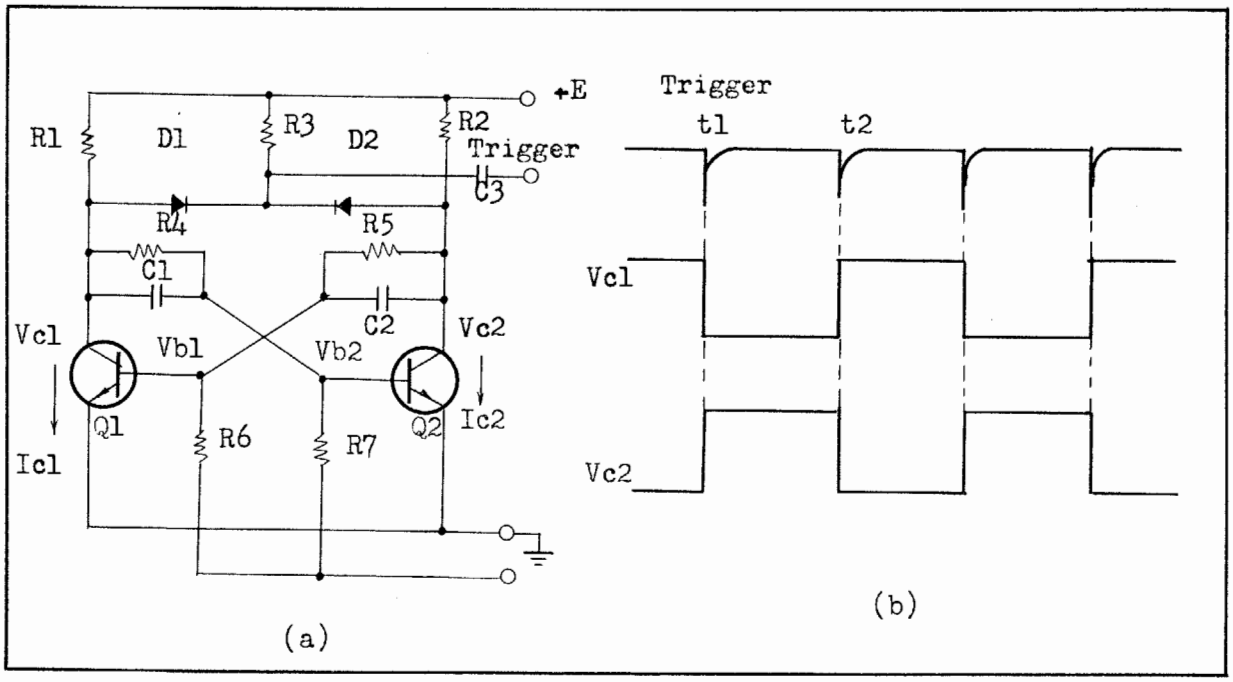


Fig. 4.17 Flip-flop circuit

As shown in the figure, since one output signal is obtained in respect to two input signals, the flip-flop circuit is employed as frequency divider.

The circuit in the figure is a binary divider; however, division to the required order can be obtained by connecting several of them in cascade and applying suitable feedback. Refer to 4.6 for information concerning the decimal divider (counting) circuit. Since the construction in the figure is completely symmetrical, which transistor (Q1 or Q2) enters the ON state when the switch is turned on cannot be predicted. Assume that Q2 is ON. If this is the case, Vc2 becomes 0 V, bias from -E is applied to Q1, and Q1 turns OFF.

This is the stable state prior to t1 in (a) of the figure. If a negative trigger is applied at this time (t1), the pulse cannot pass through D2 since D2 is reverse biased and Vc2 is almost zero since Q2 is ON.

Since Q1 is in the OFF state, the trigger pulse passes through D1, and the Q2 bias voltage drops through D1 and C1.

Hence, Ic2 decreases → Vc2 rises → Vb1 rises → Ic1 starts to flow → Vc1 rises and Q1, Q2 ON OFF are switched by the regenerative action of the drop in Vb2.

This is the second stable state.

If a trigger pulse is applied at t2, the pulse enters at D2 and Q1 and Q2 return to the state they were in prior to time t1.

4.6 Decimal Counting Circuit Operation

There are various types of pulse counting circuits; however, a binary circuit is generally employed because of its counting speed and other factors.

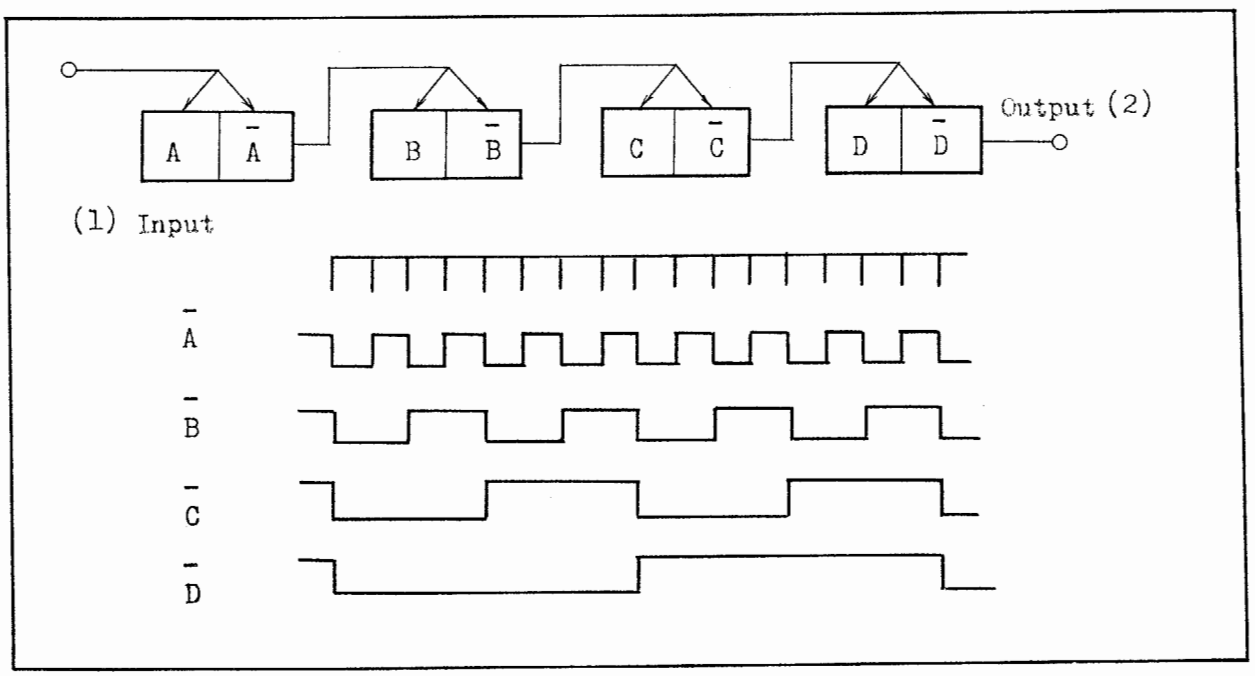


Fig. 4.18 Base 16 counting circuit

This base 16 counting circuit is converted into a decimal counting circuit by applying a suitable gate and feedback.
Refer to 4.7 concerning the integrated circuit employed as the decimal counting circuit.

4.7 Description of the Operation of Each Block

This counter employs a module system and, since it is divided into blocks having various functions, a description of each block will now be given.

1) Time base section (3D45, 3D12)

The time base section is the heart of the counter. The time base section of this counter is 3D45 and 3D12.

The time base section is broadly classified into a 1 MHz crystal oscillator circuit, a wave-shaping circuit for its output or for an external time base signal, and dividing circuits down to 0.25 Hz.
Its form when 4 flip-flops are connected in cascade is shown in Fig. 4.18. If this construction is employed since one output pulse is obtained in respect to two input pulses, in the so-called base 16 circuit, 1 output pulse will be obtained for every 16 input pulses. As shown in Fig. 4.19, flip-flops J - K are used to obtain a decimal divider. That is, the transistor in the ON state shifts to the OFF state and the transistor in the OFF states inverts to the ON state. The action following the second stage is shown in the time chart at the bottom of Fig. 4.19. This forms a decimal divider having 1 output pulse for every 10 input pulses.
In the dividing circuit (5D45, 5D12), the 1 MHz from the crystal oscillator is divided to 25 Hz, 2.5 Hz, etc. by the use of 6 decimal divider stages and a base 4 divider circuit.

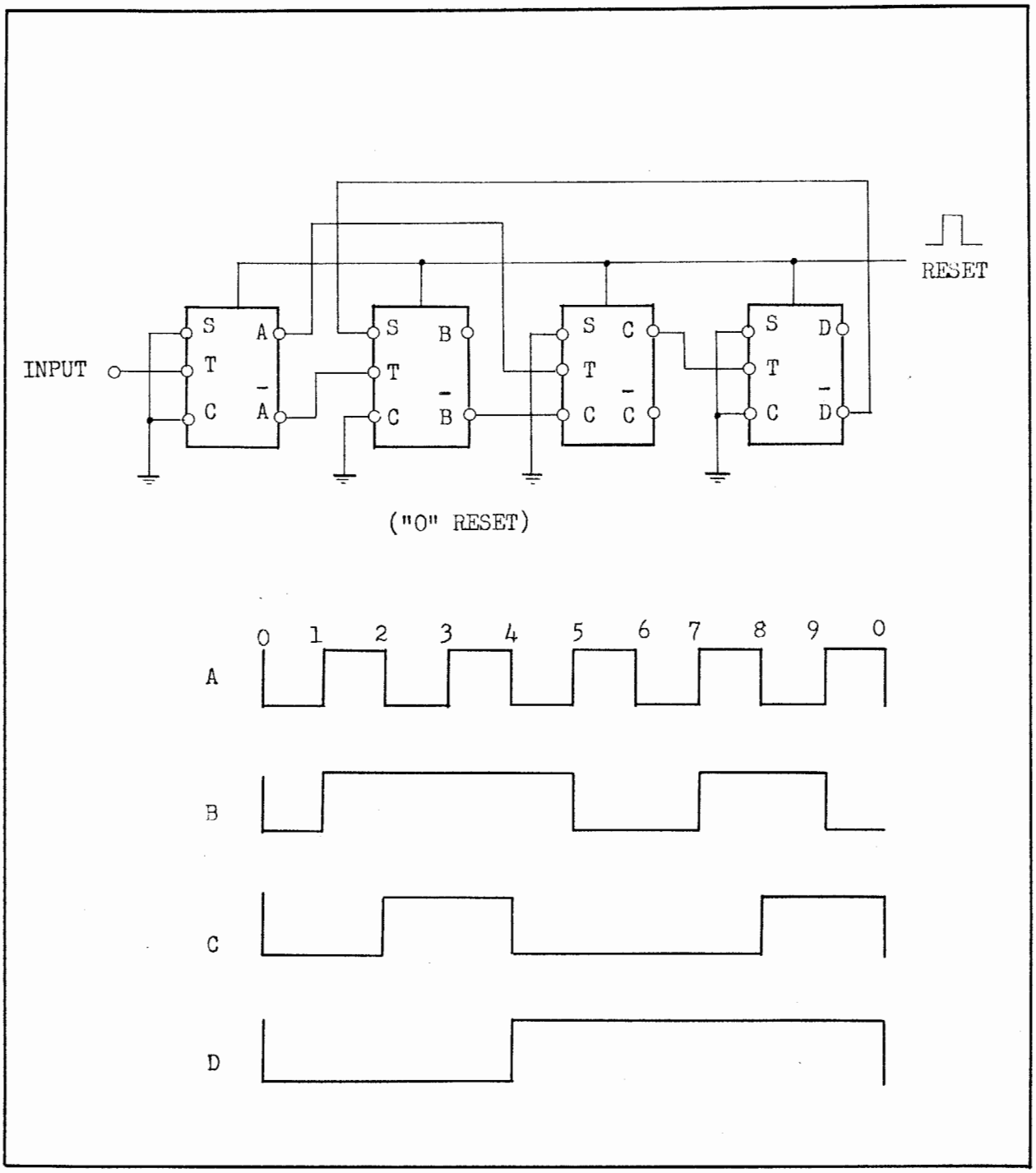


Fig. 4.19 Decimal divider formed from flip-flops J and K

2) Gate control circuit (3B30, 3B12)

The gate control circuit (3B40, 3B12) controls the opening and closing of the signal gate at a set time interval. In addition, it also controls the sampling time after counting or at any desired time, generates a reset pulse to manually reset all circuits to their original zero state, generates a memory pulse to instruct the memory during memory display, and is the circuit which lights the neon tube during the period when the gate is open.

Fig. 4.20 is a block diagram of 3B40 and 3B12. Binary in the diagram is a special name for a flip-flop. A one-shot circuit is employed.

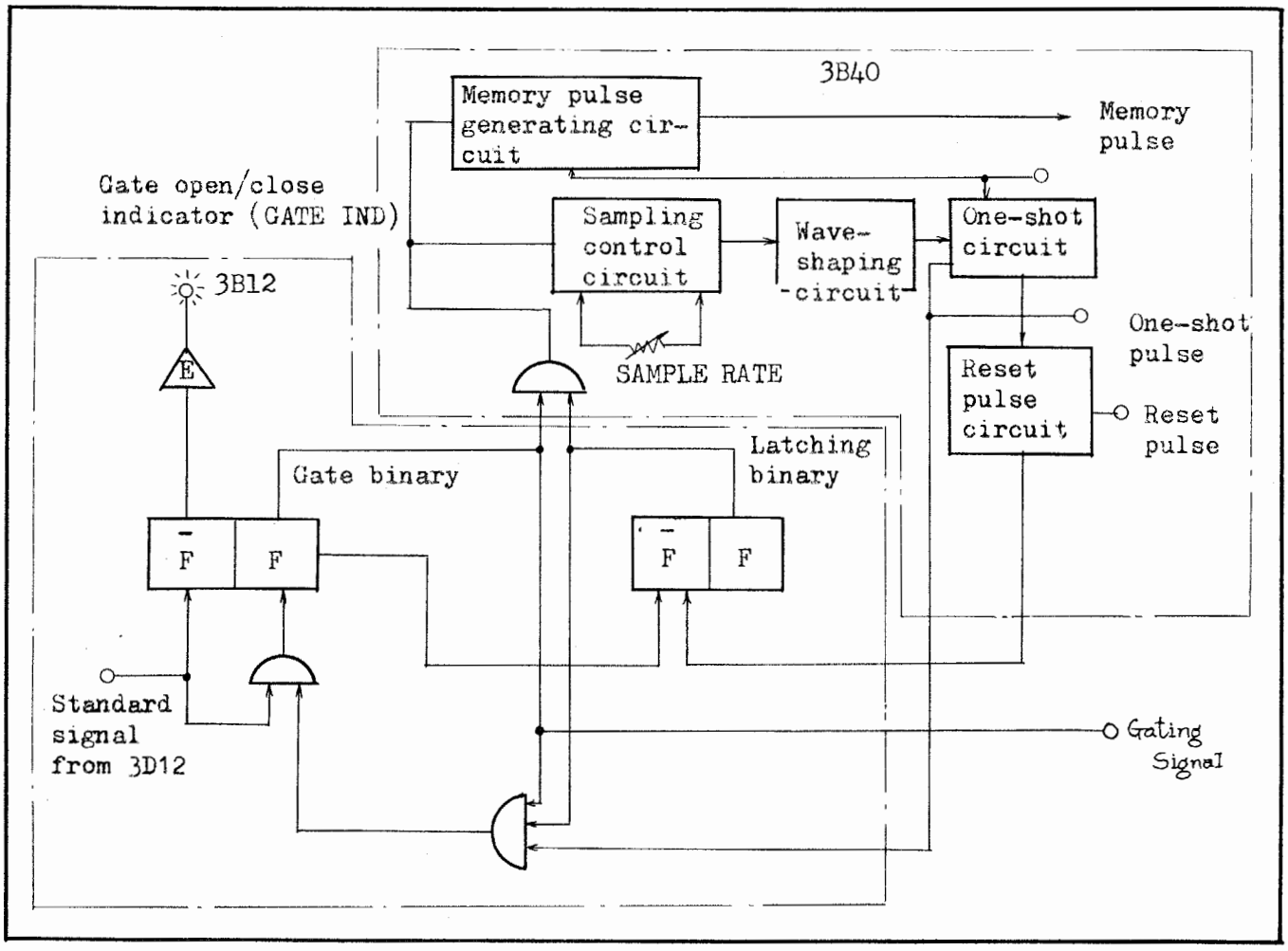


Fig. 4.20 3B40, 3B12 block diagram

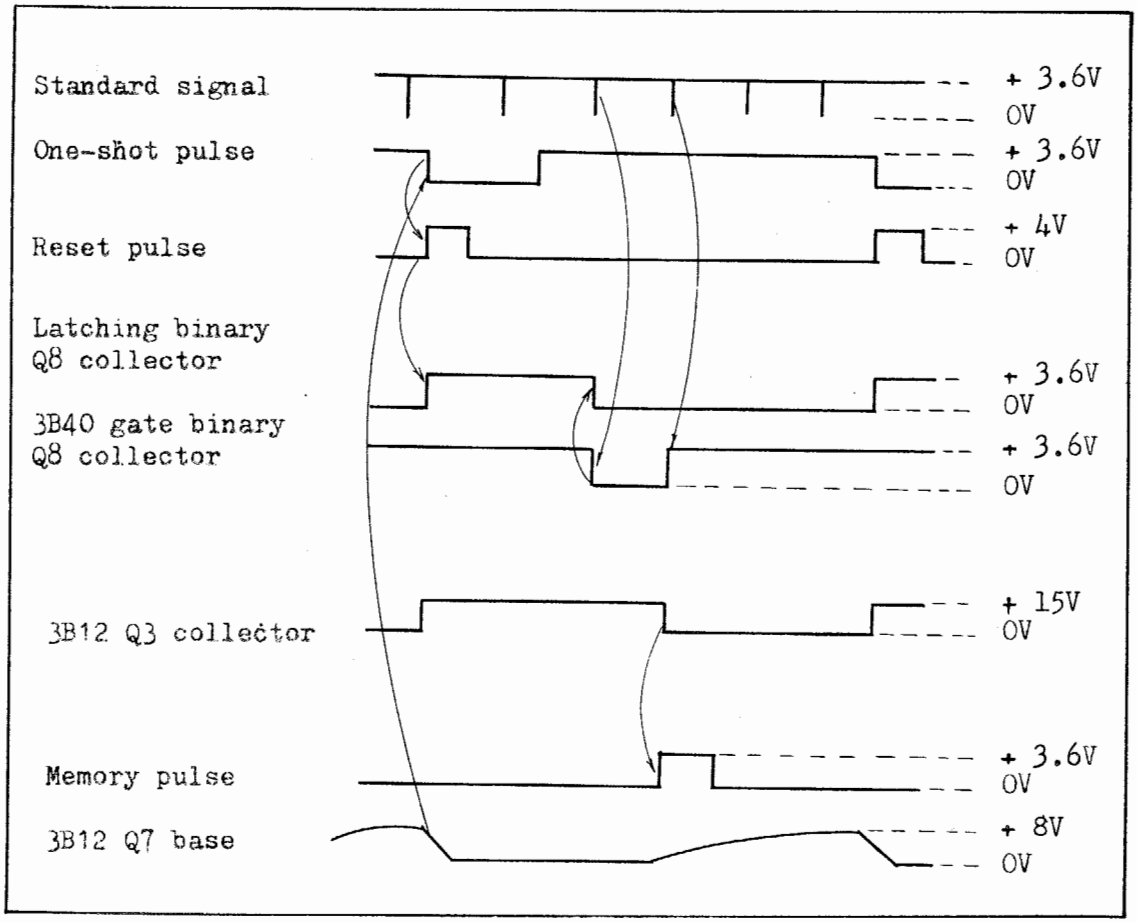


Fig. 4.21 3B40, 3B12 timing chart

3) 15 MHz counting circuit ([redacted])

This circuit divides a wide range of frequencies (0.25 Hz ~ 15 MHz) by 10:1. This circuit is called a counting circuit not because it divides in the manner of a dividing circuit but because it displays the counted result.

This is the same as the dividing circuit described previously; however, as shown in Fig. 4.22, there is no feedback but it is changed into a decimal counting circuit by means of the gate circuit. This is done to obtain high resolution since there is a phase delay when feedback is employed.

Fig. 4.22 shows the operating waveforms in various points in the circuit.

4) Other circuits

In addition to the blocks (circuits) already described in the above, there are blocks which shape the output of the wideband amplifier, a 40: 1 dividing circuit, 2 MHz counting circuit (3C40), display circuit (3C10), and power supply circuit (3E14).

3C40 is the 2 MHz counting circuit which contains the display circuit and memory circuit.

3C10 is the count display circuit and memory circuit for the counted result.

5) General

The above has been a description of the individual circuits employed in this counter. The various circuits are combined in the instrument to satisfy all the specifications in section 2.

A general block diagram of the counter appears in Fig. 4.23.

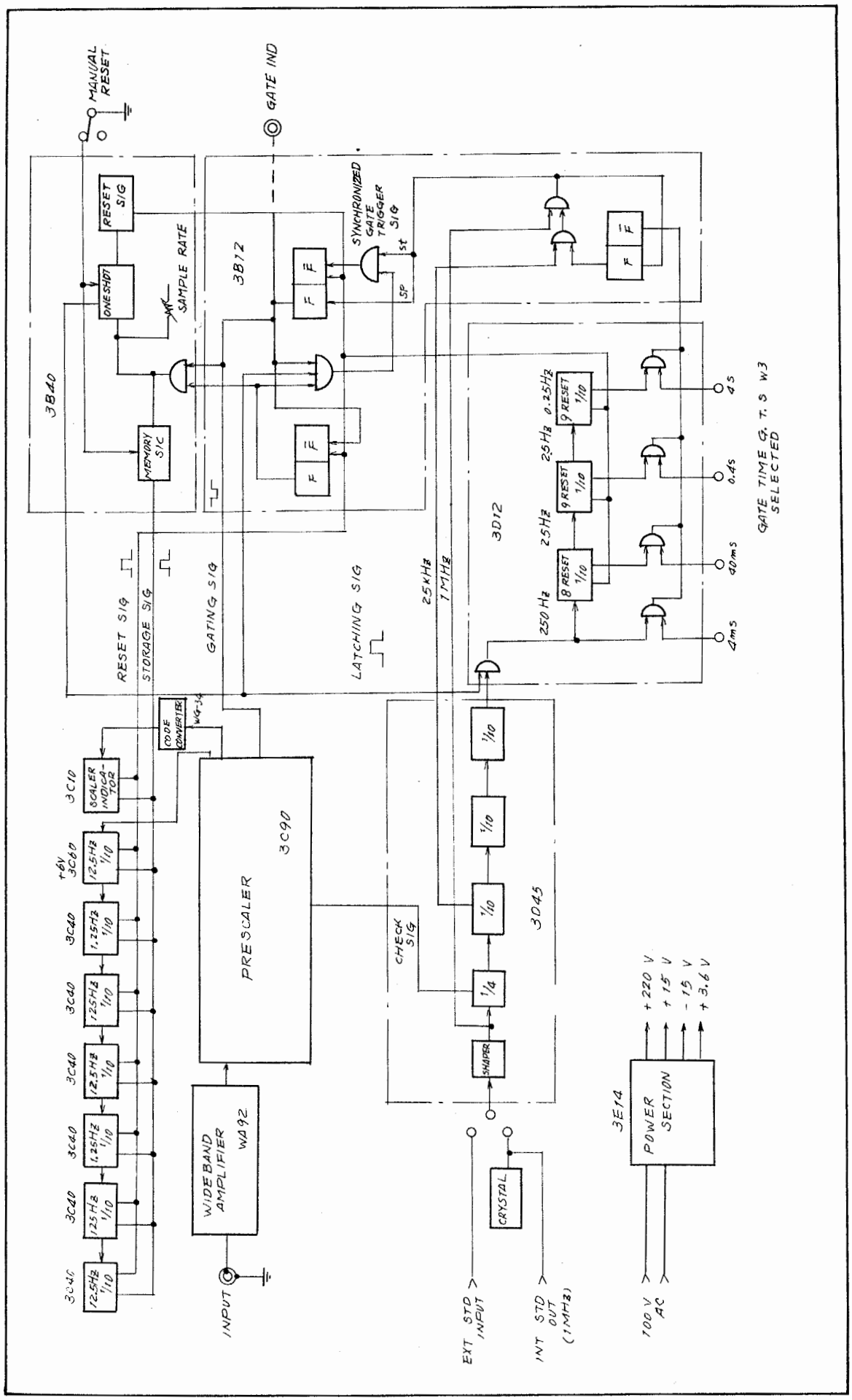


Fig. 4.23 General block diagram of the -TR-3787/3788