2N5060 Series

Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Annular PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO−92/TO-226AA package which is readily adaptable for use in automatic insertion equipment.

Features

- Sensitive Gate Trigger Current − 200 μA Maximum
- Low Reverse and Forward Blocking Current − 50 μA Maximum, T_C = 110°C
- Low Holding Current − 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- These are Pb−Free Devices

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = −40 to 110°C, Sine Wave, 50 to 60 Hz, R_{GK} = 1 kΩ) 2N5060 2N5061 2N5062 2N5064	V_{DRM}, V_{RRM}	30 60 100 200	V
On-State Current RMS (180° Conduction Angles; T_C = 80°C)	$I_{T(RMS)}$	0.8	A
*Average On-State Current (180° Conduction Angles) (T_C = 67°C) (T_C = 102°C)	$I_{T(AV)}$	0.51 0.255	A
*Peak Non-repetitive Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	A
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.4	A^2s
*Average On-State Current (180° Conduction Angles) (T_C = 67°C) (T_C = 102°C)	$I_{T(AV)}$	0.51 0.255	A
*Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec; T_A = 25°C)	P_{GM}	0.1	W
*Forward Average Gate Power (T_A = 25°C, t = 8.3 ms)	$P_{G(AV)}$	0.01	W
*Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec; T_A = 25°C)	I_{GM}	1.0	A
*Reverse Peak Gate Voltage (Pulse Width ≤ 1.0 μsec; T_A = 25°C)	V_{RGM}	5.0	V
*Operating Junction Temperature Range	T_J	−40 to +110	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*Indicates JEDEC Registered Data.

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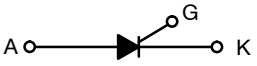
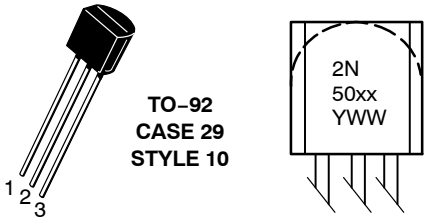
SILICON CONTROLLED RECTIFIERS
0.8 A RMS, 30 − 200 V



MARKING DIAGRAM



TO−92
CASE 29
STYLE 10

50xx = Specific Device Code
Y = Year
WW = Work Week

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction−to−Case (Note 2)	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W

2. This measurement is made with the case mounted “flat side down” on a heatsink and held in position by means of a metal clamp over the curved surface.

*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

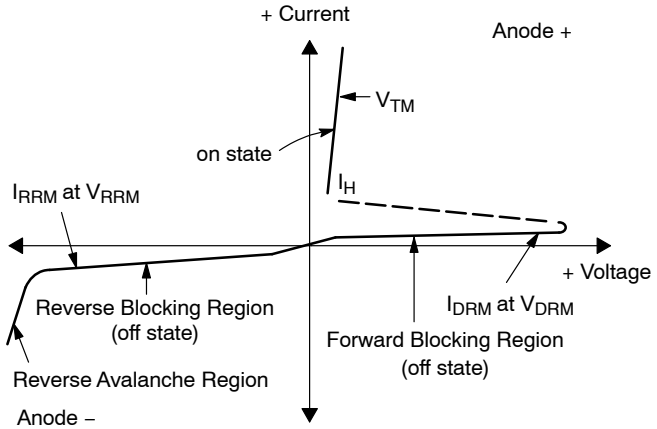
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
*Peak Repetitive Forward or Reverse Blocking Current (Note 3)		I_{DRM}, I_{RRM}				
(V_{AK} = Rated V_{DRM} or V_{RRM})	T_C = 25°C		–	–	10	μA
	T_C = 110°C		–	–	50	μA
ON CHARACTERISTICS						
*Peak Forward On−State Voltage (Note 4)		V_{TM}	–	–	1.7	V
(I_{TM} = 1.2 A peak @ T_A = 25°C)						
Gate Trigger Current (Continuous DC) (Note 5)		I_{GT}				μA
*(V_{AK} = 7.0 Vdc, R_L = 100 Ω)	T_C = 25°C		–	–	200	
	T_C = −40°C		–	–	350	
Gate Trigger Voltage (Continuous DC) (Note 5)	T_C = 25°C	V_{GT}	–	–	0.8	V
*(V_{AK} = 7.0 Vdc, R_L = 100 Ω)	T_C = −40°C		–	–	1.2	
*Gate Non−Trigger Voltage		V_{GD}				V
(V_{AK} = Rated V_{DRM}, R_L = 100 Ω) T_C = 110°C			0.1	–	–	
Holding Current (Note 3)	T_C = 25°C	I_H	–	–	5.0	mA
*(V_{AK} = 7.0 Vdc, initiating current = 20 mA)	T_C = −40°C		–	–	10	
Turn-On Time						μs
Delay Time		t_d	–	3.0	–	
Rise Time		t_r	–	0.2	–	
(I_{GT} = 1.0 mA, V_D = Rated V_{DRM}, Forward Current = 1.0 A, di/dt = 6.0 A/μs						
Turn-Off Time		t_q				μs
(Forward Current = 1.0 A pulse, Pulse Width = 50 μs, 0.1% Duty Cycle, di/dt = 6.0 A/μs, dv/dt = 20 V/μs, I_{GT} = 1 mA)	2N5060, 2N5061		–	10	–	
	2N5062, 2N5064		–	30	–	
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off−State Voltage		dv/dt	–	30	–	V/μs
(Rated V_{DRM}, Exponential, R_{GK} = 1 kΩ)						

*Indicates JEDEC Registered Data.

3. R_{GK} = 1000 Ω is included in measurement.
4. Forward current applied for 1 ms maximum duration, duty cycle ≤ 1%.
5. R_{GK} current is not included in measurement.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak on State Voltage
I_H	Holding Current



CURRENT DERATING

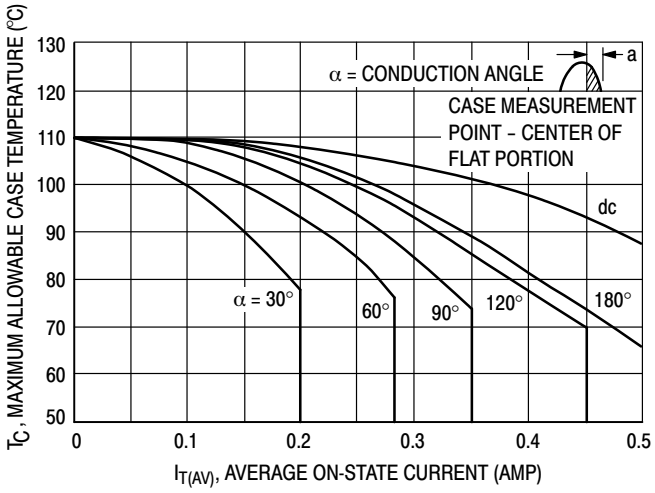


Figure 1. Maximum Case Temperature

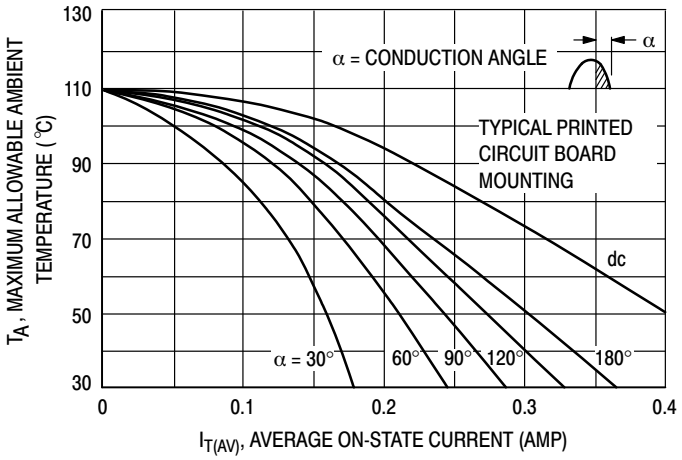


Figure 2. Maximum Ambient Temperature

CURRENT DERATING

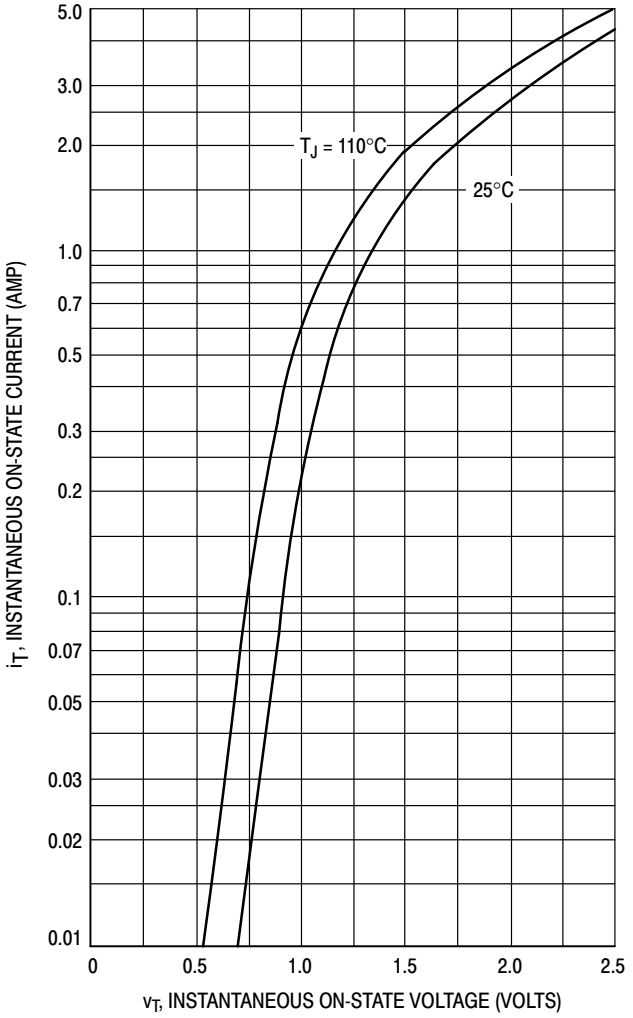


Figure 3. Typical Forward Voltage

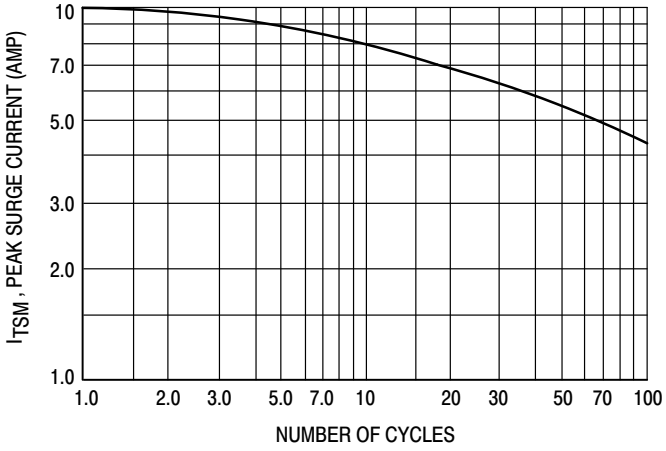


Figure 4. Maximum Non−Repetitive Surge Current

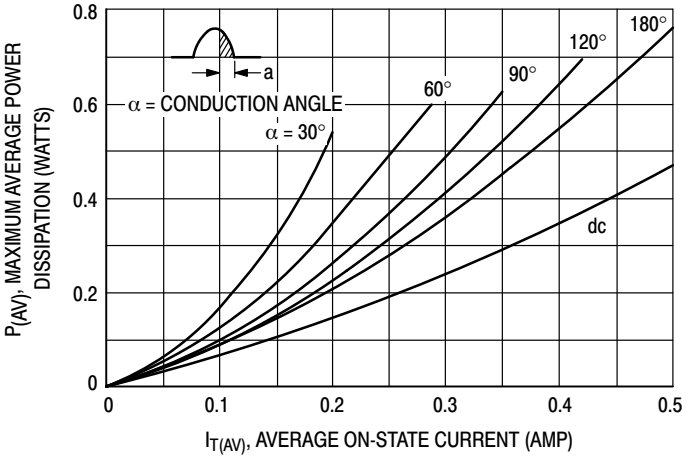


Figure 5. Power Dissipation

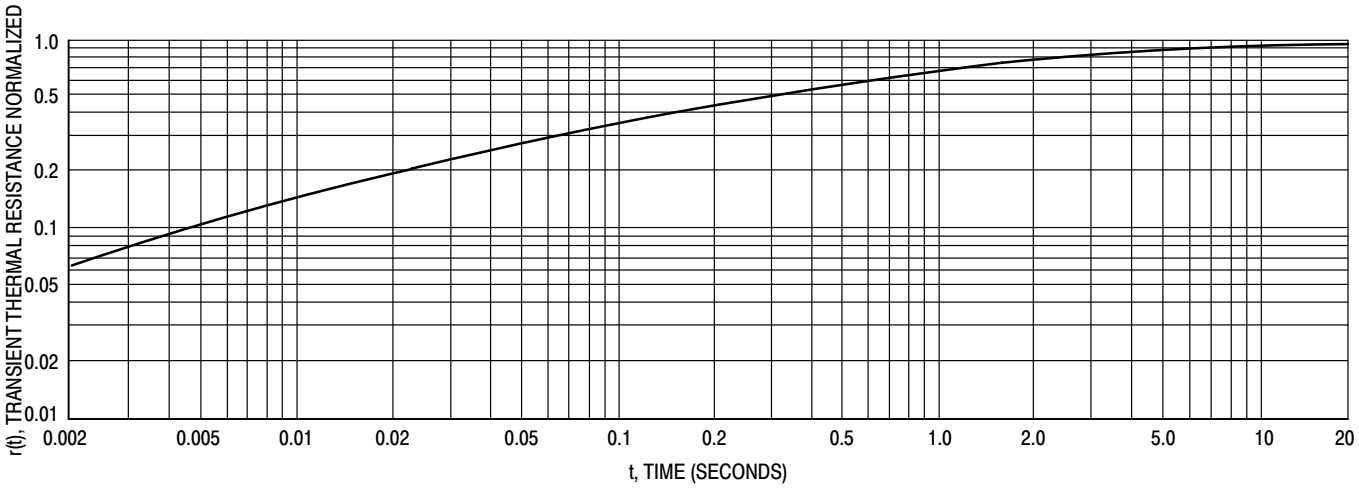


Figure 6. Thermal Response

TYPICAL CHARACTERISTICS

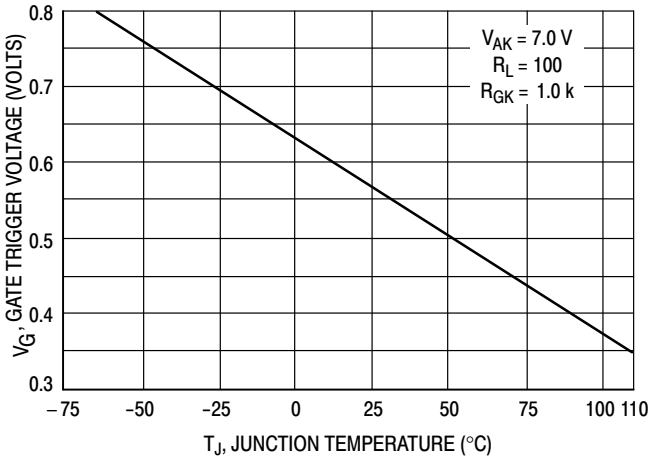


Figure 7. Typical Gate Trigger Voltage

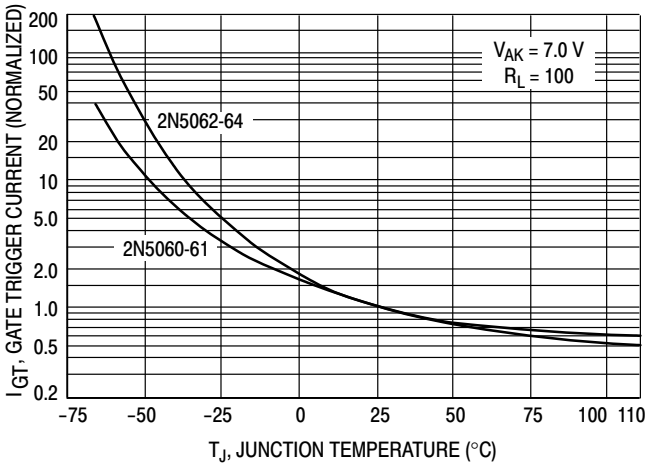


Figure 8. Typical Gate Trigger Current

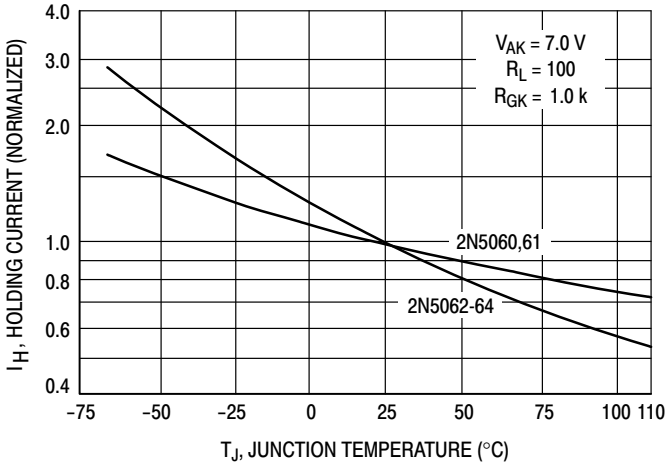


Figure 9. Typical Holding Current

ORDERING INFORMATION

Device	Package	Shipping†
2N5060G	TO−92 (Pb−Free)	5000 Units / Box
2N5060RLRA	TO−92	2000 / Tape & Reel
2N5060RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N5060RLRMG	TO−92 (Pb−Free)	2000 / Ammo Pack
2N5061G	TO−92 (Pb−Free)	5000 Units / Box
2N5061RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N5062G	TO−92 (Pb−Free)	5000 Units / Box
2N5062RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N5064RLRMG	TO−92 (Pb−Free)	2000 / Ammo Pack
2N5064RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N5064G	TO−92 (Pb−Free)	5000 Units / Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

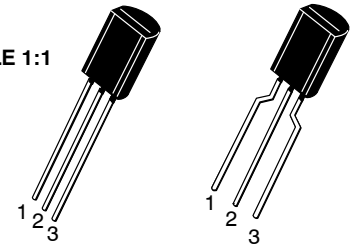
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

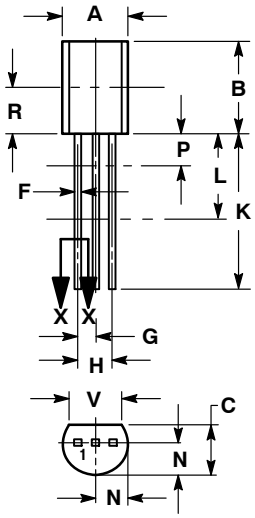
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

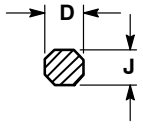
SCALE 1:1



STRAIGHT LEAD BENT LEAD



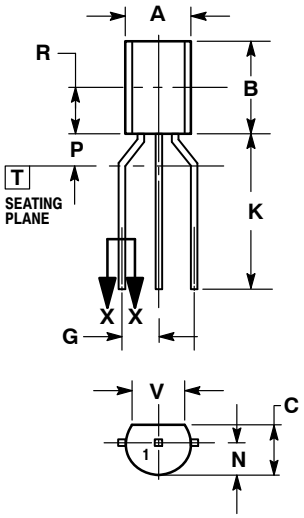
STRAIGHT LEAD



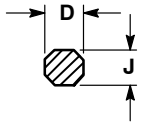
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



BENT LEAD



SECTION X−X

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	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 1 OF 2**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

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